DR1 (Roberts) Schematics Document

uFCPGA Mobile Penryn

Intel Cantiga-GM + ICH9M

2008-10-02

REV : A00

DY : Nopop Component

<Core Design>

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Roberts Block Diagram

Project code : 91.4AQ01.001
PCB P/N : 48.4AQ01.011
Revision : 08212-1

Clock Generator
SLG8SP513VTR 4

Intel Mobile CPU
Penryn
Socket P
5,6,7

FSB
800/1066MHz

Intel
Cantiga-GML
AGTL+ CPU I/F
DDR Memory I/F
External Graphics
8,9,10,11,12,13

DDRII 667/800 Slot 0 14
DDRII 667/800 Slot 1 15
DDRII 667/800 Channel A
DDR II 667/800 Channel B

RGB CRT
LVDS(Dual Channel)
CRT (on I/O board)
LCD 35

DMIx4
C-LINK

Intel
ICH9-M
USB 2.0/1.1 ports (12)
PCI Express ports (6)
High Definition Audio
SATA ports (4)
LPC I/F
ACPI 1.1
PCI/PCI BRIDGE
16,17,18,19

PCIE
USB 2.0
LPC Bus
SATA
SATA

Power SW
G577BR91U 41
New Card 41
PCIE x 1 & USB 2.0 x 1
PCIE x 1
10/100 NIC
Marvell 88E8040 20
RJ45 CONN
I/O Board Connector 41
USB 2.0 x 2
Left Side: USB x 2
Mini-Card
802.11a/b/g 37
PCIE x 1
CAMERA (Option) 41
USB 2.0 x 1
Bluetooth 41
USB 2.0 x 1
Right Side: USB x 1 43
USB 2.0 x 1

SD/MMC
MS/MS Pro/xD 37
CardReader
Realtek
RTS5158E 21
USB2.0

CAMERA Module
Digital Mic Array
MIC IN
Internal Analog MIC
Azalia
CODEC
IDT
92HD71B7 22
AZALIA

HP1
OP AMP
MAX9789A 23
2CH SPEAKER
40

KBC
WINBOND
WPCE773L 24
SPI

HDD 36
ODD 36
Flash ROM
2MB 42
Touch PAD 44
Int. KB 44
Thermal & Fan
EMC2102 25

CPU DC/DC ISL6266A 28,29	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC TPS51117 30	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VCCP

SYSTEM DC/DC MAX17020 27	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

SYSTEM DC/DC TPS51116 31	
INPUTS	OUTPUTS
+PWR_SRC	+1.8V_SUS +0.9V_DDR_VTT +V_DDR_MCH_REF

SYSTEM DC/DC APL5912 32	
INPUTS	OUTPUTS
+1.8V_SUS	+1.5V_RUN

SYSTEM DC/DC LDO 34	
INPUTS	OUTPUTS
+5V_ALW +3.3V_ALW	+5V_RUN +3.3V_RUN

MAXIM CHARGER MAX8731A 26	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

PCB LAYER

L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom

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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK.	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 Rev.0.5

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) **1 = The iTPM Host Interface is disabled (default)**
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality(Default)**
CFG9	PCIE Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. **1 = Normal operation (Default): Lane Numbered in Order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1 = Disable (Default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) **11 = Disabled (Default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation (Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3 DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 = Digital display Port and PCIe are operating simulataneously via the PEG port
SDVO _CTRLDATA	SDVO Present	**0 = No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1 = LFP Card Present; PCIE disabled

NOTE:

1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

PCIE Routing

LANE2	MiniCard WLAN
LANE3	LAN
LANE5	New Card

USB Table

USB	
Pair	Device
0	USB1
1	USB2
2	USB3
3	RESERVED
4	MINI CARD
5	RESERVED
6	BLUETOOTH
7	NEW CARD
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

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Title: Table of Content

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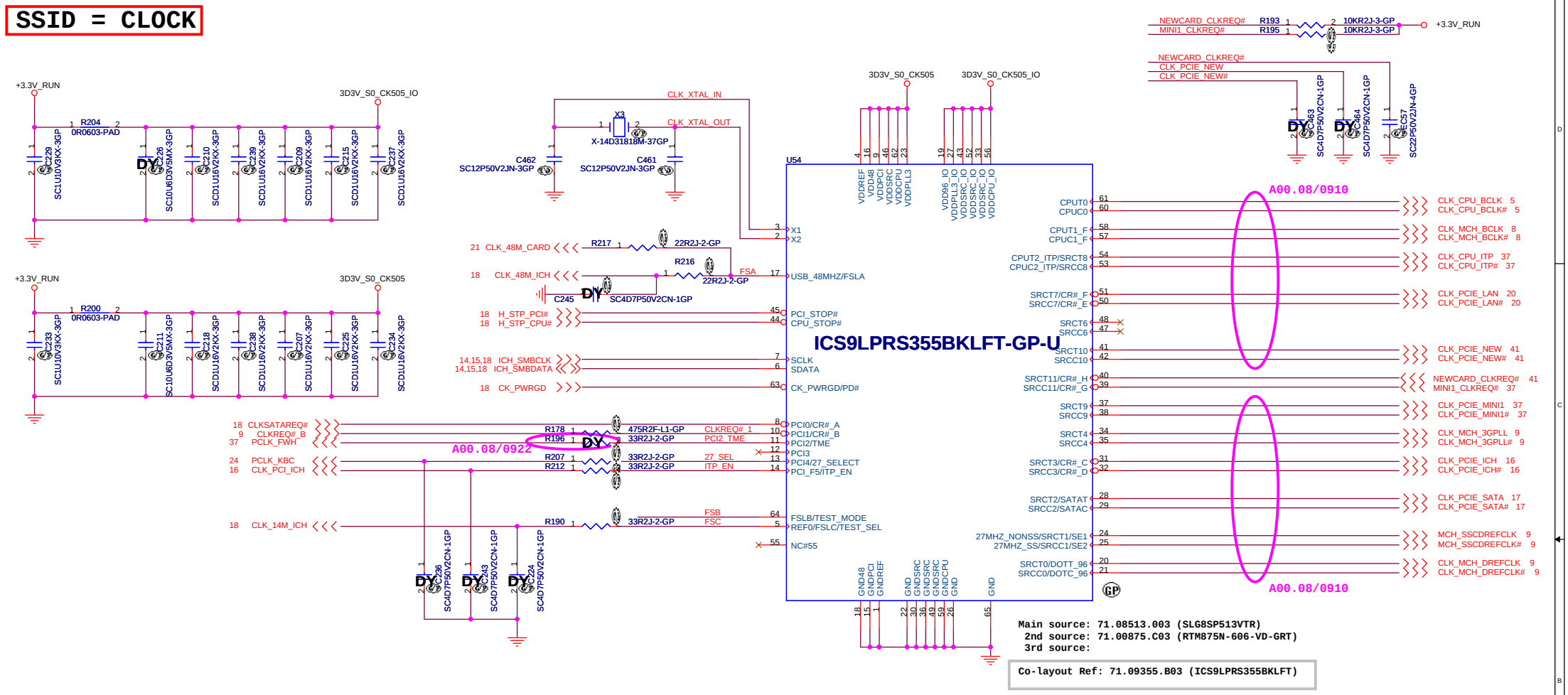
SSID = CLOCK



ITP_EN	Output
0	SRC8
1	CPU_ITP

PCI2_TME	Output
0	Overclocking of CPU and SRC allowed
1	Overclocking of CPU and SRC not allowed

27_SEL	PIN 20	PIN 21	
0	DOT96T	DOT96C	GM45
1	SRCT0	SRCC0	PM45

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

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Title: Clock Generator SLG8SP513VTR

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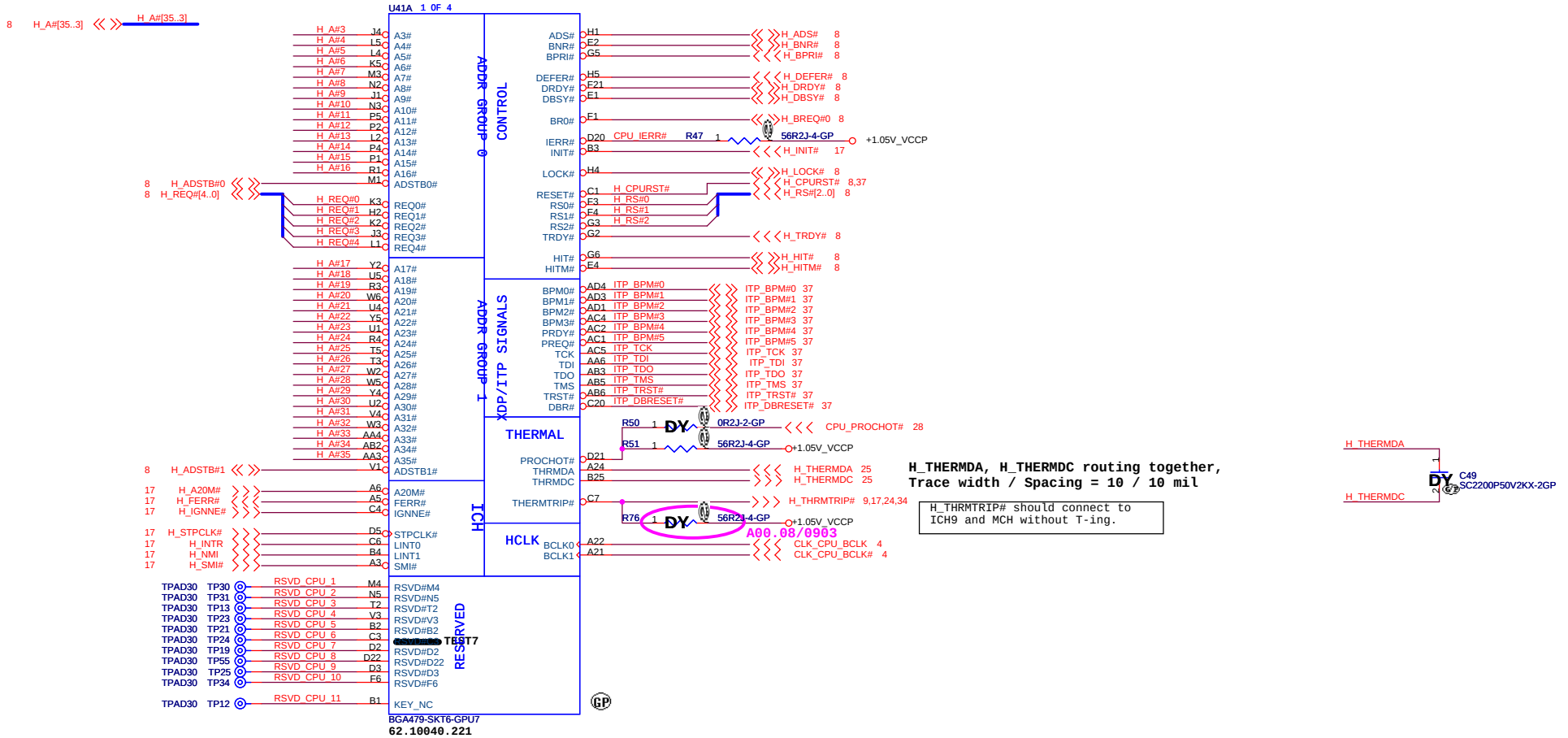
SSID = CPU



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Title: ***CPU-FSB(1/3)***

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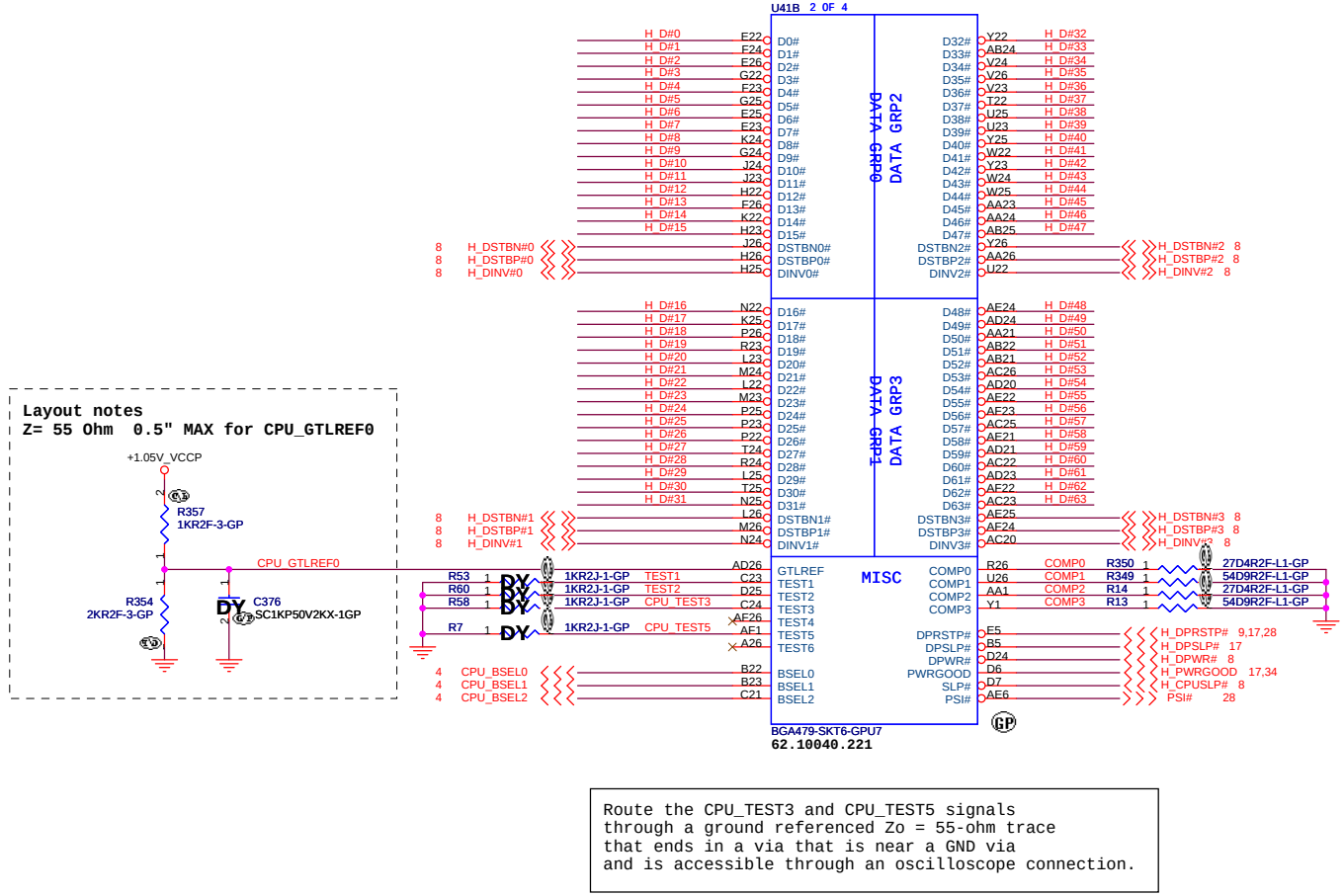
SSID = CPU

H_DINV#[3..0] → H_DINV#[3..0] 8
H_DSTBN#[3..0] → H_DSTBN#[3..0] 8
H_DSTBP#[3..0] → H_DSTBP#[3..0] 8
H_D#[63..0] → H_D#[63..0] 8



Layout notes
Z= 55 Ohm 0.5" MAX for CPU_GTLREF0

R53 1 DY 1KR2J-1-GP TEST1
R60 1 DY 1KR2J-1-GP TEST2
R58 1 DY 1KR2J-1-GP CPU_TEST3
R7 1 DY 1KR2J-1-GP CPU_TEST5

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

Route the CPU_TEST3 and CPU_TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

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Title: CPU-FSB(2/3)
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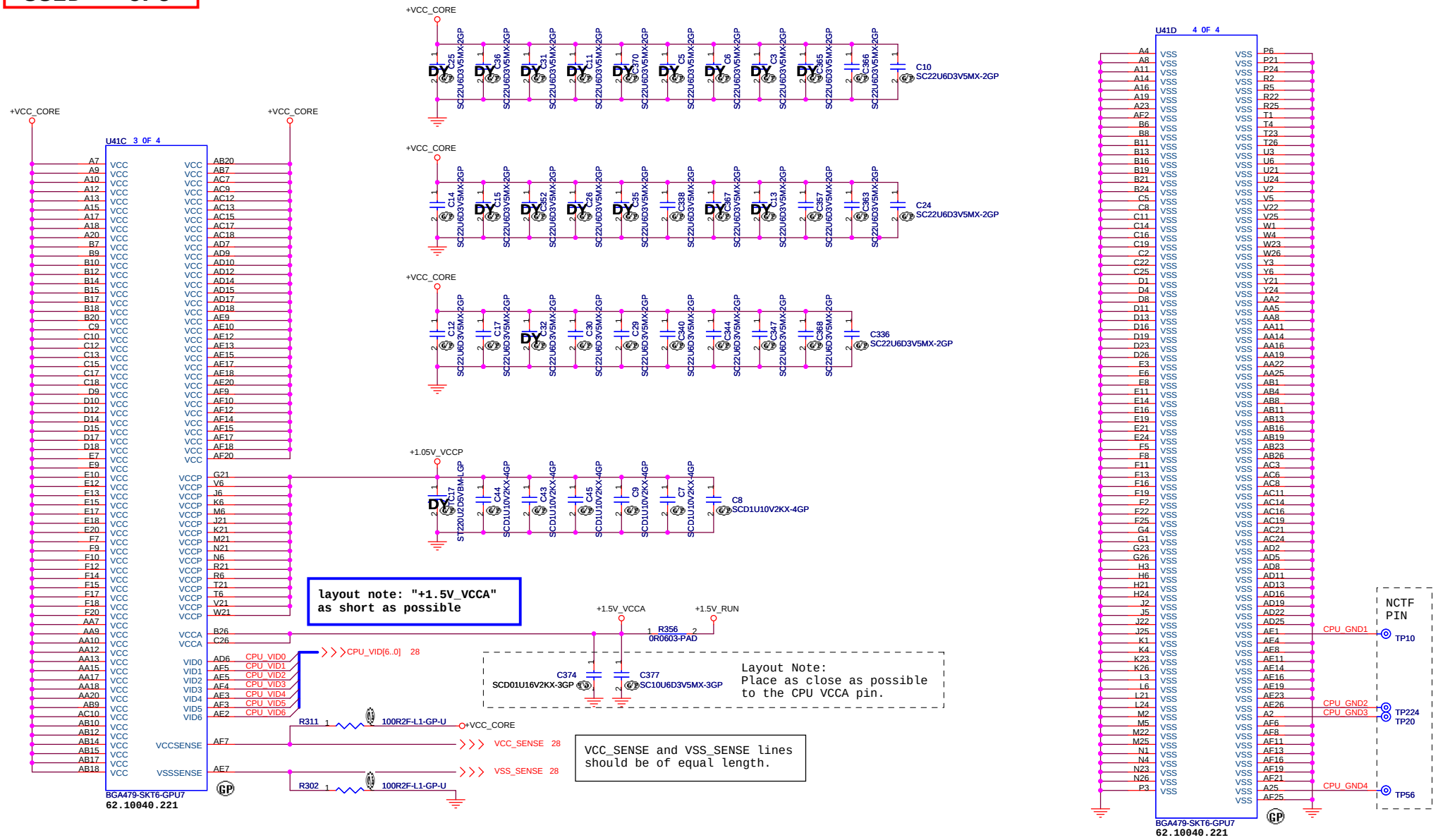
SSID = CPU



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Title	CPU-Power(3/3)	
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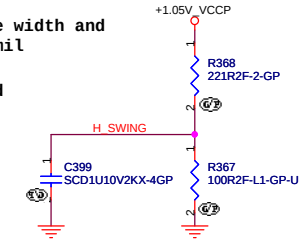
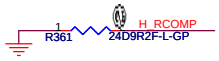
SSID = MCH

H_SWING routing Trace width and Spacing use 10 / 20 mil

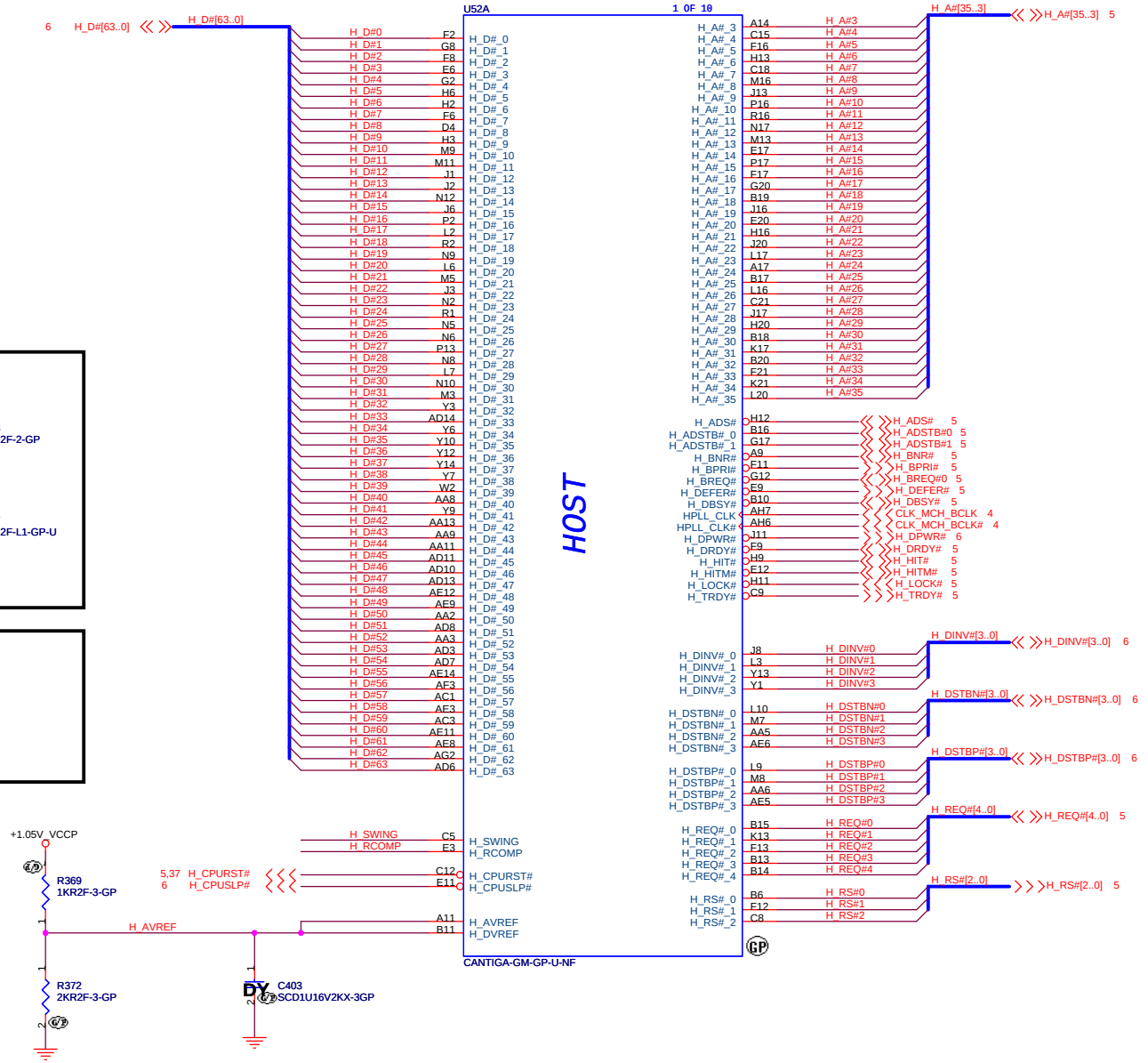
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place R51 near to the chip (< 0.5")



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Title: Cantiga-HOST(1/6)

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SSID = MCH

* is current setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	ITPM enable	ITPM disable *
CFG 7	TLS cipher suite with no confidentiality	TLS cipher suite with confidentiality *
CFG 9	PCIE GFX lane reversed	PCIE GFX lane numbered in oder *
CFG 10	PCIE loopback enable	PCIE loopback disable *
CFG 12	ALLZ mode enable	ALLZ mode disable *
CFG 13	XOR mode enable	XOR mode disable *
CFG 16	FSB dynamic ODT disable	FSB Dynamic ODT enable *
CFG 19 DMI Lane Reserved	Normal operation *	Reverse DMI lanes
CFG 20 SDVO concurrent with PCIE	Only PCIE or SDVO is operational *	PCIE and SDVO are operatiing simultaneously via the PEG port
SDVO_CTRLDATA	SDVO interface disable *	SDVO interface enable
L_DDC_DATA	LFP disable *	LFP card present
DDPC_CTRLDATA	SDVO/iHDMI/DP interface disabled *	SDVO/iHDMI/DP interface enabled

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RSVD: M36 RESERVED#M36, N36 RESERVED#N36, R33 RESERVED#R33, T33 RESERVED#T33, AH9 RESERVED#AH9, AH10 RESERVED#AH10, AH12 RESERVED#AH12, AH13 RESERVED#AH13, K12 RESERVED#K12, AL34 RESERVED#AL34, AK34 RESERVED#AK34, AN35 RESERVED#AN35, AM35 RESERVED#AM35, T24 RESERVED#T24, B31 RESERVED#B31, B2 RESERVED#B2, M1 RESERVED#M1, AY21 RESERVED#AY21, BG23 RESERVED#BG23, BF23 RESERVED#BF23, BH18 RESERVED#BH18, BF18 RESERVED#BF18

DDR CLK/ CONTROL/COMPENSATION: SA_CK_0 AP24 M_CLK_DDR0 14; SA_CK_1 AT21 M_CLK_DDR1 14; SB_CK_0 AV24 M_CLK_DDR2 15; SB_CK_1 AU20 M_CLK_DDR3 15; SA_CK#_0 AR24 M_CLK_DDR#0 14; SA_CK#_1 AR21 M_CLK_DDR#1 14; SB_CK#_0 AU24 M_CLK_DDR#2 15; SB_CK#_1 AV20 M_CLK_DDR#3 15; SA_CKE_0 BC28 M_CKE0 14; SA_CKE_1 AY28 M_CKE1 14; SB_CKE_0 AY36 M_CKE2 15; SB_CKE_1 BB36 M_CKE3 15; SA_CS#_0 BA17 M_CS0# 14; SA_CS#_1 AY16 M_CS1# 14; SB_CS#_0 AV16 M_CS2# 15; SB_CS#_1 AR13 M_CS3# 15; SA_ODT_0 BD17 M_ODT0 14; SA_ODT_1 AY17 M_ODT1 14; SB_ODT_0 BF15 M_ODT2 15; SB_ODT_1 AY13 M_ODT3 15; SM_RCOMP BG22 M_RCOMPP; SM_RCOMP# BH21 M_RCOMPN; SM_RCOMP_VOH BF28 SM_RCOMP_VOH; SM_RCOMP_VOL BH28 SM_RCOMP_VOL; SM_VREF AV42; SM_PWROK AR36; SM_REXT BF17 SM_REXT R374 1 2 499R2F-2-GP; SM_DRAMRST# BC36

CLK: DPLL_REF_CLK B38 CLK_MCH_DREFCLK; DPLL_REF_CLK# A38 CLK_MCH_DREFCLK#; DPLL_REF_SSCLK E41 MCH_SSCDREFCLK; DPLL_REF_SSCLK# F41 MCH_SSCDREFCLK#; PEG_CLK F43 CLK_MCH_3GPLL; PEG_CLK# F43 CLK_MCH_3GPLL#

DMI: DMI_RXN_0 AE41 DMI_TXN0; DMI_RXN_1 AE37 DMI_TXN1; DMI_RXN_2 AE47 DMI_TXN2; DMI_RXN_3 AH39 DMI_TXN3; DMI_RXP_0 AE40 DMI_TXP0; DMI_RXP_1 AE38 DMI_TXP1; DMI_RXP_2 AE48 DMI_TXP2; DMI_RXP_3 AH40 DMI_TXP3; DMI_TXN_0 AE35 DMI_RXN0; DMI_TXN_1 AE43 DMI_RXN1; DMI_TXN_2 AE46 DMI_RXN2; DMI_TXN_3 AH42 DMI_RXN3; DMI_TXP_0 AD35 DMI_RXP0; DMI_TXP_1 AE44 DMI_RXP1; DMI_TXP_2 AE46 DMI_RXP2; DMI_TXP_3 AH43 DMI_RXP3

CFG: CFG_0 T25, CFG_1 R25, CFG_2 P25, CFG_3 P20, CFG_4 P24, CFG_5 C25, CFG_6 N24, CFG_7 M24, CFG_8 E21, CFG_9 C23, CFG_10 C24, CFG_11 N21, CFG_12 P21, CFG_13 T21, CFG_14 R20, CFG_15 M20, CFG_16 L21, CFG_17 H21, CFG_18 P29, CFG_19 R28, CFG_20 T28

GRAPHICS VID: GFX_VID_0 B33, GFX_VID_1 B32, GFX_VID_2 G33, GFX_VID_3 F33, GFX_VID_4 F33; GFX_VR_EN C34

PM: PM_SYNC# R29, PM_DPRSTP# B7, PM_EXT_TS#_0 N33, PM_EXT_TS#_1 P32, PWROK AT40, RSTIN# AT11, THERMTRIP# T20, DPRSLPVR R32

ME: CL_CLK AH37 CL_CLK0 18; CL_DATA AH36 CL_DATA0 18; CL_PWROK AN36 M_PWROK 18; CL_RST# AJ35 CL_RST#0 18; CL_VREF AH34 MCH_CLVREF

MCH_CLVREF ~= 0.35V

NC: NC#BG48 BG48, NC#BF48 BF48, NC#BD48 BD48, NC#BC48 BC48, NC#BH47 BH47, NC#BG47 BG47, NC#BE47 BE47, NC#BH46 BH46, NC#BF46 BF46, NC#BG45 BG45, NC#BH44 BH44, NC#BH43 BH43, NC#BH6 BH6, NC#BH5 BH5, NC#BG4 BG4, NC#BH3 BH3, NC#BF3 BF3, NC#BH2 BH2, NC#BG2 BG2, NC#BE2 BE2, NC#BG1 BG1, NC#BF1 BF1, NC#BD1 BD1, NC#BC1 BC1, NC#F1 F1, NC#A47 A47

MISC: DDPC_CTRLCLK N28, DDPC_CTRLDATA M28, SDVO_CTRLCLK G36, SDVO_CTRLDATA E36, CLKREQ# K36 CLKREQ#_B 4, ICH_SYNC# H36 MCH_ICH_SYNC# 18; TSATN# B12 TSATN#

HDA: HDA_BCLK B28, HDA_RST# B30, HDA_SDI B29, HDA_SDO C29, HDA_SYNC A28

CANTIGA-GM-GP-U-NF

+3.3V_RUN

R104 DY 2K21R2F-GP CFG11; R128 DY 2K21R2F-GP CFG18; R117 DY 4K02R2F-GP CFG19; R121 DY 4K02R2F-GP CFG20; RN20 4 3 1 2 PM_EXTTS#0 PM_EXTTS#1 SRN10KJ-5-GP

R383 DY 2K21R2F-GP CFG5; R112 DY 2K21R2F-GP CFG6; R111 DY 2K21R2F-GP CFG7; R102 DY 2K21R2F-GP CFG8; R382 DY 4K02R2F-GP CFG9; R375 DY 2K21R2F-GP CFG10; R101 DY 2K21R2F-GP CFG12; R105 DY 2K21R2F-GP CFG13; R103 DY 2K21R2F-GP CFG16

FSB setting: 4 MCH_CLKSEL0, 4 MCH_CLKSEL1, 4 MCH_CLKSEL2

TP86 CFG3; TP88 CFG4; CFG5 CFG6 CFG7 CFG8 CFG9 CFG10 CFG11 CFG12 CFG13 CFG14 CFG15 CFG16 CFG17 CFG18 CFG19 CFG20; TP84 TP85 TP87

18 PM_SYNC# 6,17,28 H_DPRSTP# 14 PM_EXTTS#0 15 PM_EXTTS#1

18,24,25 PM_PWROK; RSTIN#

16,20,21,24,37,41 PLT_RST# R94 1 100R2F-L1-GP-U C94 DY SC100P50V2JN-3GP

5,17,24,34 H_THRMTRIP# 18,28 DPRSLPVR

+1.8V_SUS R380 80D6R2F-L-GP; R377 80D6R2F-L-GP

+V_DDR_MCH_REF +1.8V_SUS R142 DY 10KR2J-3GP; R145 DY 10KR2J-3GP

+1.8V_SUS R122 1KR2F-3-GP; SM_RCOMP_VOH C159 SC2D2U10V3KX-1GP C162 SCD01U16V2KX-3GP R116 3K01R2F-3-GP; SM_RCOMP_VOL C145 SC2D2U10V3KX-1GP C151 SCD01U16V2KX-3GP R119 1KR2F-3-GP

+1.05V_VCCP R370 56R2J-4-GP; TSATN#

+3.3V_RUN R371 DY 10KR2J-3-GP; TSATN#_KBC TSATN#_KBC 24; Q19 DY MMBT3904WT1G-GP

+1.05V_VCCP R126 1KR2F-3-GP; R130 499R2F-2-GP; C175 SCD1U10V2KX-4GP; TP271

+3.3V_RUN R131 CLKREQ#_B 10KR2J-3-GP

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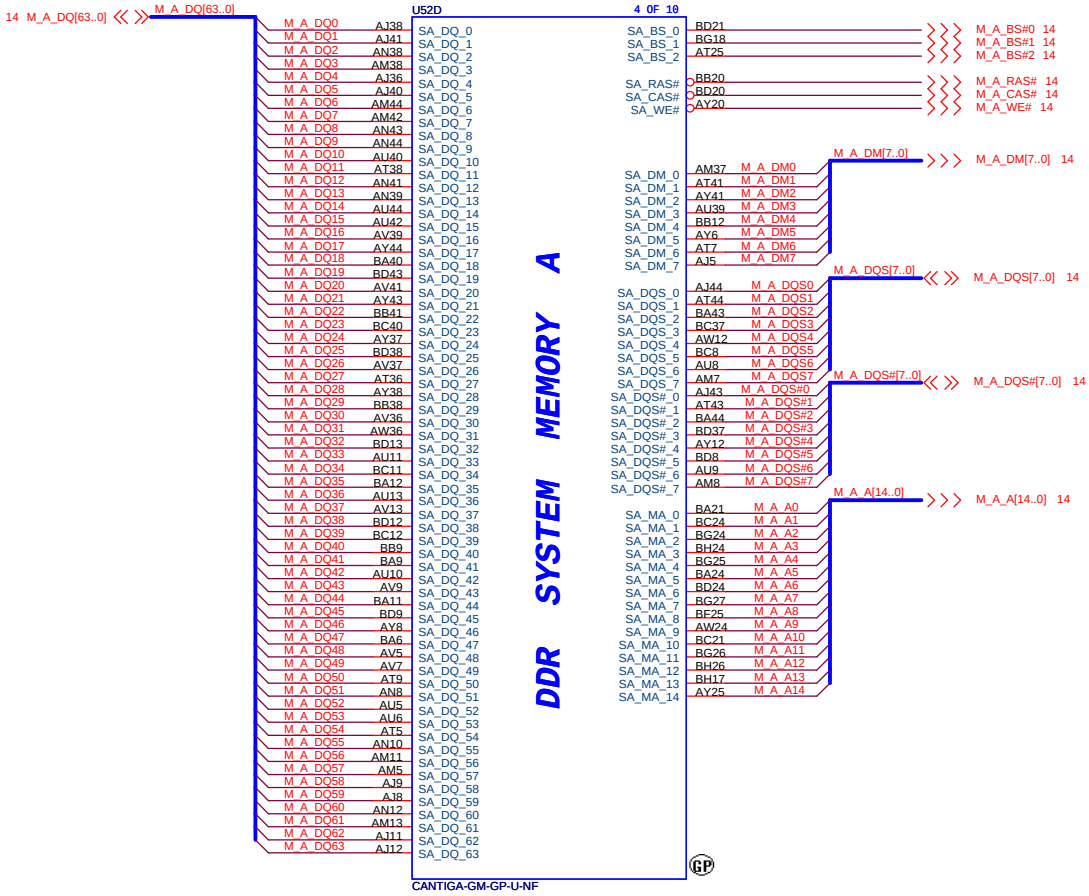
Taipei Hsien 221, Taiwan, R.O.C.

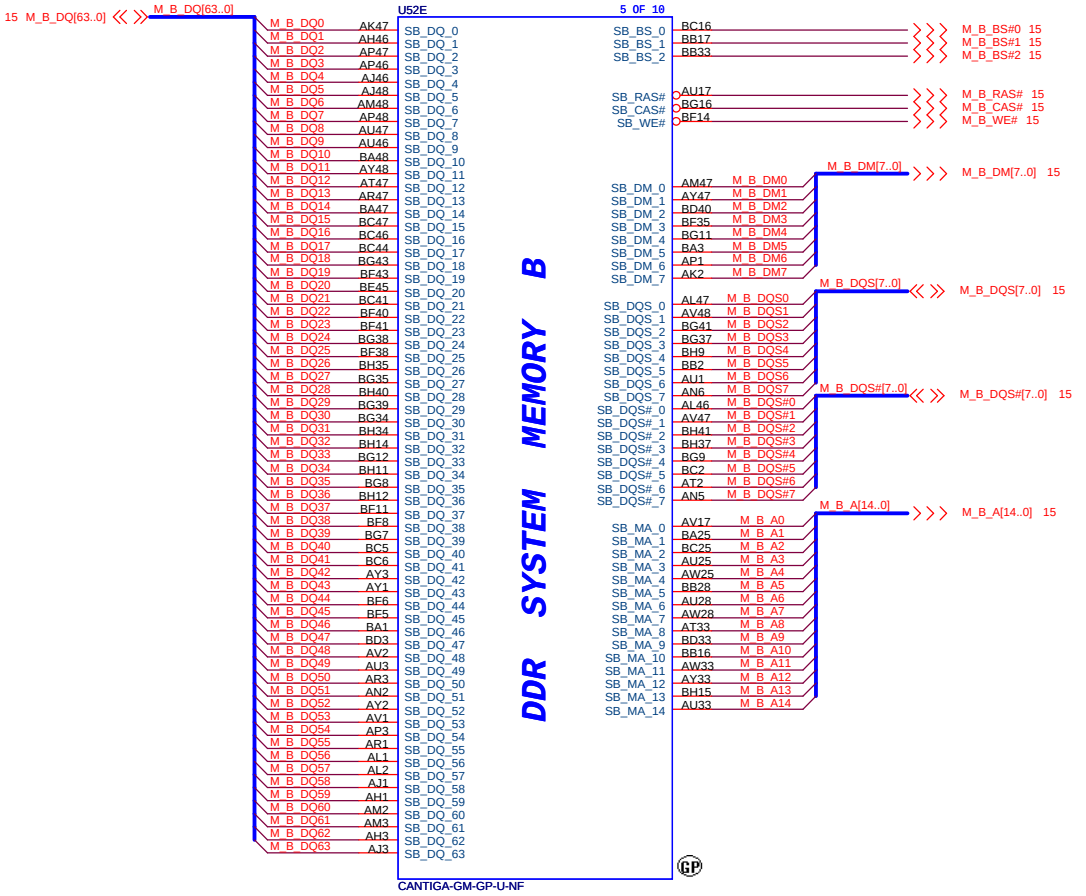
Title: Cantiga-DMI/CFG(2/6)

Size: Custom | Document Number: Roberts | Rev: A00

Date: Thursday, October 02, 2008 | Sheet 9 of 58

SSID = MCH





<Core Design>

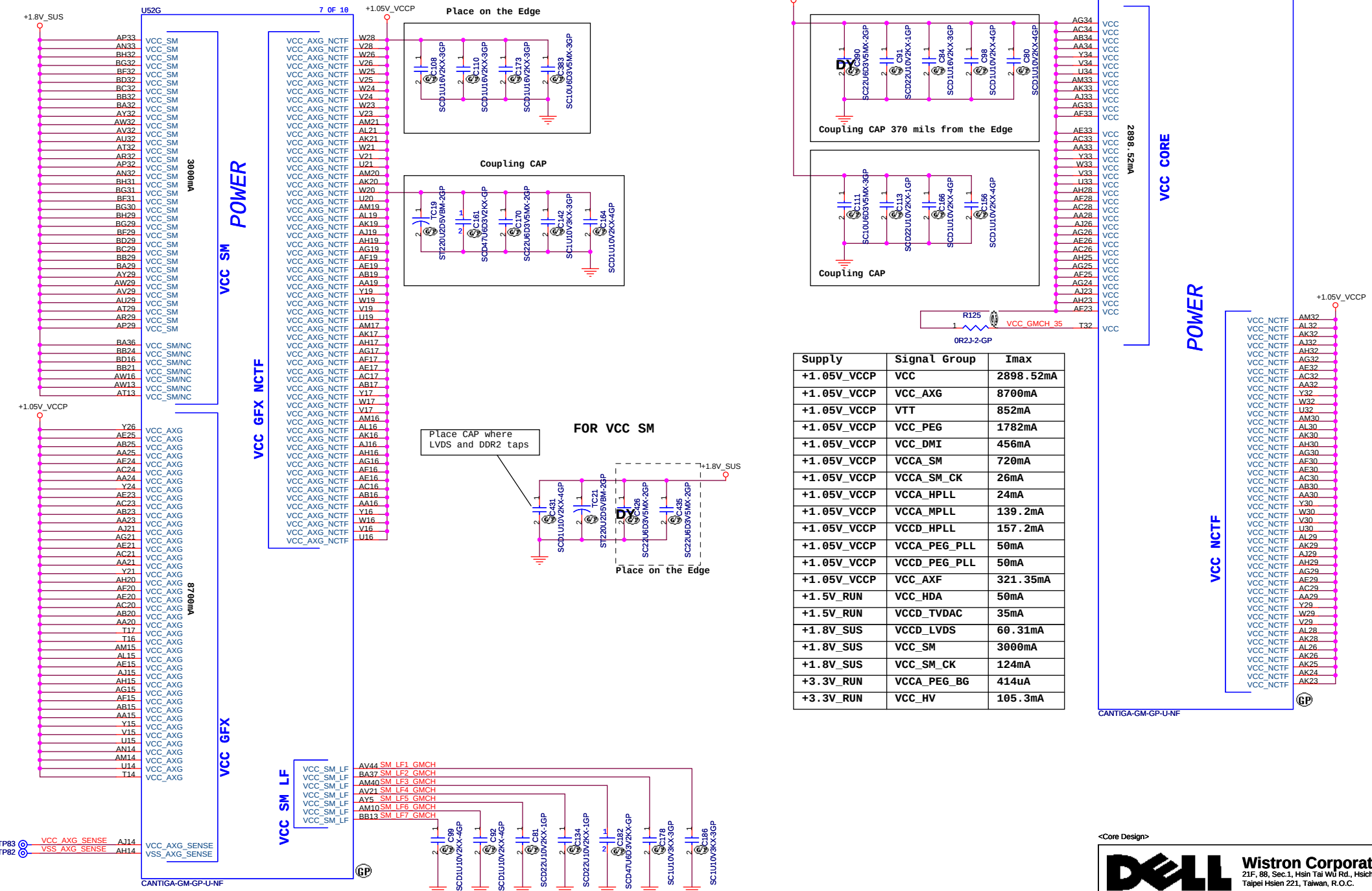
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-DDR(3/6)

Size	Document Number	Rev
Custom	Roberts	A00

Date: Thursday, October 02, 2008 Sheet 10 of 58

SSID = MCH



Supply	Signal Group	Imax
+1.05V_VCCP	VCC	2898.52mA
+1.05V_VCCP	VCC_AXG	8700mA
+1.05V_VCCP	VTT	852mA
+1.05V_VCCP	VCC_PEG	1782mA
+1.05V_VCCP	VCC_DMI	456mA
+1.05V_VCCP	VCCA_SM	720mA
+1.05V_VCCP	VCCA_SM_CK	26mA
+1.05V_VCCP	VCCA_HPLL	24mA
+1.05V_VCCP	VCCA_MPLL	139.2mA
+1.05V_VCCP	VCCD_HPLL	157.2mA
+1.05V_VCCP	VCCA_PEG_PLL	50mA
+1.05V_VCCP	VCCD_PEG_PLL	50mA
+1.05V_VCCP	VCC_AXF	321.35mA
+1.5V_RUN	VCC_HDA	50mA
+1.5V_RUN	VCCD_TVDAC	35mA
+1.8V_SUS	VCCD_LVDS	60.31mA
+1.8V_SUS	VCC_SM	3000mA
+1.8V_SUS	VCC_SM_CK	124mA
+3.3V_RUN	VCCA_PEG_BG	414uA
+3.3V_RUN	VCC_HV	105.3mA

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-Power(4/6)

Size: Custom | Document Number: Roberts | Rev: A00

Date: Thursday, September 11, 2008 | Sheet 11 of 58

SSID = MCH

POWER

Cantiga-Power/Filter(5/6)

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<Core Design>

Size: Custom	Document Number: Roberts	Rev: A00	
Date: Thursday, September 11, 2008	Sheet 12 of 58		

Reserved for TV ripple

Main source: 74.09091.H3F
2nd source: 74.09198.07F

SSID = MCH

U52I 9 OF 10

U52J 10 OF 10

CANTIGA-GM-GP-U-NF

VSS NCTF

VSS SCB

NC

NCTF PIN

U52C 3 OF 10

CANTIGA-GM-GP-U-NF

LVDS

PCI-EXPRESS GRAPHICS

VGA

CRT_IREF routing Trace width use 20 mil.

Place R105 close to MCH within 500 mils.

5V @ ext. CRT side

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-GND/LVDS/VGA(6/6)

Size: Custom | Document Number: Roberts | Rev: A00

Date: Thursday, October 02, 2008 | Sheet 13 of 58

SSID = MEMORY

DM2

10 M_A_DQS#[7..0]
10 M_A_DQ[63..0]
10 M_A_DM[7..0]
10 M_A_DQS[7..0]
10 M_A_A[14..0]

M_A_A0 102 … M_A_A14 86
M_A_BS#2 85
M_A_BS#0 107
M_A_BS#1 106
M_A_DQ0 5 … M_A_DQ63 194
M_A_DQS#0 11 … M_A_DQS#7 186
M_A_DQS0 13 … M_A_DQS7 188
M_ODT0 114
M_ODT1 119
VREF 1
VSS 2
GND 202
MH1

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16/BA2
BA0 BA1
DQ0 … DQ63
DQS0# DQS1# DQS2# DQS3# DQS4# DQS5# DQS6# DQS7#
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7
OTD0 OTD1
VREF VSS GND MH1

RAS# 108 → M_A_RAS# 10
WE# 109 → M_A_WE# 10
CAS# 113 → M_A_CAS# 10
CS0# 110 → M_CS0# 9
CS1# 115 → M_CS1# 9
CKE0 79 → M_CKE0 9
CKE1 80 → M_CKE1 9
CK0 30 → M_CLK_DDR0 9
CK0# 32 → M_CLK_DDR#0 9
CK1 164 → M_CLK_DDR1 9
CK1# 166 → M_CLK_DDR#1 9
DM0 10 → M_A_DM0
DM1 26 → M_A_DM1
DM2 52 → M_A_DM2
DM3 67 → M_A_DM3
DM4 130 → M_A_DM4
DM5 147 → M_A_DM5
DM6 170 → M_A_DM6
DM7 185 → M_A_DM7
SDA 195 → ICH_SMBDATA 4,15,18
SCL 197 → ICH_SMBCLK 4,15,18
VDDSPD 199 → +3.3V_RUN
SA0 198 → R55 10KR2J-3-GP
SA1 200 → R56 10KR2J-3-GP
NC#50 50 → PM_EXTTS#0 9
NC#69 69
NC#83 83
NC#120 120
NC#163/TEST 163

VDD 81 82 87 88 95 96 103 104 111 112 117 118
VSS 3 8 9 12 15 18 21 24 27 28 33 34 39 40 41 42 47 48 53 54 59 60 65 66 71 72 77 78 121 122 127 128 132 133 138 139 144 145 149 150 155 156 161 162 165 168 171 172 177 178 183 184 187 190 193 196
GND 201
MH2

SKT-SODIMM200-37GP
62.10017.F21

+1.8V_SUS

+3.3V_RUN

+0.9V_DDR_VTT

+V_DDR_MCH_REF

9 M_ODT0
9 M_ODT1

C203 SCD1U16V2KX-3GP
C202 SC2D2U10V3KX-1GP

put near connector

M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1

C72 C74 C92 C195 DUMMY-C2

Layout Note:
Place near DM1

+1.8V_SUS

C132 C122 C60 C138 C116 C93 C109 C100 C106 C8
SC2D2U10V3KX-1GP SC2D2U10V3KX-1GP SC2D2U10V3KX-1GP SC2D2U10V3KX-1GP SC2D2U10V3KX-1GP SCD1U16V2KX-3GP SCD1U16V2KX-3GP SCD1U16V2KX-3GP SCD1U16V2KX-3GP ST220U2D5VBM-LGP

Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT.

+0.9V_DDR_VTT

C101 C409 C103 C96 C83 C432 C87 C114 C118 C119 C115 C428 C420
SCD1U16V2KX-3GP

+3.3V_RUN

C54 SCD1U16V2KX-3GP
C53 SC2D2U10V3KX-1GP

Layout Note:
Place these resistors close to DM1,
all trace length Max=1.5".

+0.9V_DDR_VTT

RN37 SRN56J-4-GP: M_A_A9, M_A_A12
RN6 SRN56J-4-GP: M_A_A13
RN31 SRN56J-4-GP: M_A_A10, M_A_BS#0
RN35 SRN56J-4-GP: M_A_A5, M_A_A8
RN4 SRN56J-4-GP: M_ODT0, M_CS0#
RN10 SRN56J-4-GP: M_A_A6, M_A_A2
RN12 SRN56J-4-GP: M_CKE1, M_A_A14
RN33 SRN56J-4-GP: M_A_A1, M_A_A3
RN29 SRN56J-4-GP: M_A_WE#, M_A_CAS#
RN39 SRN56J-4-GP: M_CKE0, M_A_BS#2
RN28 SRN56J-4-GP: M_CS1#, M_ODT1
RN8 SRN56J-4-GP: M_A_BS#1, M_A_RAS#
RN11 SRN56J-4-GP: M_A_A11, M_A_A7
RN17 SRN56J-4-GP: M_A_A0, M_A_A4

<Core Design>

Wistron Corporation
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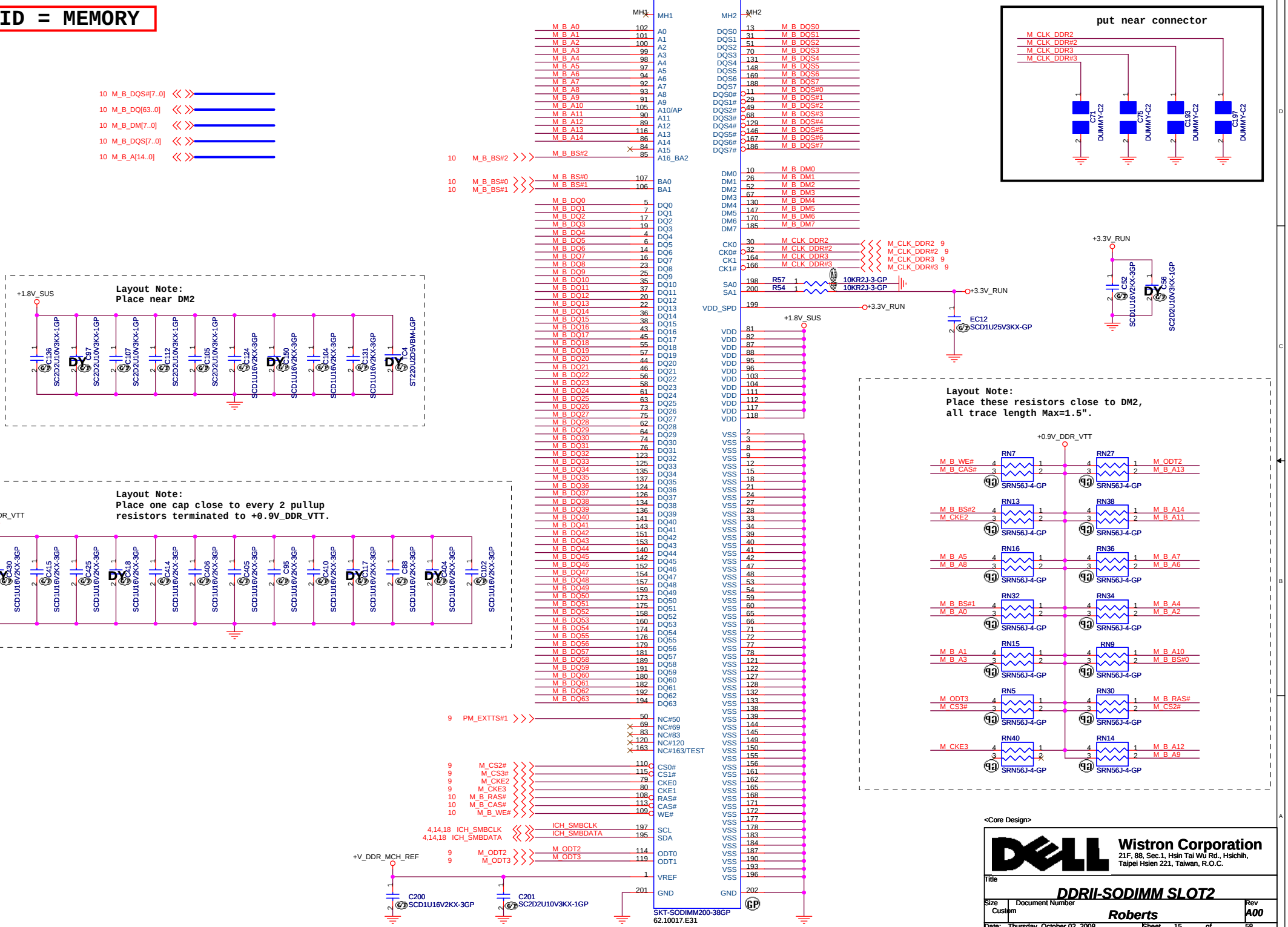
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRII-SODIMM SLOT1
Size: Custom
Document Number: Roberts
Rev: A00
Date: Thursday, October 02, 2008
Sheet 14 of 58

SSID = MEMORY



<Core Design>

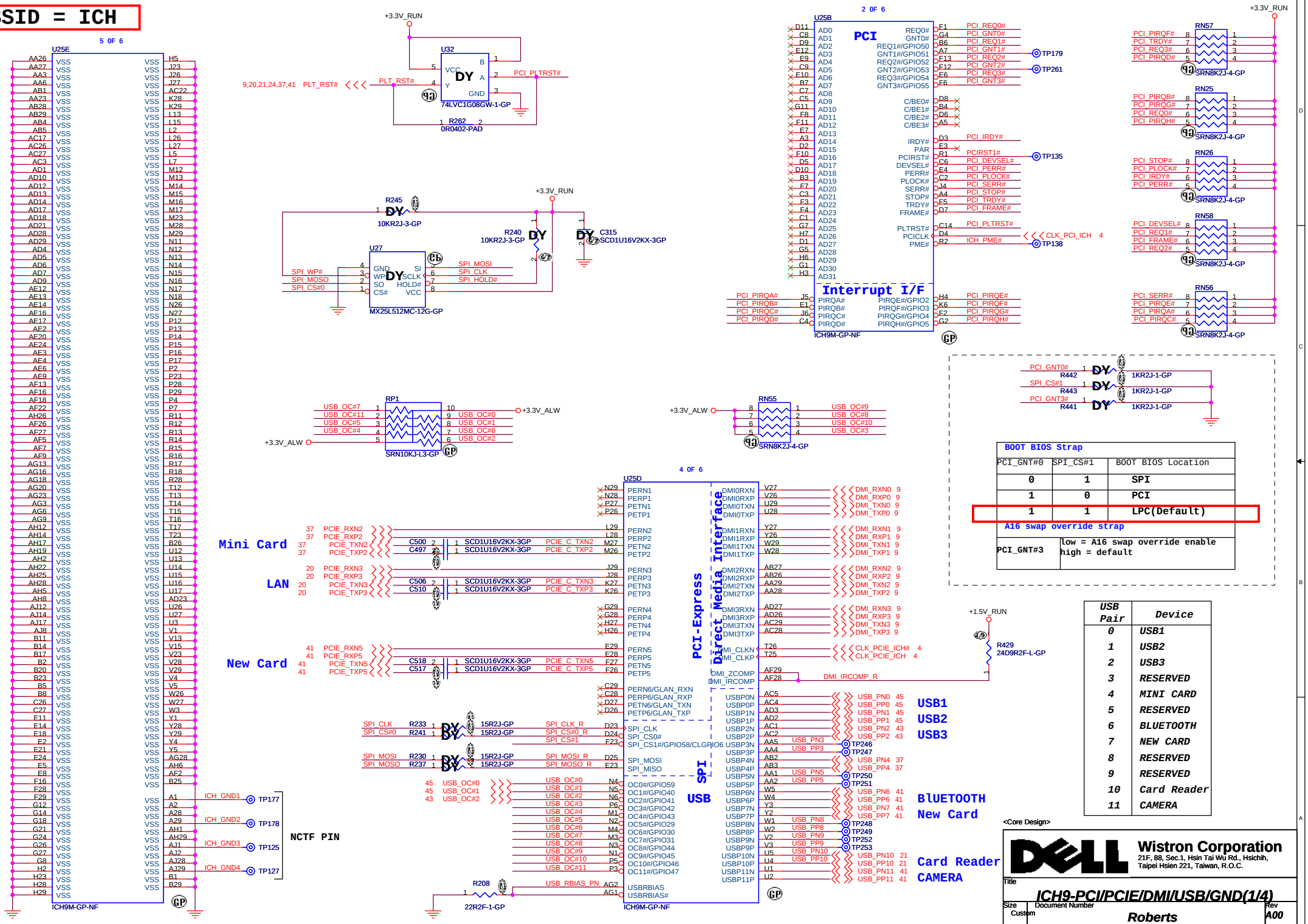
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRII-SODIMM SLOT2

Size	Document Number	Rev
Custom	Roberts	A00

Date: Thursday, October 02, 2008 Sheet 15 of 58

SSID = ICH



<Core Design>

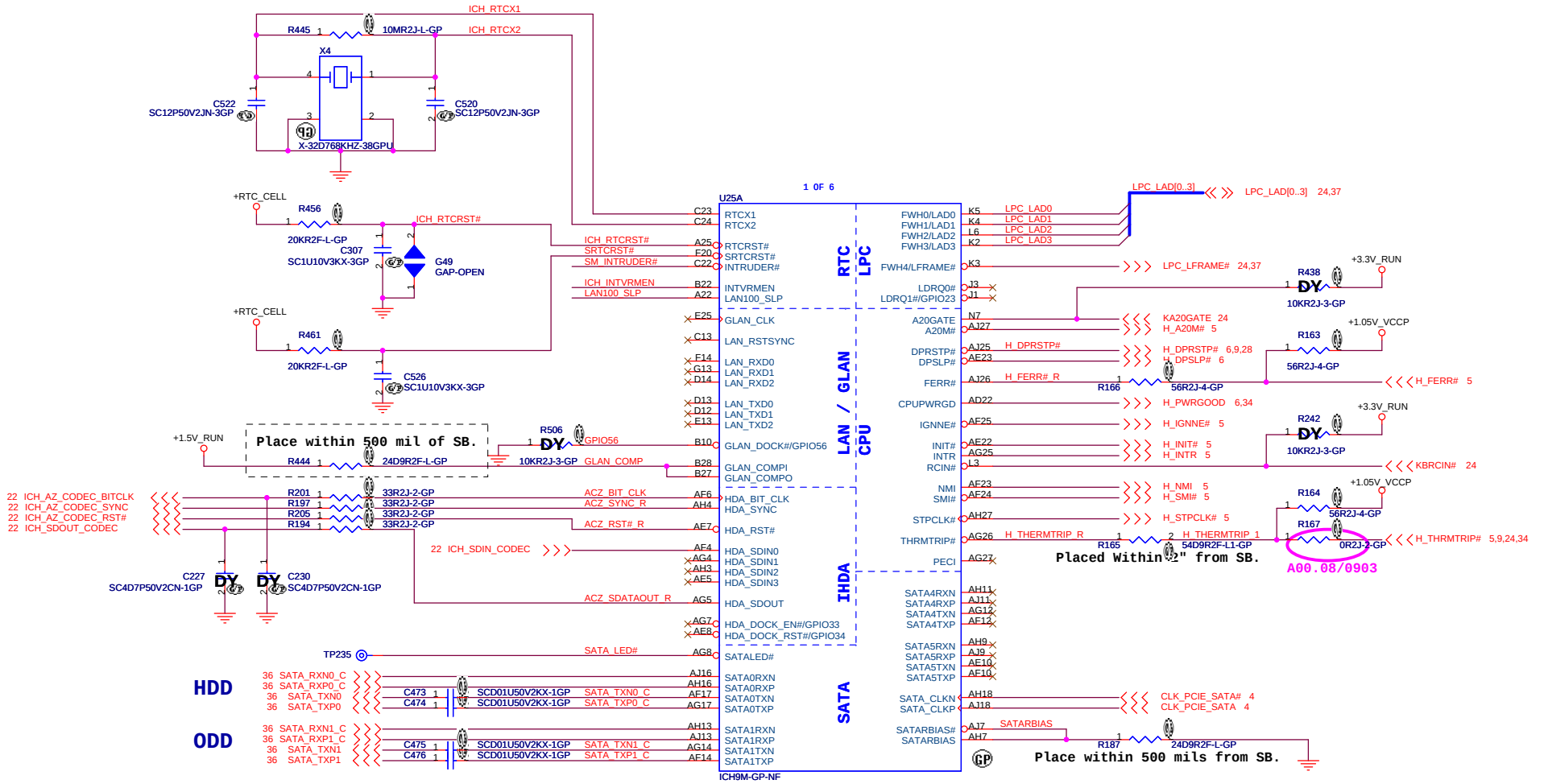
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

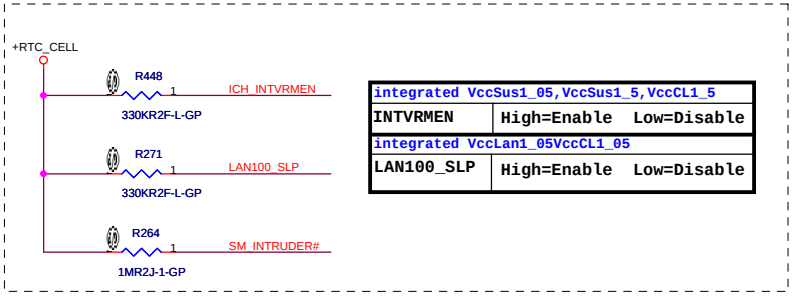
Title: ICH9-PCI/PCIE/DMI/USB/GND(1/4)

Size: Custom | Document Number: Roberts | Rev: A00

Date: Thursday, October 02, 2008 | Sheet 16 of 58

SSID = ICH





integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

<Core Design>

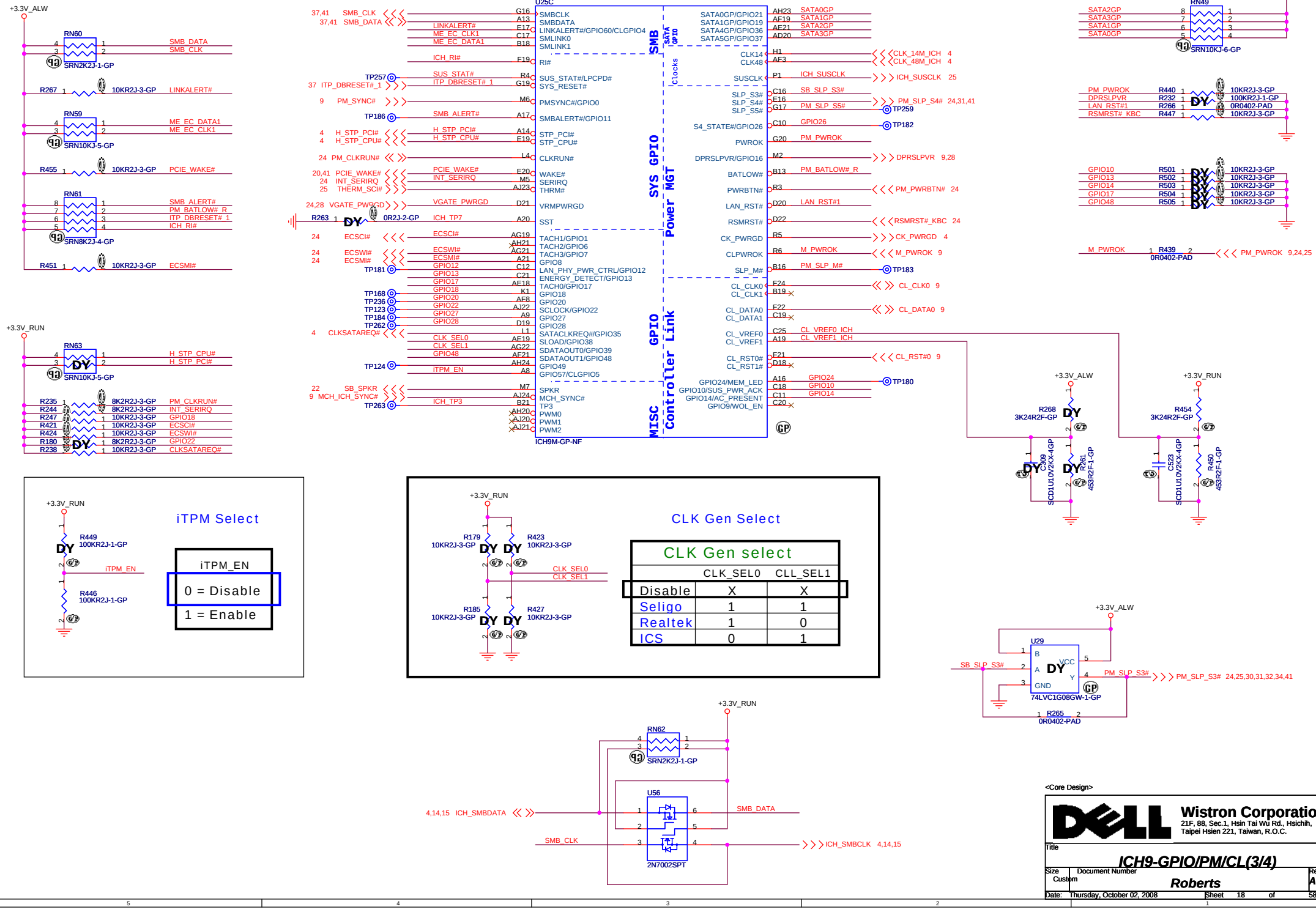
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-LAN/HDA/SATA/LPC(2/4)

Size	Document Number	Rev
Custom	Roberts	A00

Date: Thursday, October 02, 2008 Sheet 17 of 58

SSID = ICH



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-GPIO/PM/CL(3/4)

Size: Custom | Document Number: Roberts | Rev: A00

Date: Thursday, October 02, 2008 | Sheet 18 of 58

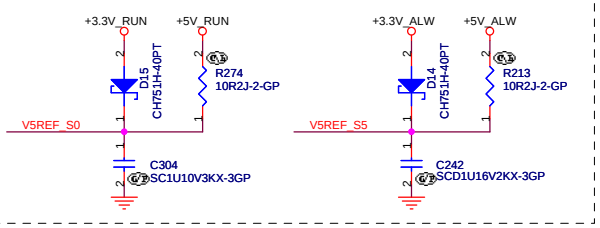
SSID = ICH

6 OF 6

U25F

ICH9M-GP-NF

*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail



+RTC_CELL

V5REF_S0

V5REF_S5

+1.05V_VCCP

+1.5V_RUN

+3.3V_RUN

+3.3V_ALW

+VCCSATAPLL

1D5V_DMIPLL_ICH_S0

VCCDMI

SB_V_CPU_IO

SB_VCC_3_3_C

3D3V_VCCPCORE_ICH_S0

PCI_VCCP_CORE_S0

SB_VCCHDA

SB_VCCSUS3_3

VCCSUS1_05[3]

VCCSUS1_5[3]

SB_VCCCL3_3

VCC_GLAN_PLL

1D5V_USB_S0

VCCLAN1D05

SB_VCCLAN3_3

3D3V_GLAN_S0

A00.08/0909

<Core Design>

Wistron Corporation
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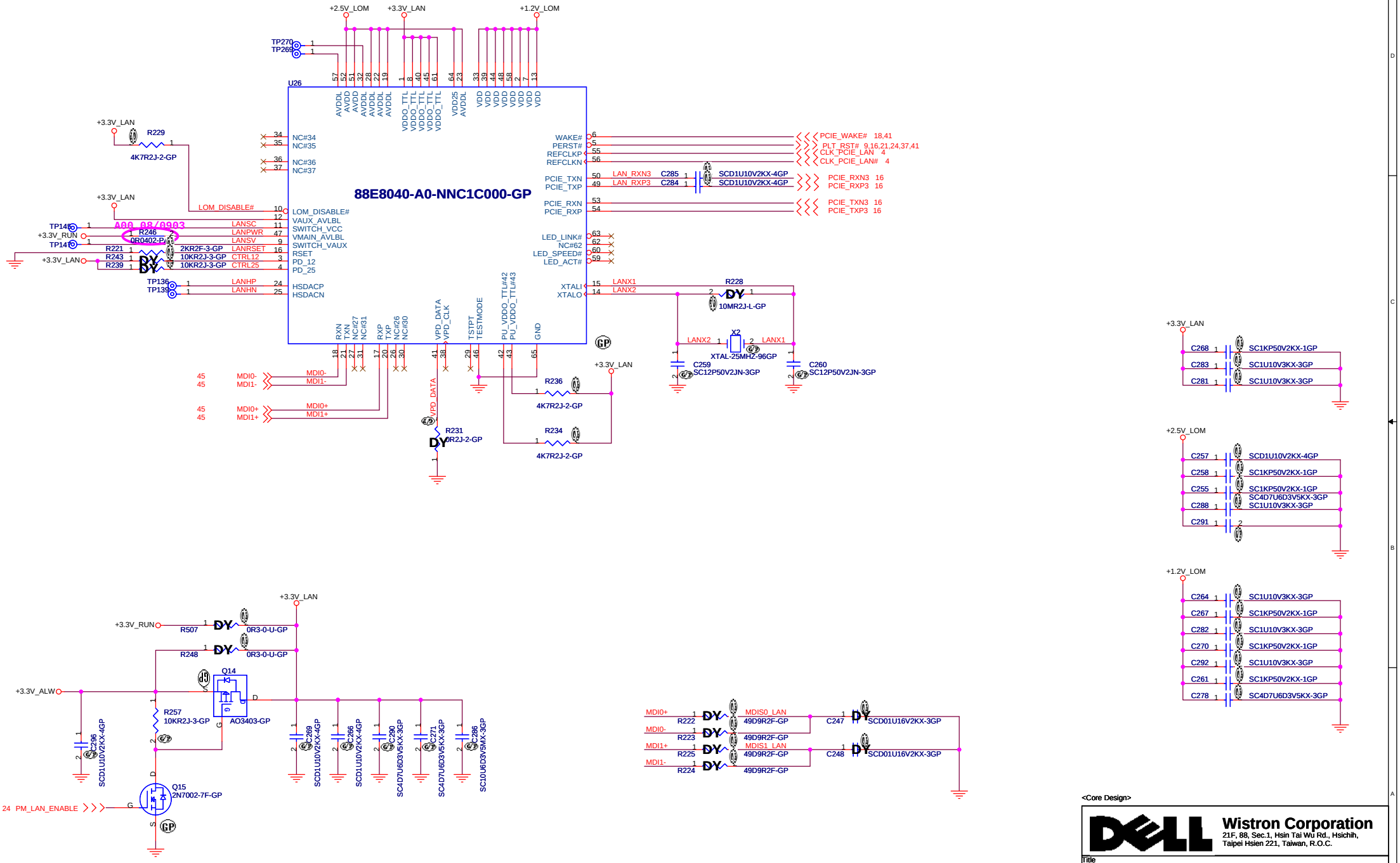
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-POWER(4/4)

Size: Custom | Document Number: Roberts | Rev: A00

Date: Thursday, September 11, 2008 | Sheet 19 of 58

SSID = LOM



<Core Design>

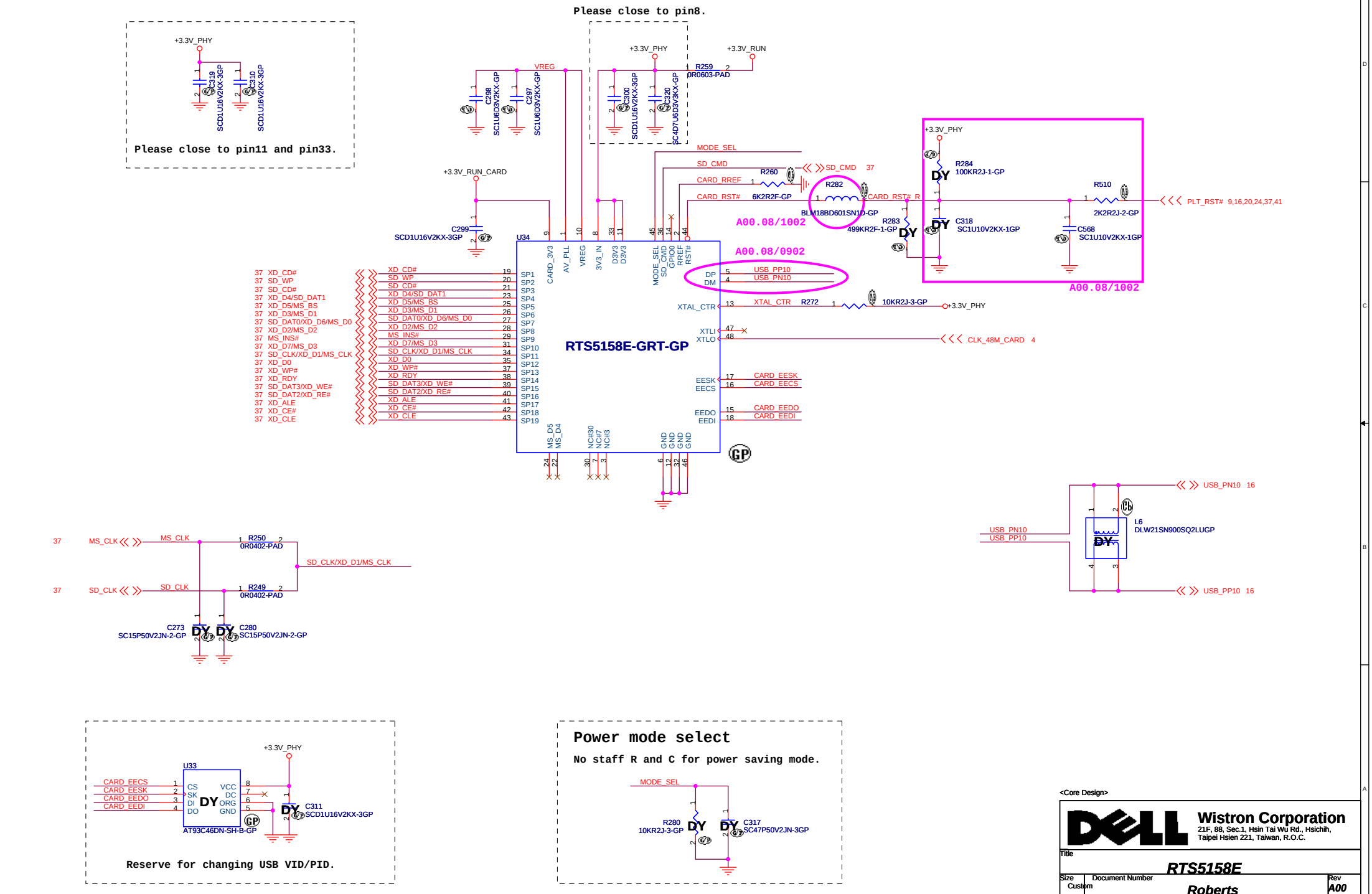
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN Marvell-88E8040

Size	Document Number	Rev
Custom	Roberts	A00

Date: Thursday, October 02, 2008 Sheet 20 of 58

SSID = SDIO

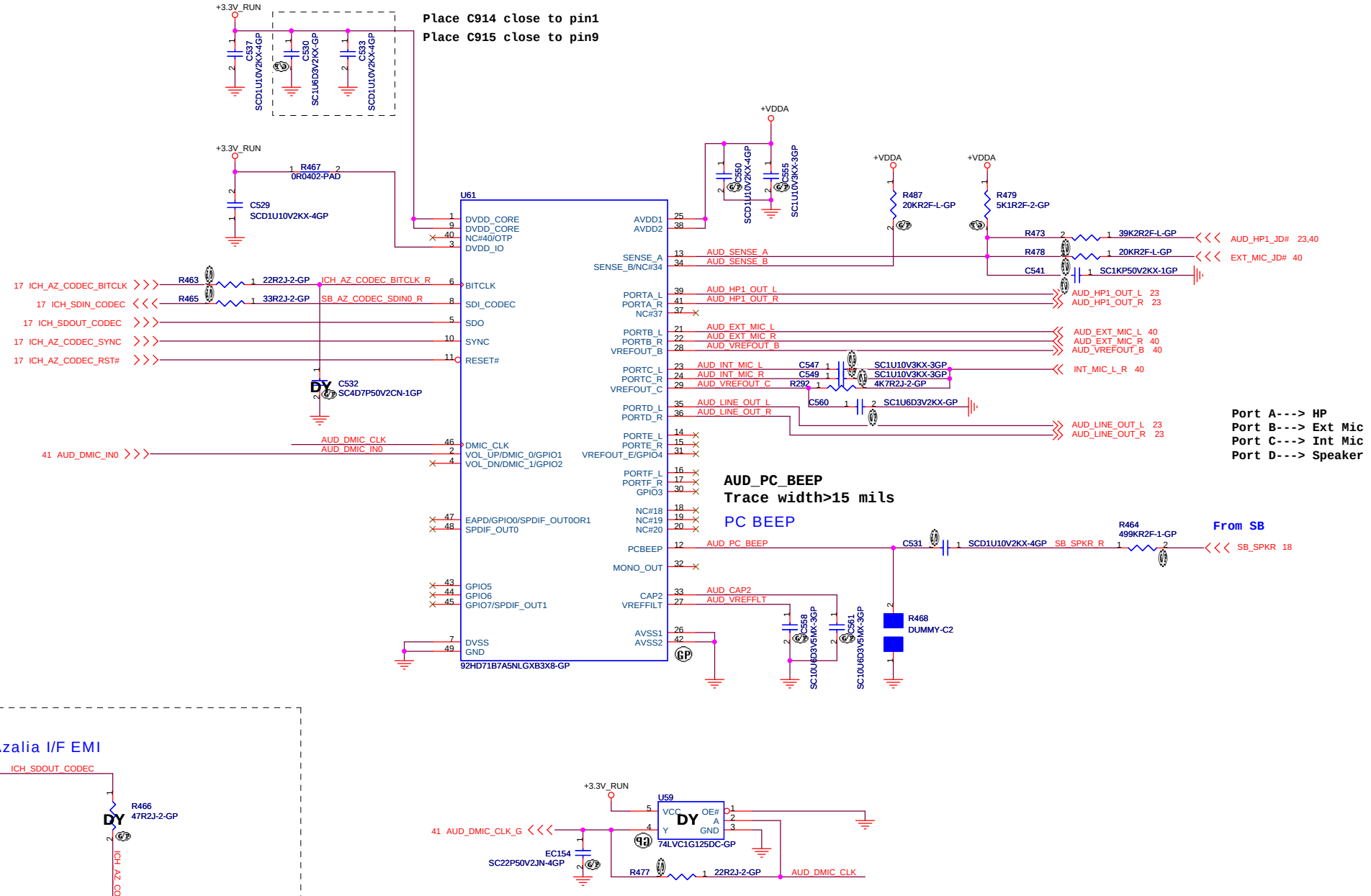


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RTS5158E	
Size: Custom	Document Number: Roberts	Rev: A00
Date: Thursday, October 02, 2008	Sheet 21 of 58	

SSID = AUDIO



<Core Design>

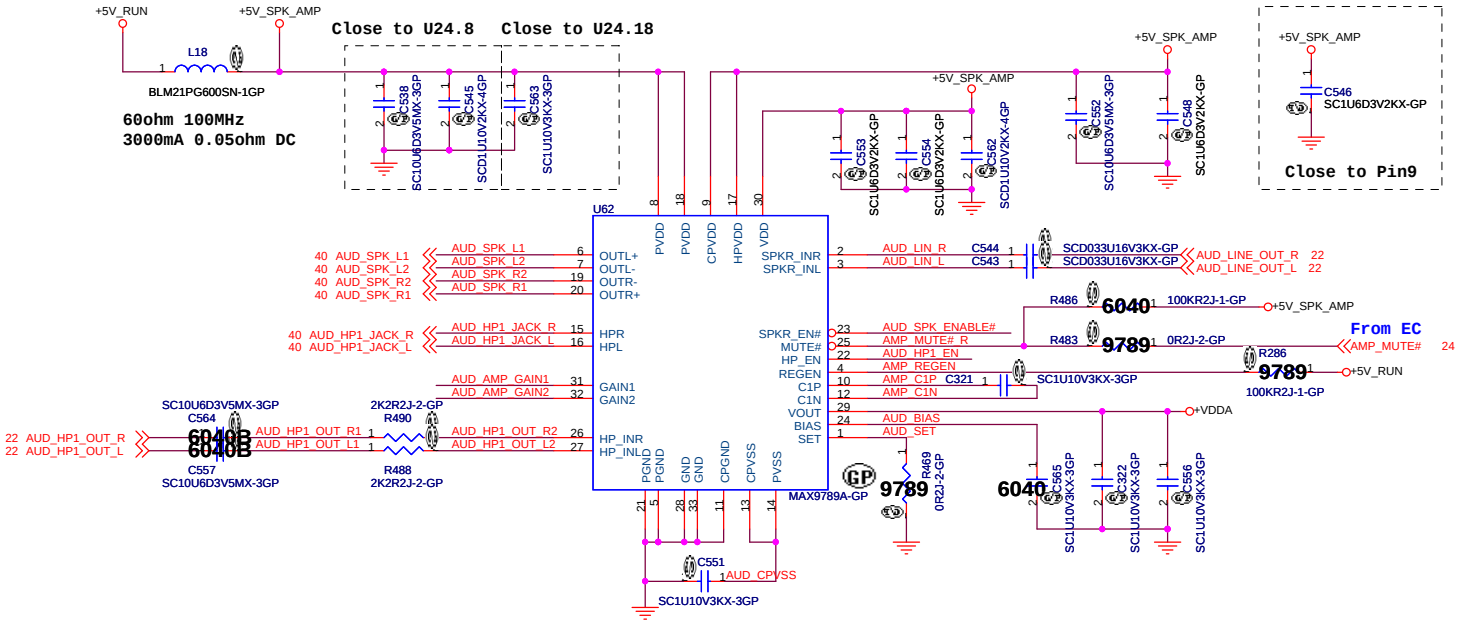
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

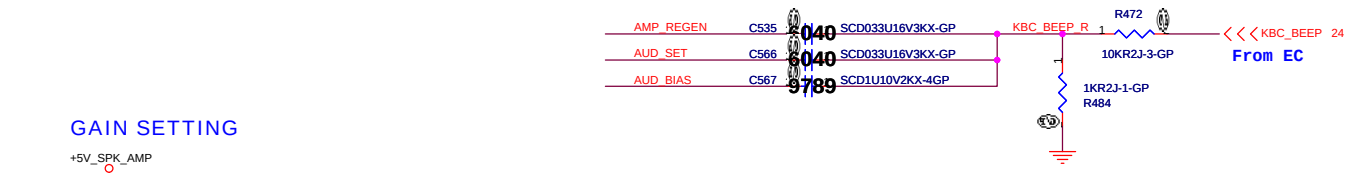
Title: AUDIO CODEC 92HD71B7

Size: Custom | Document Number: Roberts | Rev: A00

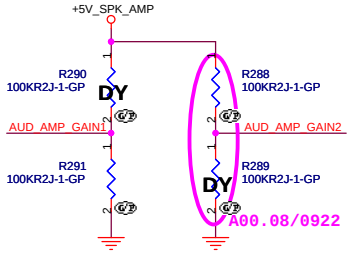
Date: Thursday, October 02, 2008 | Sheet 22 of 58

SSID = AUDIO



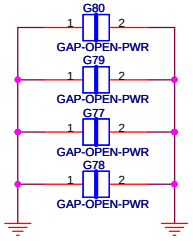


GAIN SETTING

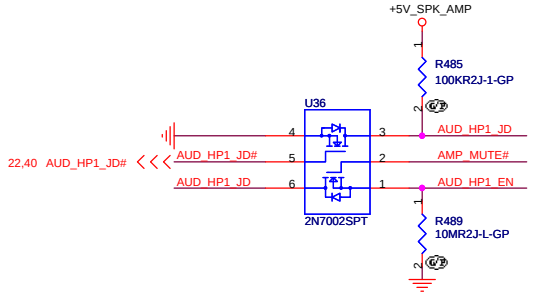


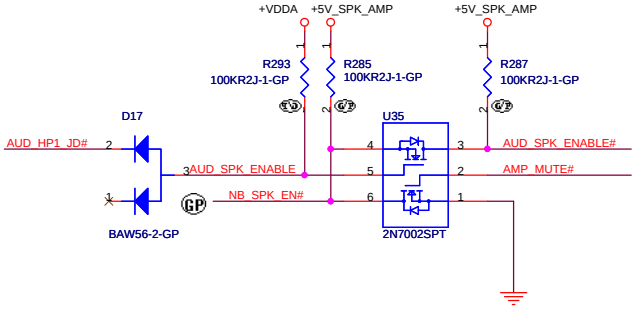
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

	Main source	Second source
	TPA6040A (74.06040.013)	MAX9789A (74.09789.013)
R486	100K	No ASM
R483	No ASM	0 Ohm
R469	No ASM	0 Ohm
R286	No ASM	100K
C535	0.033uF	No ASM
C566	0.033uF	No ASM
C565	1uF	No ASM
C567	No ASM	0.1uF
C564	10uF	2.2uF
C557	10uF	2.2uF



Signal inverter for speaker shutdown





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP/SPEAKER

Size: Custom | Document Number: Roberts | Rev: A00

Date: Thursday, October 02, 2008 | Sheet 23 of 58

CAP close to VCC-GND pin pair

SSID = KBC

MB VERSION ID

MB VERSION ID	VER2	VER1	VER0
X00	0	0	0
X01	0	0	1
X02	0	1	0
-1	0	1	1

KBC CLK EMI

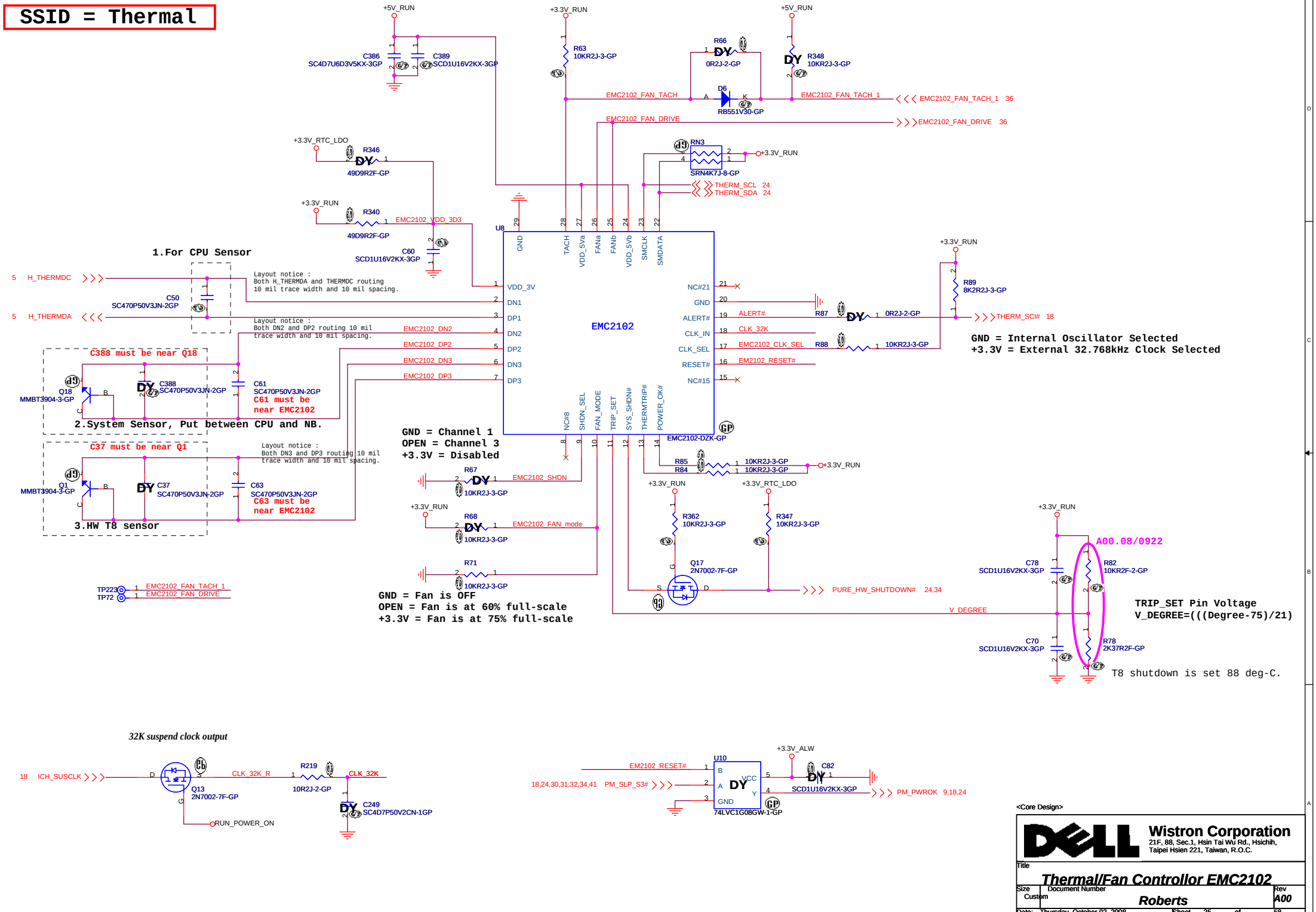
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Winbond WPC773L

Size: Custom | Document Number: Roberts | Rev: A00

Date: Thursday, October 02, 2008 | Sheet 24 of 58

SSID = Thermal



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

Size	Document Number	Rev
Custom	Roberts	A00

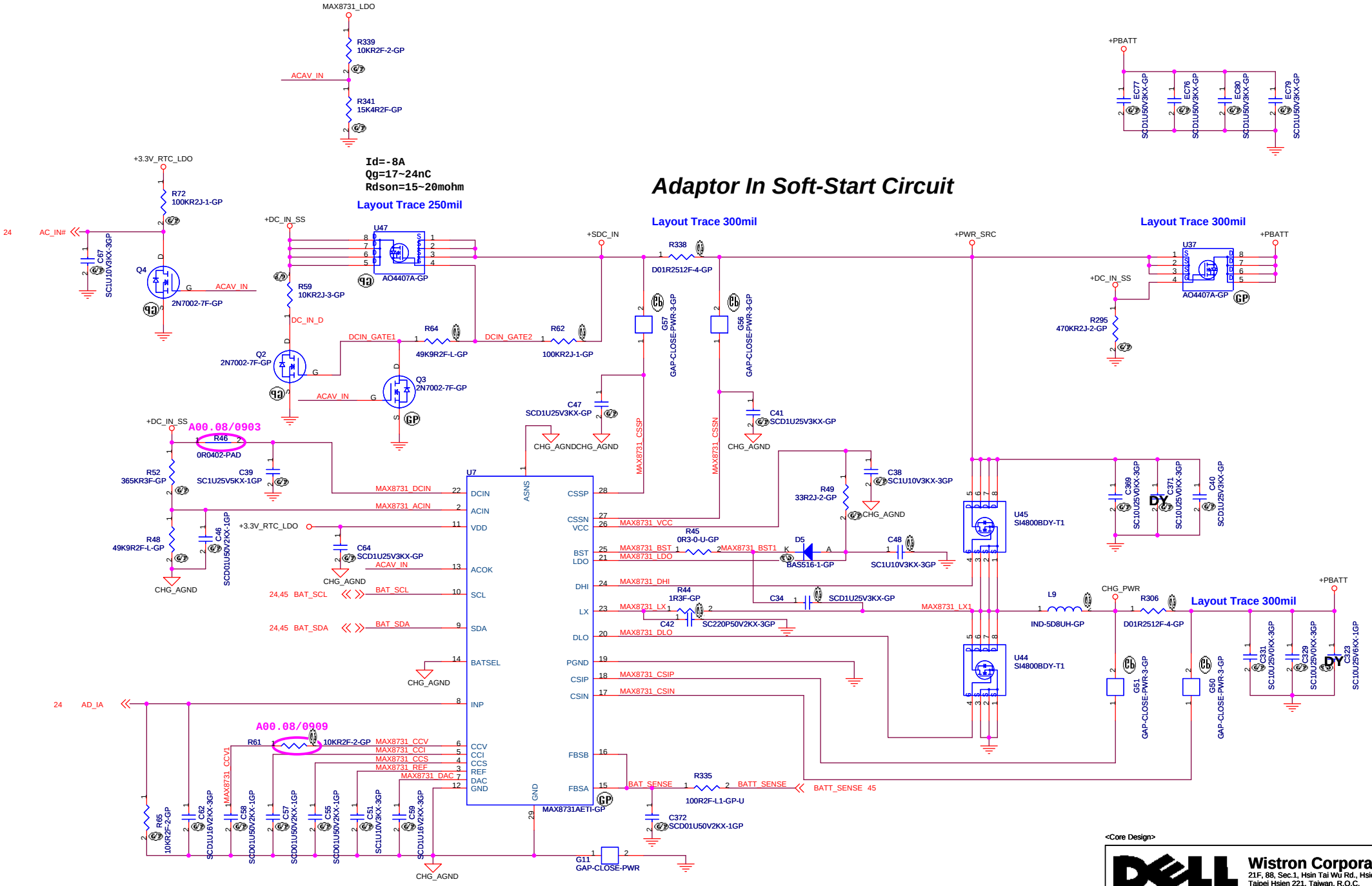
Date: Thursday, October 02, 2008 Sheet 25 of 58

SSID = Charger

Adaptor In Soft-Start Circuit

Id=-8A
Qg=17~24nC
Rdson=15~20mohm

Layout Trace 250mil
Layout Trace 300mil
Layout Trace 300mil
Layout Trace 300mil



<Core Design>

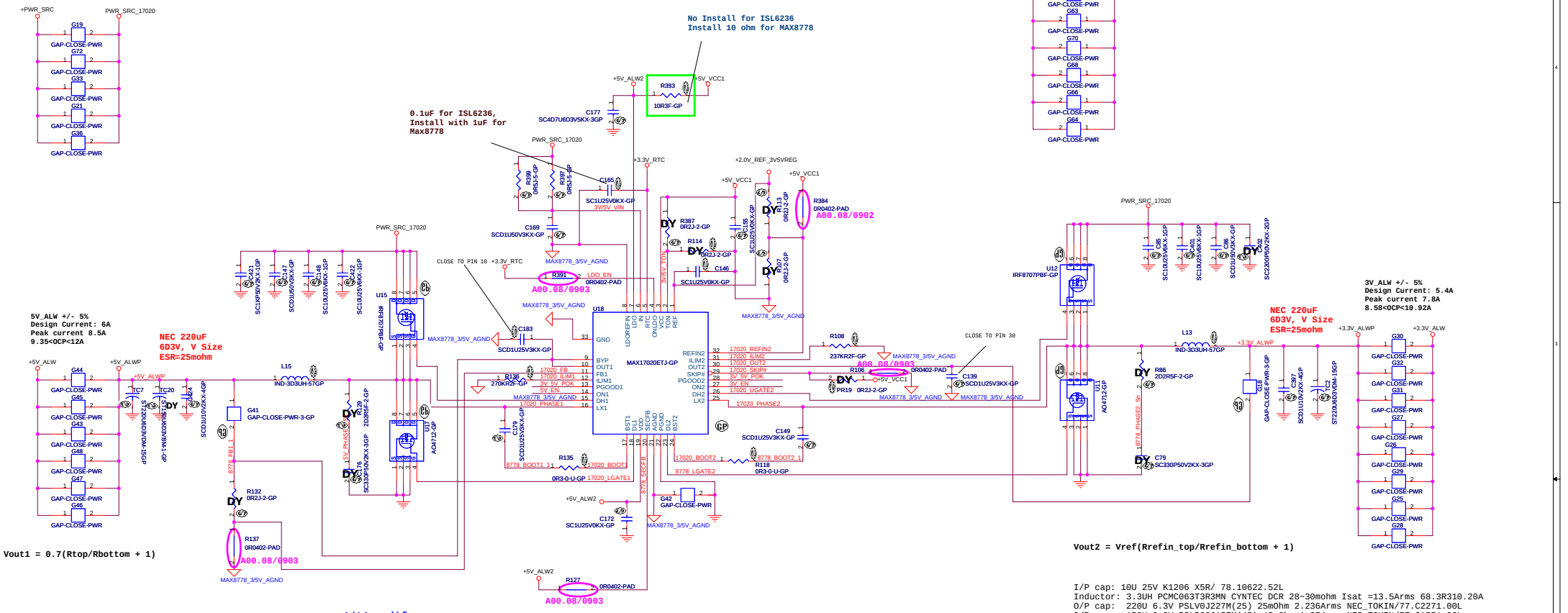
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER MAX8731

Size	Document Number	Rev
Custom	Roberts	A00

Date: Thursday, October 02, 2008 Sheet 26 of 58

SSID = PWR.Plane.Regulator_3p3v5v



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMC063T3R3MN CYNTEC DCR 28~30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 150U 6.3V PSLB20J157M(45) 45mOhm 1.374rms NEC_TOKIN/77.C1571.09L
H/S: IRF8707 SO-8/ 14.2mohm/17.5mOhm@4.5Vgs/ 84.08707.037
L/S: FDS4712 SO-8/ 15mohm/18mOhm@4.5Vgs/ 84.04712.037

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMC063T3R3MN CYNTEC DCR 28~30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 150U 6.3V PSLB20J157M(45) 45mOhm 1.374rms NEC_TOKIN/77.C1571.09L
H/S: IRF8707 SO-8/ 14.2mohm/17.5mOhm@4.5Vgs/ 84.08707.037
L/S: FDS4712 SO-8/ 15mohm/18mOhm@4.5Vgs/ 84.04712.037

SKIPSEL	GND	Open/REF (2V)	High (VCC or 3.3V)
Operating Mode	pulse-skipping mode	ultrasonic mode	forced-PWM operation

TONSEL	GND	Open (REF)	High (VCC)
CH1 Freq	400kHz	400kHz	200kHz
CH2 Freq	500kHz	300kHz	300kHz

LDOREFIN	GND	VCC	VLDOREFIN = 0.5V
Operating Mode	4.90/5.0/5.10	3.23/3.3/3.37	0.96/1.0/1.04

FB1	GND	VCC	
Operating Mode	4.925/5.00/5.075	1.482/1.50/1.518	

REFIN2	5V	RTC (3.3V)	
Operating Mode	3.255/3.30/3.345	1.038/1.050 /1.062	

<Core Design>

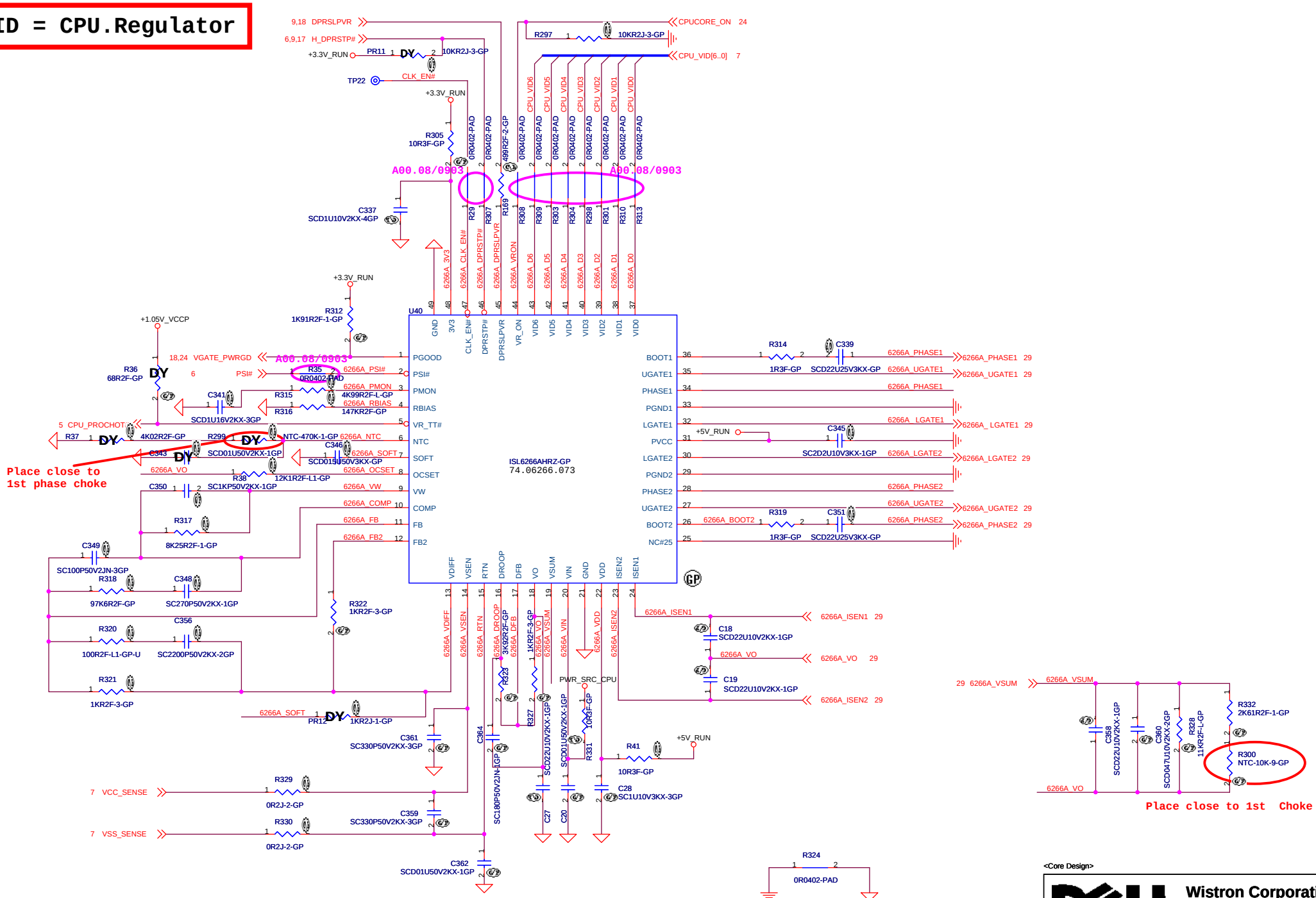
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 3.3V/5V

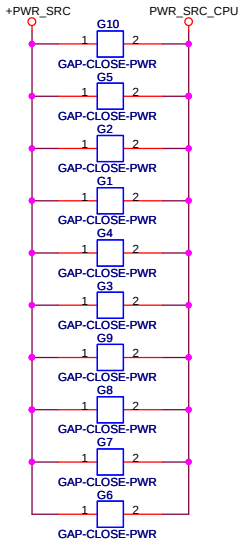
Size	Document Number	Rev
A2	Roberts	A00

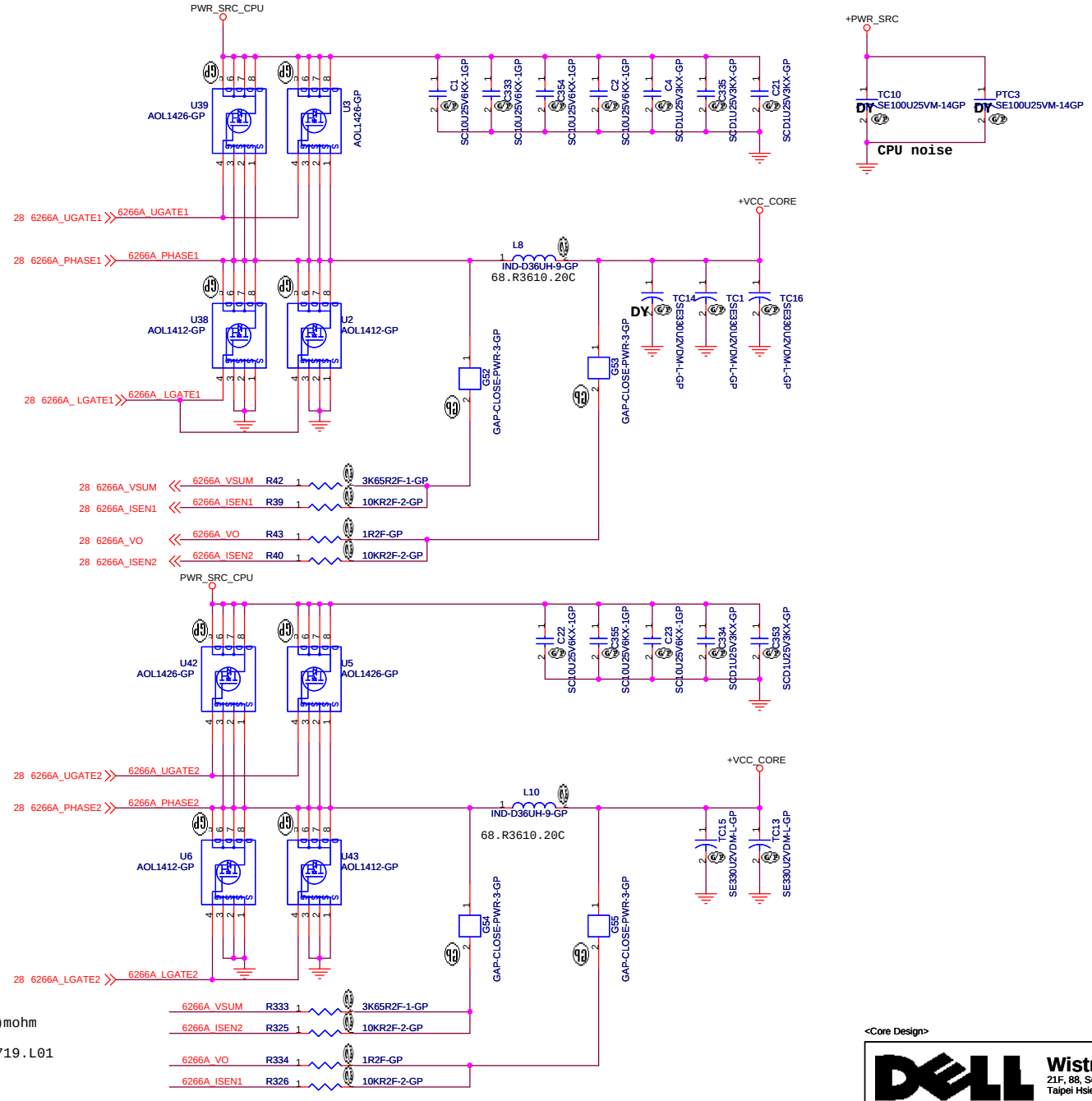
Date: Thursday, October 02, 2008 Sheet 27 of 58

SSID = CPU.Regulator



SSID = CPU.Regulator





I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH PCMC104T-R36MN1R05J CYNTEC DCR 1.05(+5%~-5%)mohm
Isat =60Arms 68.R3610.20C
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S: AOL1426 PowerPAK/ 10.2mohm/12.5mOhm@4.5Vgs/84.01426.037
L/S: AOL1412 PowerPAK/ 3.8mohm/4.65mOhm@4.5Vgs/ 84.01412.037

<Core Design>

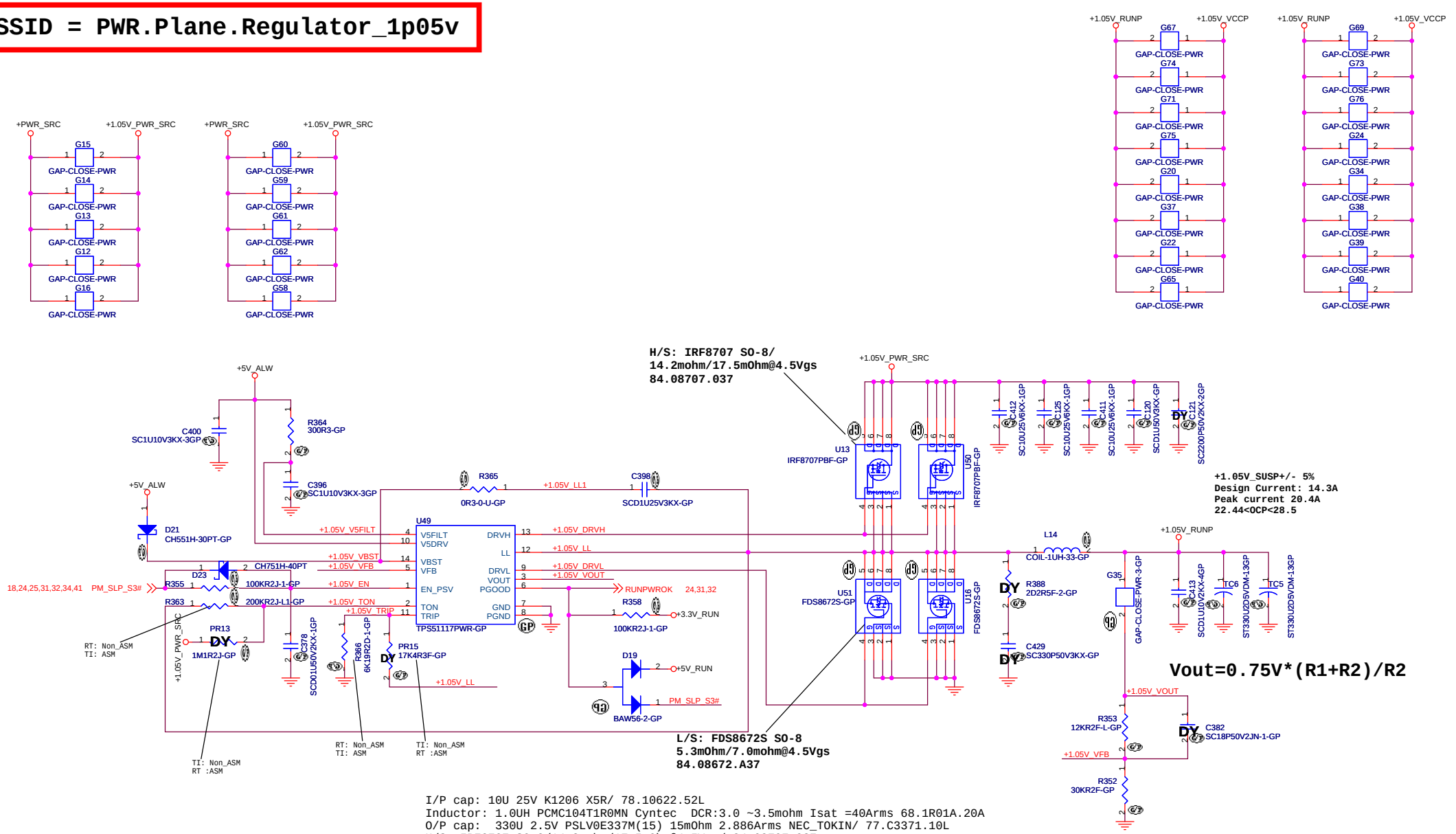
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU VCORE POWER(2/2)

Size	Document Number	Rev
Custom	Roberts	A00

Date: Thursday, October 02, 2008 Sheet 29 of 58

SSID = PWR.Plane.Regulator_1p05v



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.0UH PCMC104T1R0MN Cyntec DCR:3.0 ~3.5mohm Isat =40Arms 68.1R01A.20A
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: IRF8707 SO-8/14.2mohm/17.5mOhm@4.5Vgs/ 84.08707.037
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A37
Switching freq-->350KHz

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

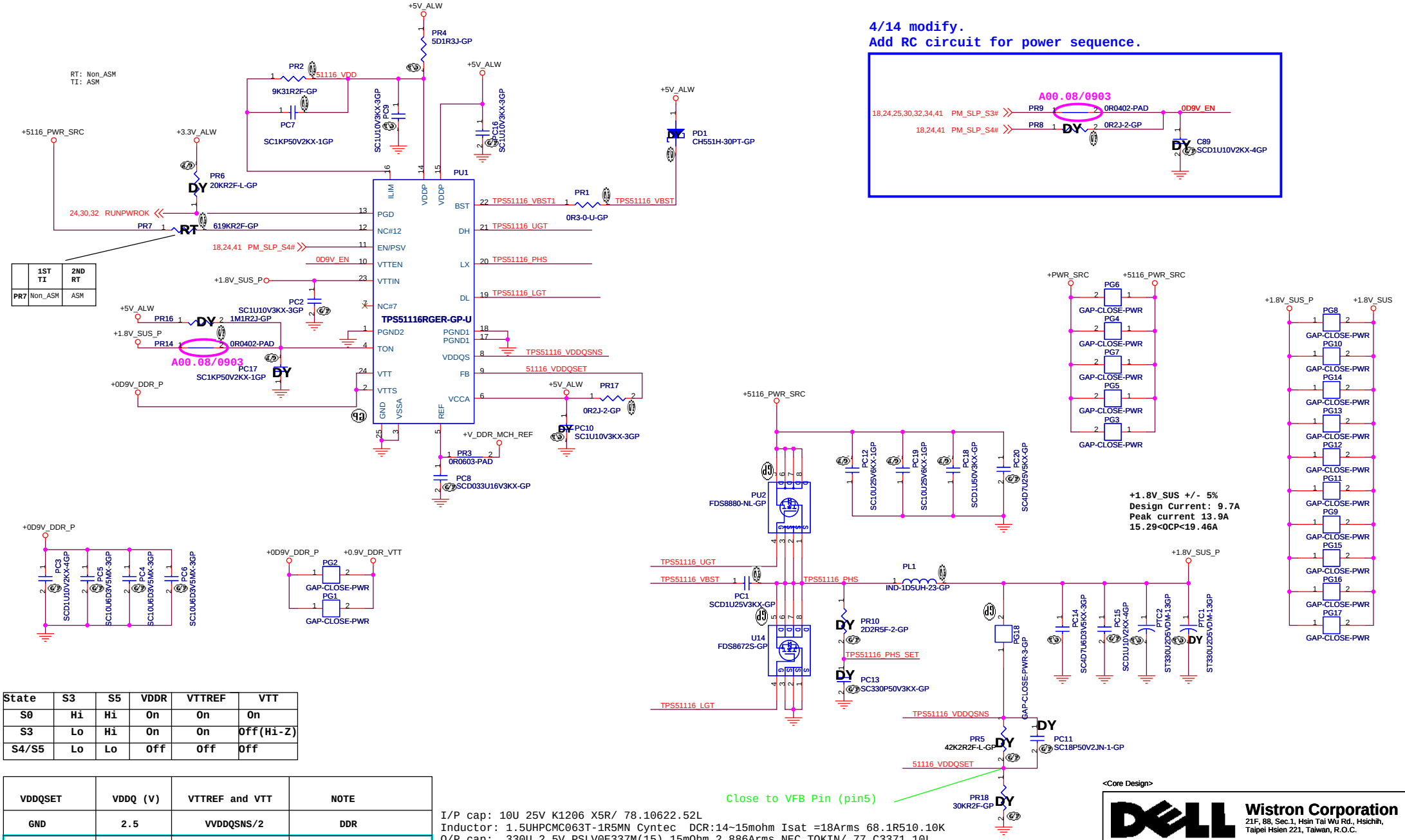
Title: DC to DC 1.05V

Size: Custom | Document Number: Roberts | Rev: A00

Date: Thursday, October 02, 2008 | Sheet 30 of 58

SSID = PWR.Plane.Regulator_1p8v0p9v

TI TPS51116 for 1.8V and 0.9V



	1ST TI	2ND RT
PR7	Non_ASM	ASM

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCMC063T-1R5MN Cyntec DCR:14~15mohm Isat =18Arms 68.1R510.10K
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: FDS8880 SO-8/9.6mohm/ 12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A37
Switching freq-->400KHz

<Core Design>

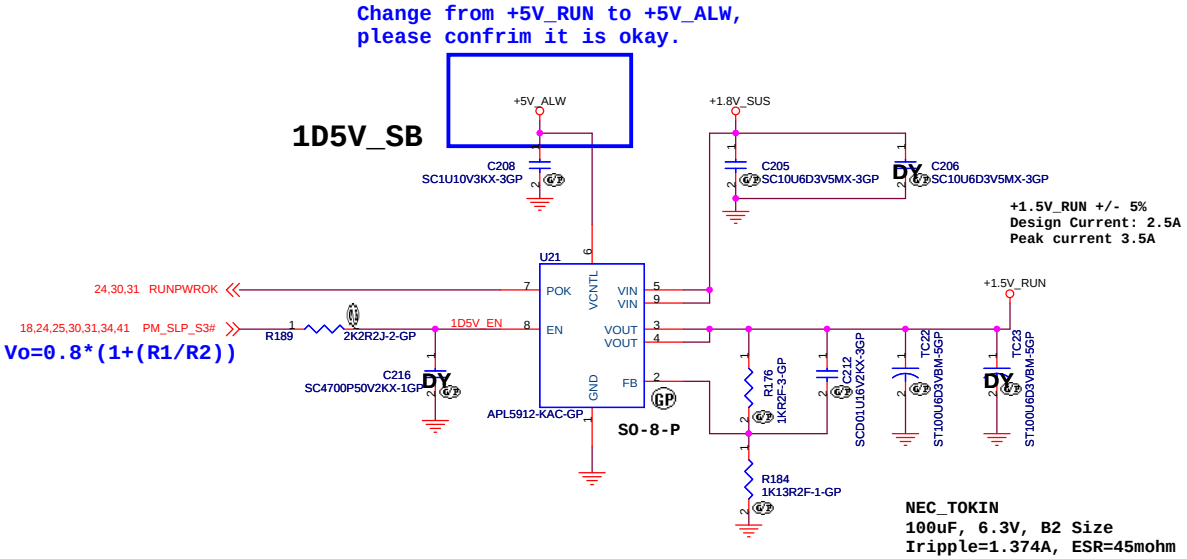
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1.8V/0.9V

Size	Document Number	Rev
Custom	Roberts	A00

Date: Thursday, October 02, 2008 Sheet 31 of 58

SSID = PWR.Plane.Regulator_1p5v



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DC to DC 1.5V	
Size: Custom	Document Number: Roberts	Rev: A00
Date: Thursday, October 02, 2008	Sheet 32 of 58	

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

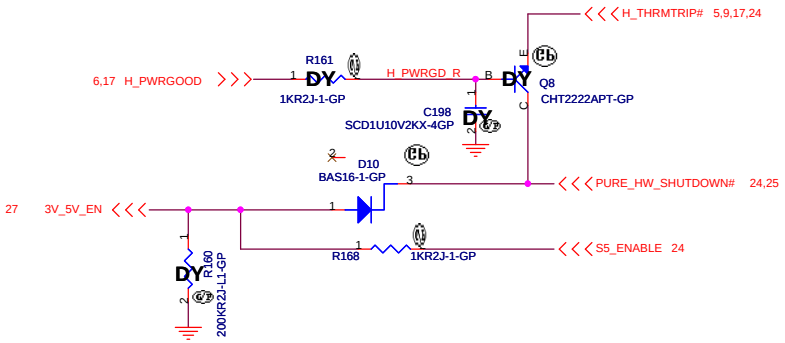
Title

VGA Power

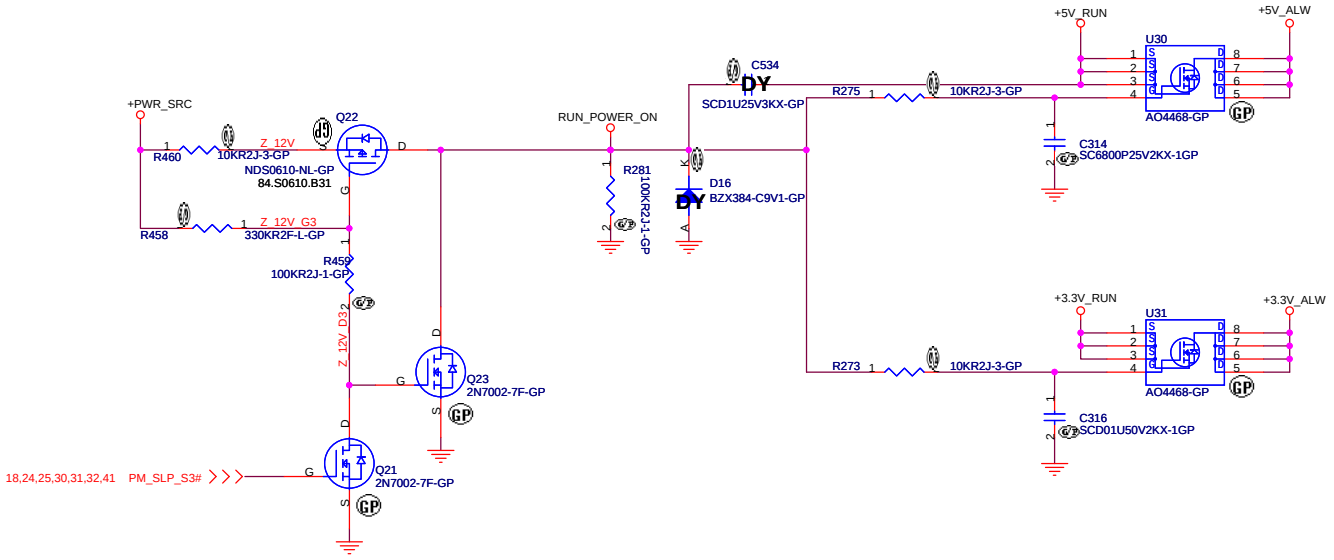
Size	Document Number	Rev
Custom	Roberts	A00

Date: Tuesday, September 09, 2008 Sheet 33 of 58

SSID = Reset.Suspend



Run Power



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

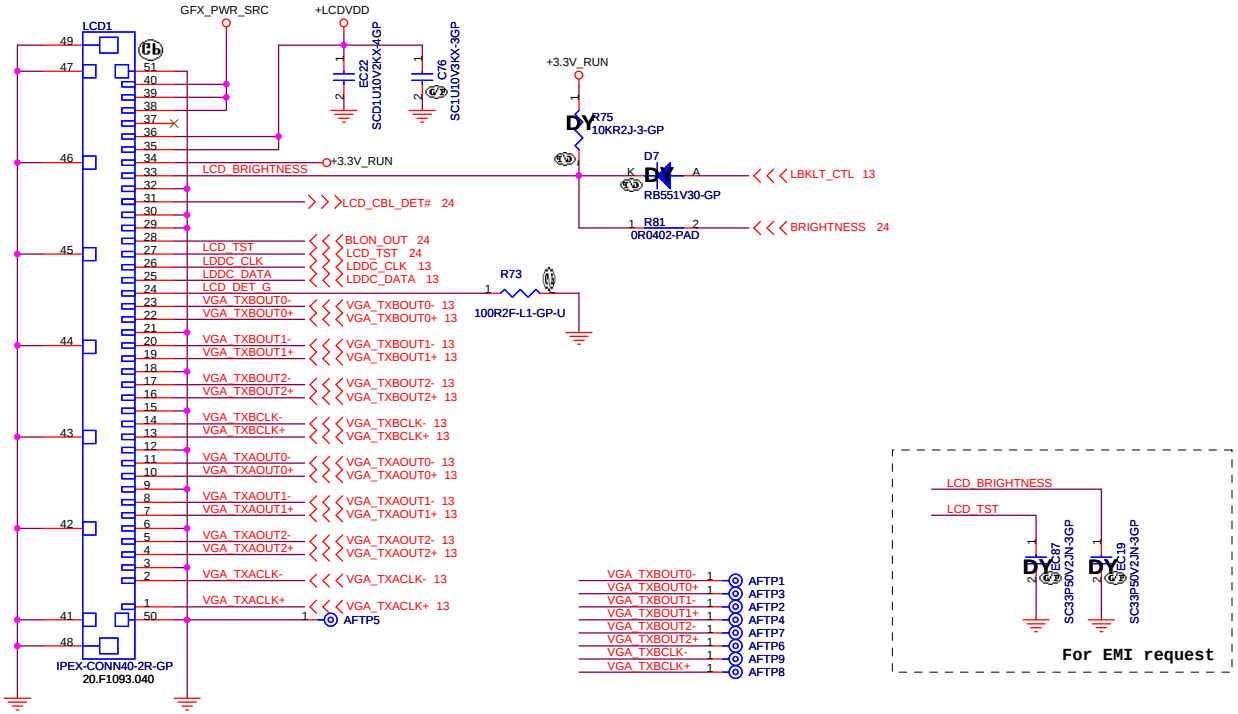
Title: ***Power Plane Enable***

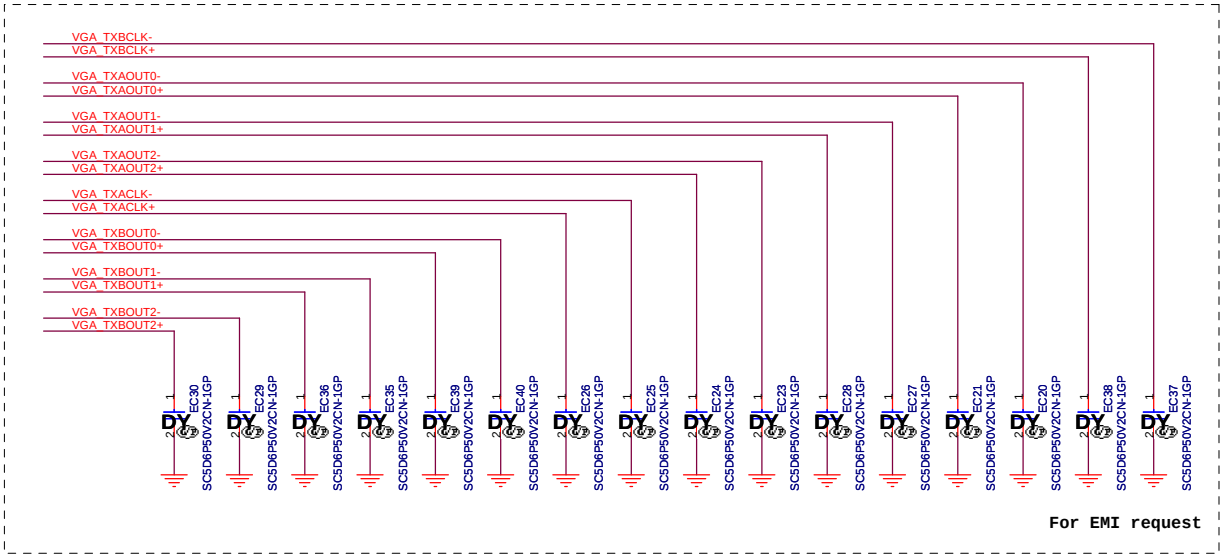
Size	Document Number	Rev
Custom	***Roberts***	*A00*

Date: Thursday, October 02, 2008 Sheet 34 of 58

SSID = VIDEO

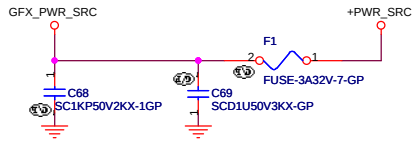
LVDS CONNECTOR





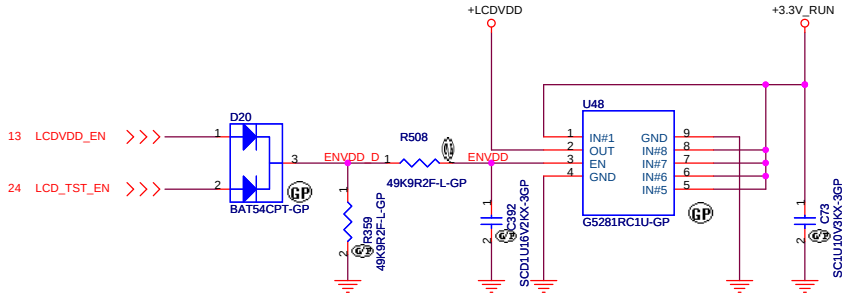
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

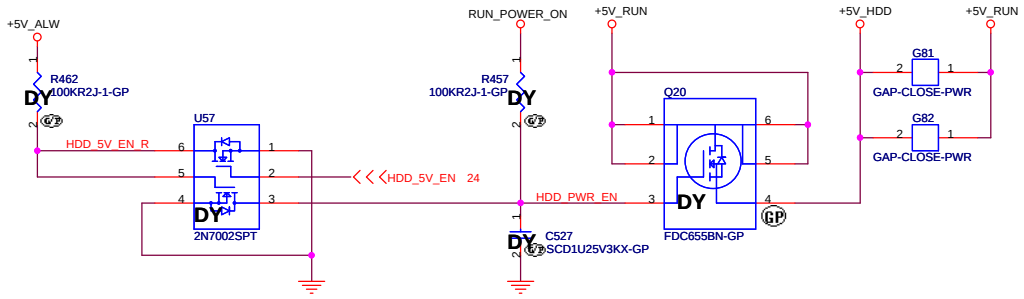
Title: LCD/Inverter Connector

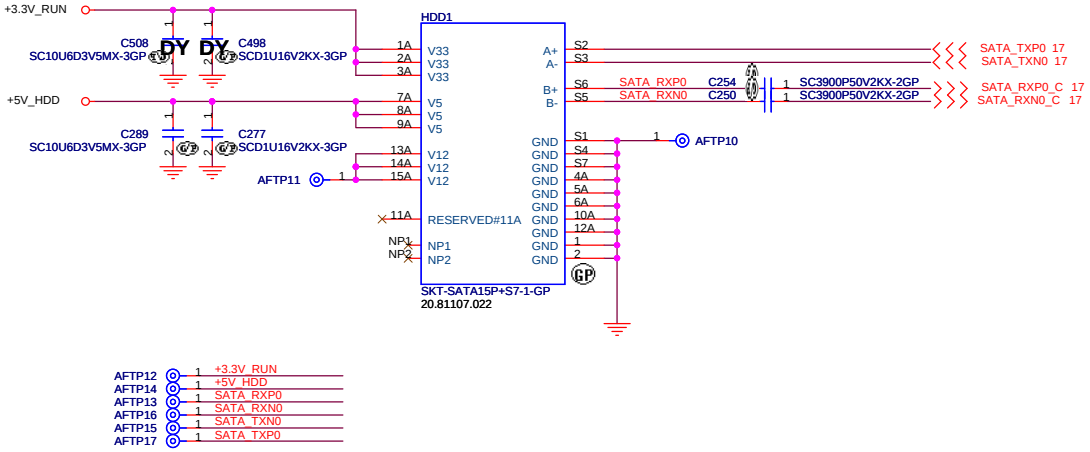
Size	Document Number	Rev
Custom	Roberts	A00

Date: Thursday, October 02, 2008 Sheet 35 of 58

SSID = SATA

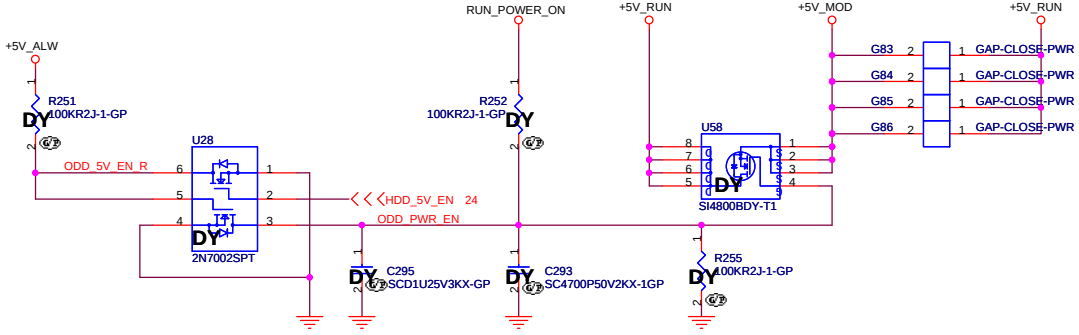
SATA HDD Connector

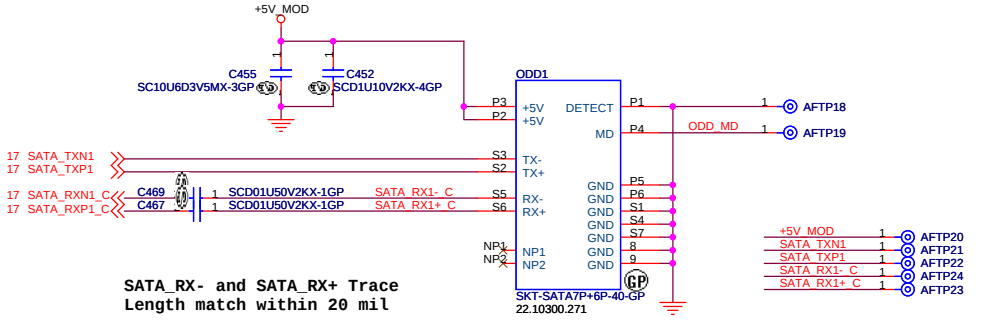




SSID = SATA

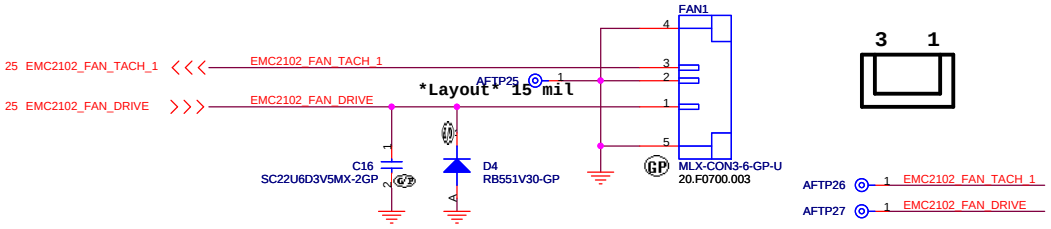
ODD Connector





SSID = Thermal

Fan Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

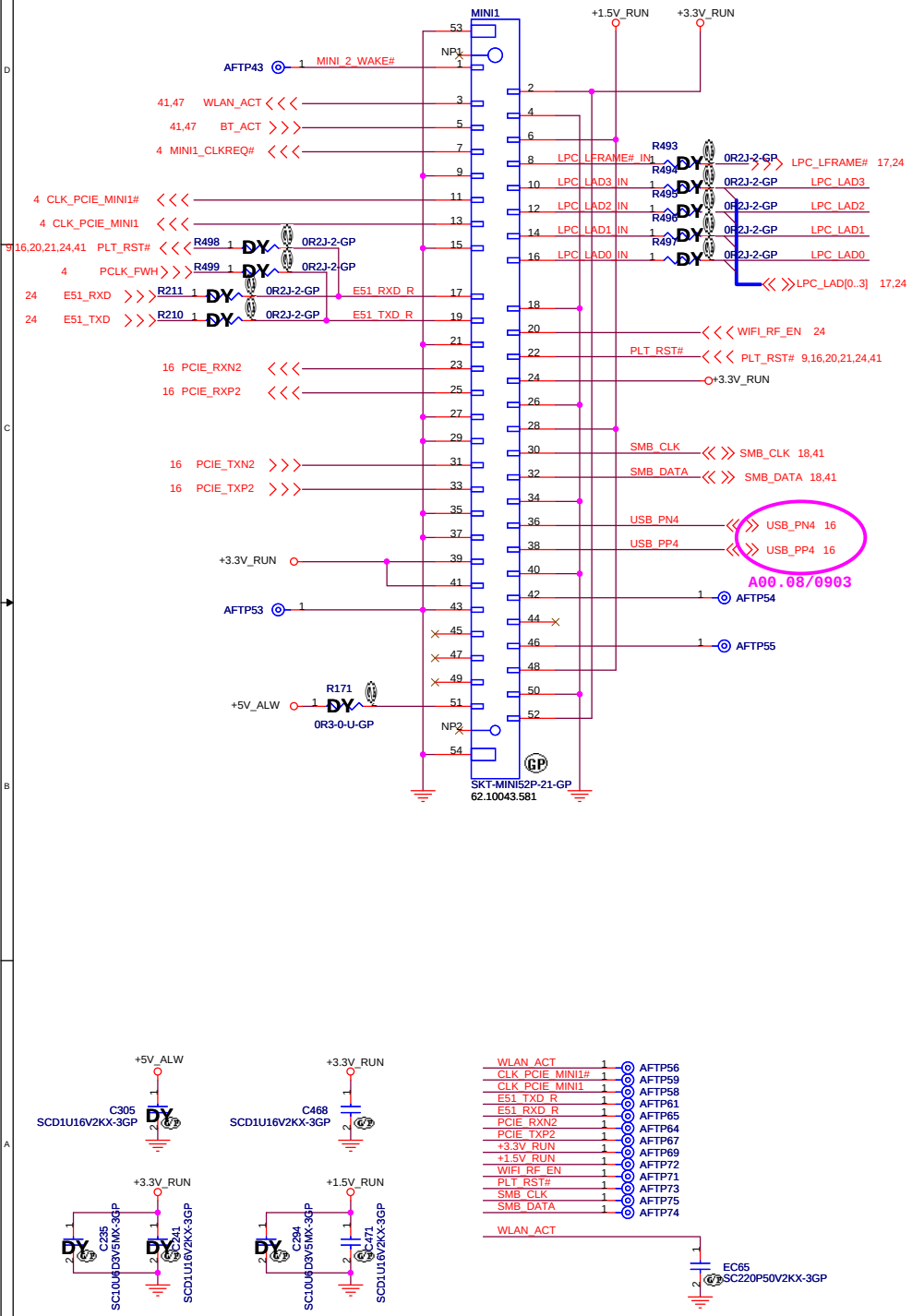
Title: HDD/ODD/FAN

Size: Custom | Document Number: Roberts | Rev: A00

Date: Thursday, October 02, 2008 | Sheet 36 of 58

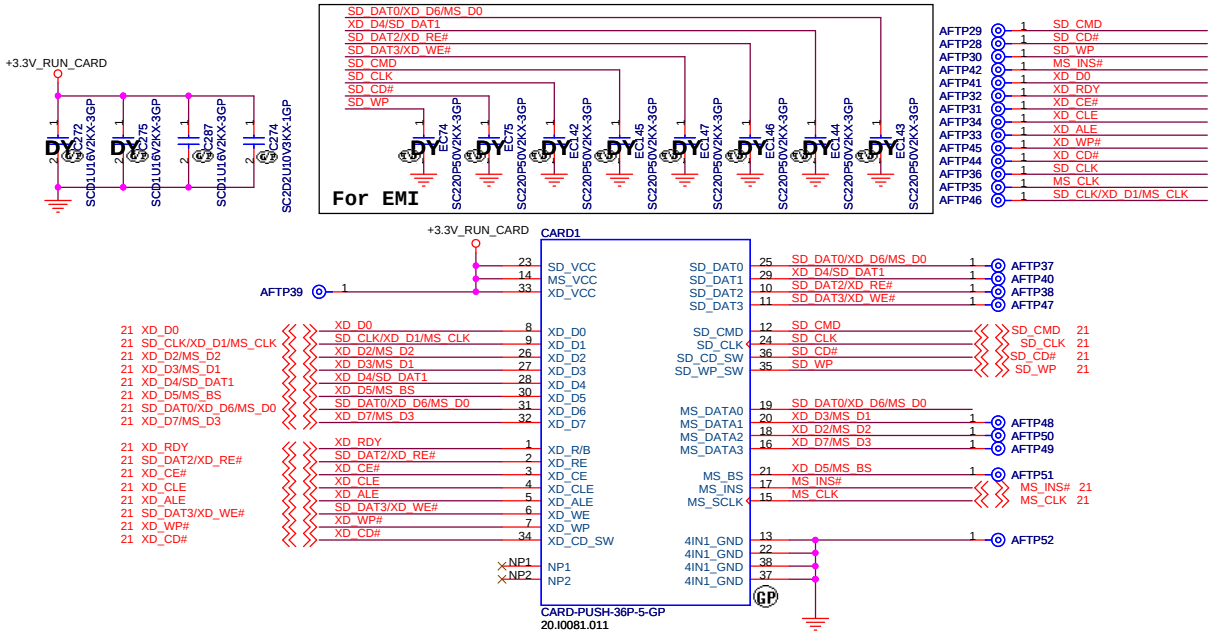
SSID = Wireless

Mini Card Connector(802.11a/b/g)



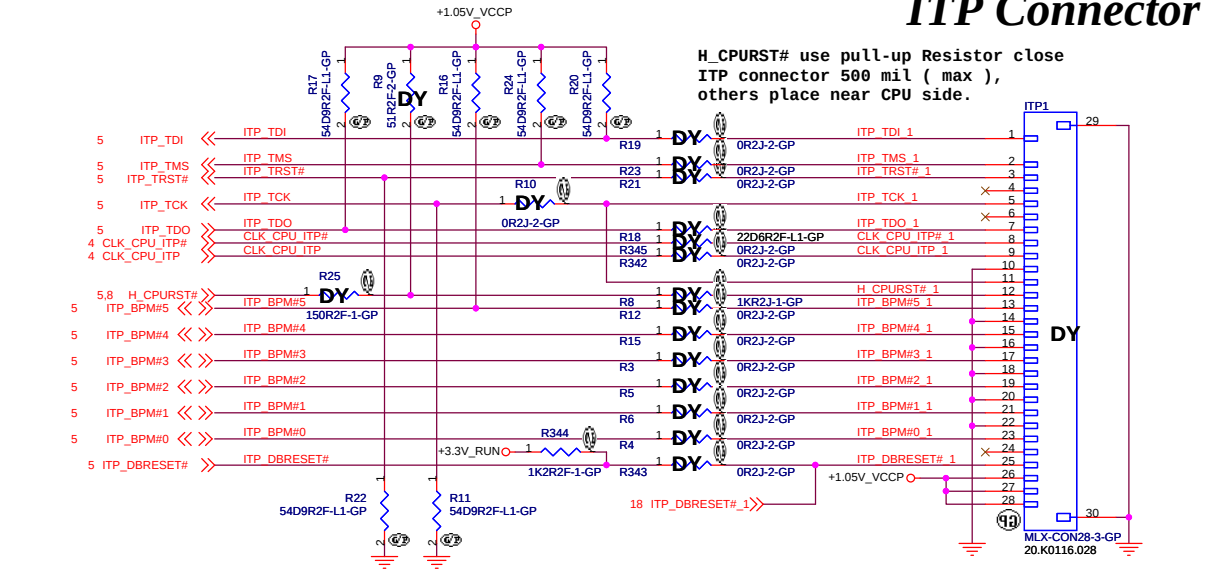
SSID = SDIO

SD/XD/MS Card Reader



SSID = User.Interface

ITP Connector



+1.05V_VCCP use Decoupling Capacitor close
ITP connector 100 mil (max)

CPU

TCK(PIN AC5)

ITP Connector

TCK(PIN 5)

FBO(PIN 11)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)/SD/ITP CONN

Size	Document Number	Rev
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

MINICARD(WWAN)

Size	Document Number	Rev
Custom	***Roberts***	***A00***

Date:	Monday, September 22, 2008	Sheet	38	of	58

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai WU Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

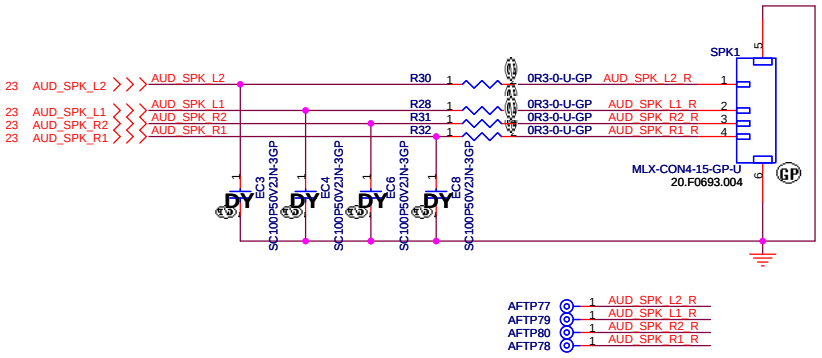
Title: *MINICARD(WPAN)*

Size: Custom | Document Number: *Roberts* | Rev: *A00*

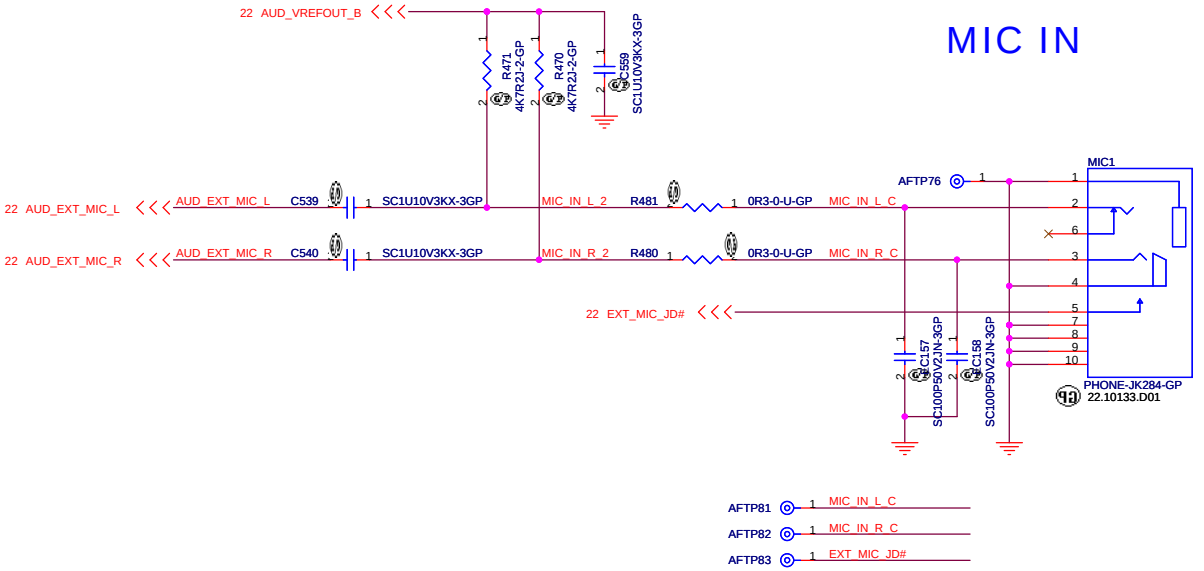
Date: Monday, September 22, 2008 | Sheet 39 of 58

SSID = AUDIO

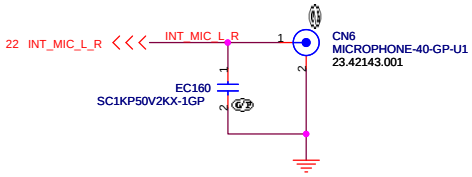
Speaker Connector



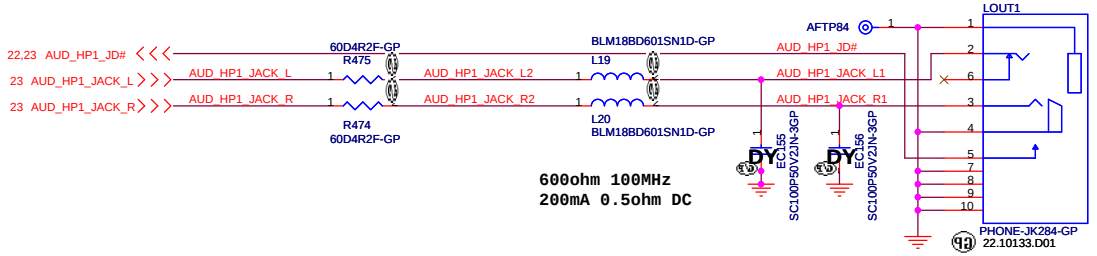
MIC IN



Internal Microphone



LINE1 OUT



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack

Size: Custom | Document Number: Roberts | Rev: A00

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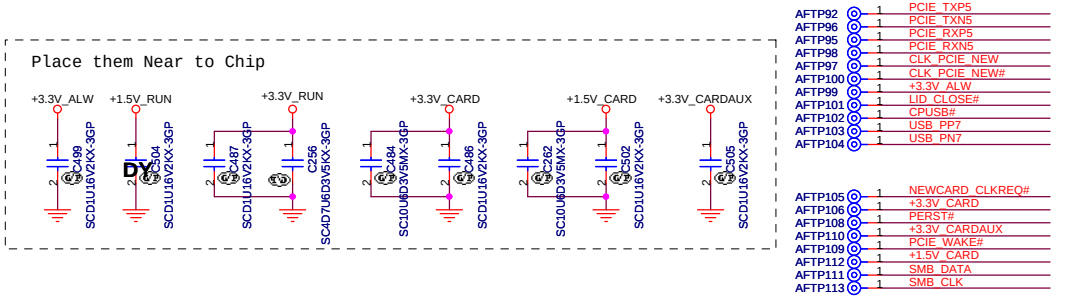
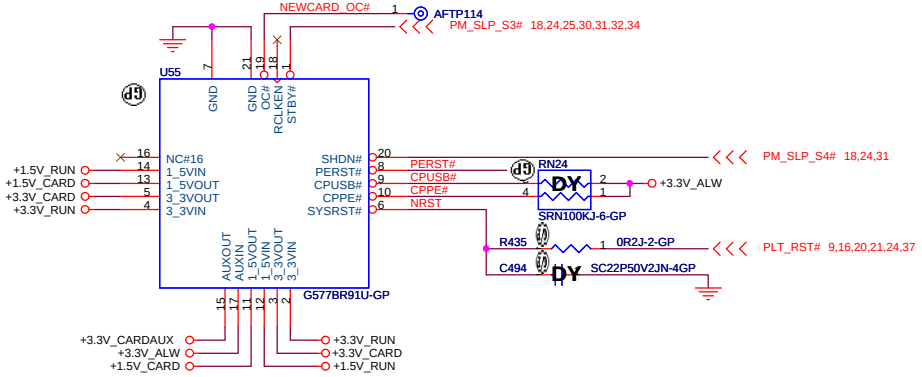
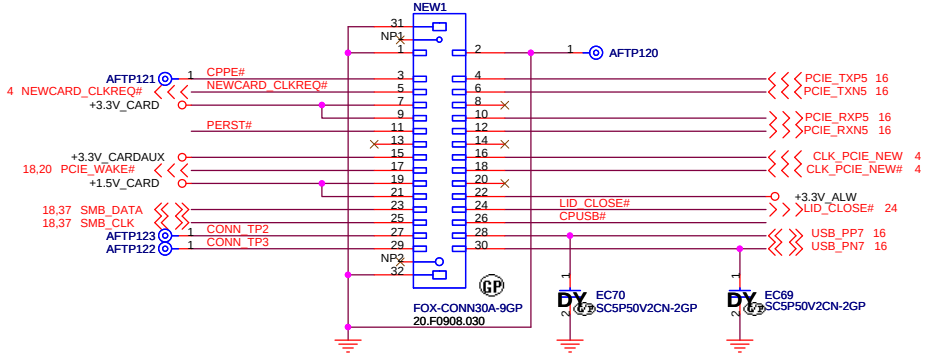
SSID = ExpressCard





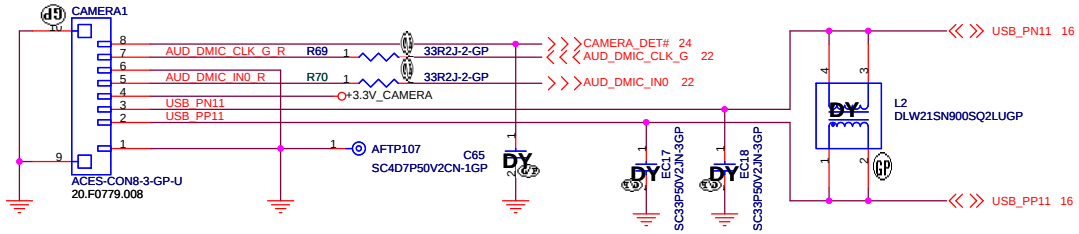
+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

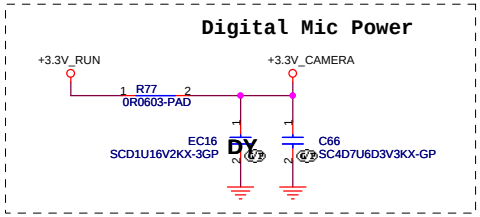
New Card Connector

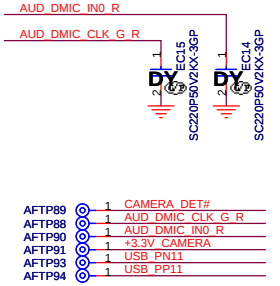


SSID = User.Interface

Camera Connector

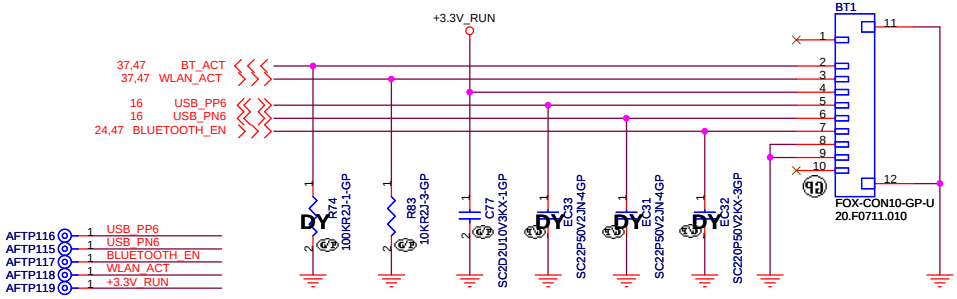






SSID = User.Interface

Bluetooth Module conn.



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Bluetooth/CAM/New Card**

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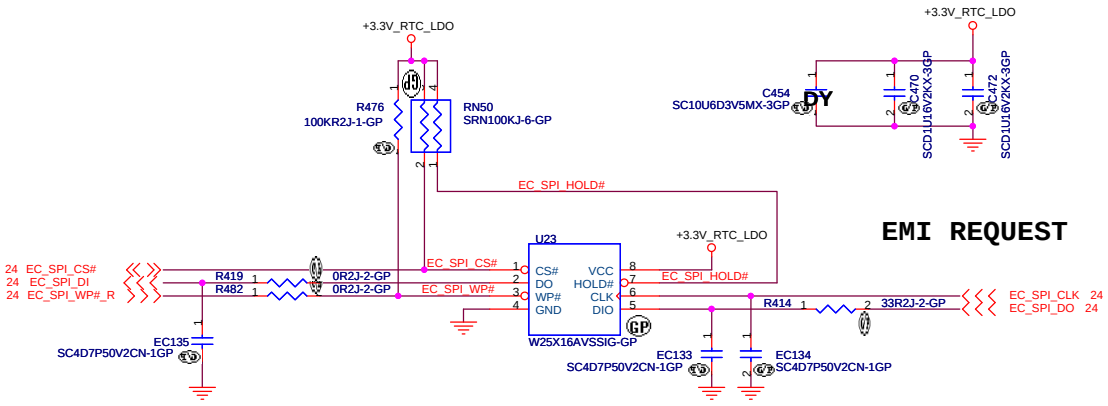
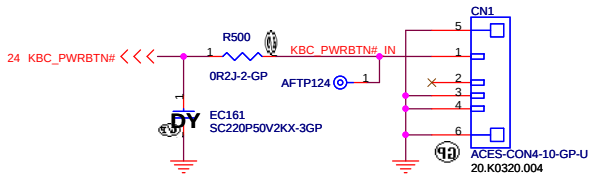
SPI FLASH ROM (16M bits)

SSID = Flash.ROM



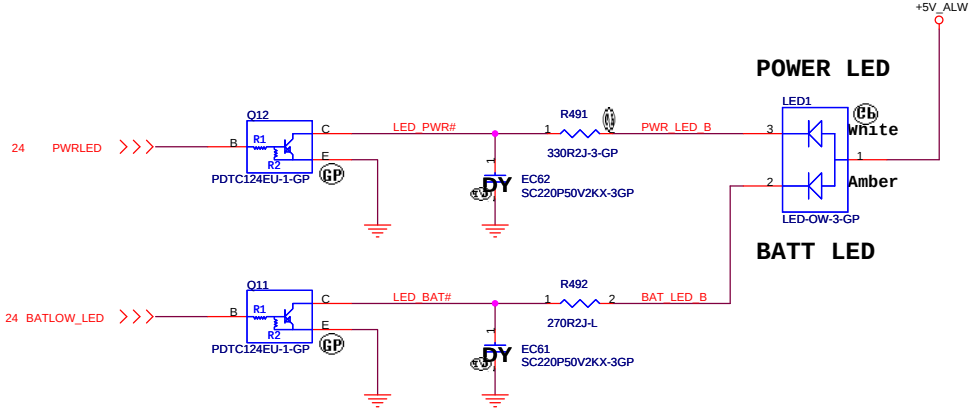
SSID = User.Interface

Power Dash Board to Board CONN



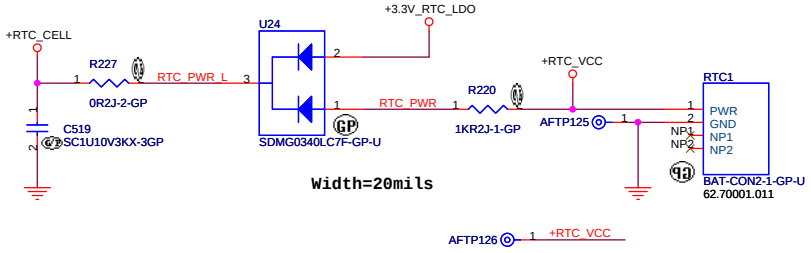
SSID = User.Interface

Power/Battery LED



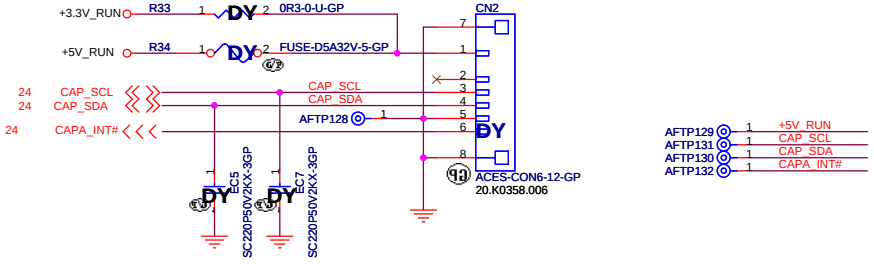
SSID = RBATT

RTC Connector



SSID = User.Interface

Capacitive Button



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: FWH/LED/Power Dash/RTC/Cap

Size	Document Number	Rev
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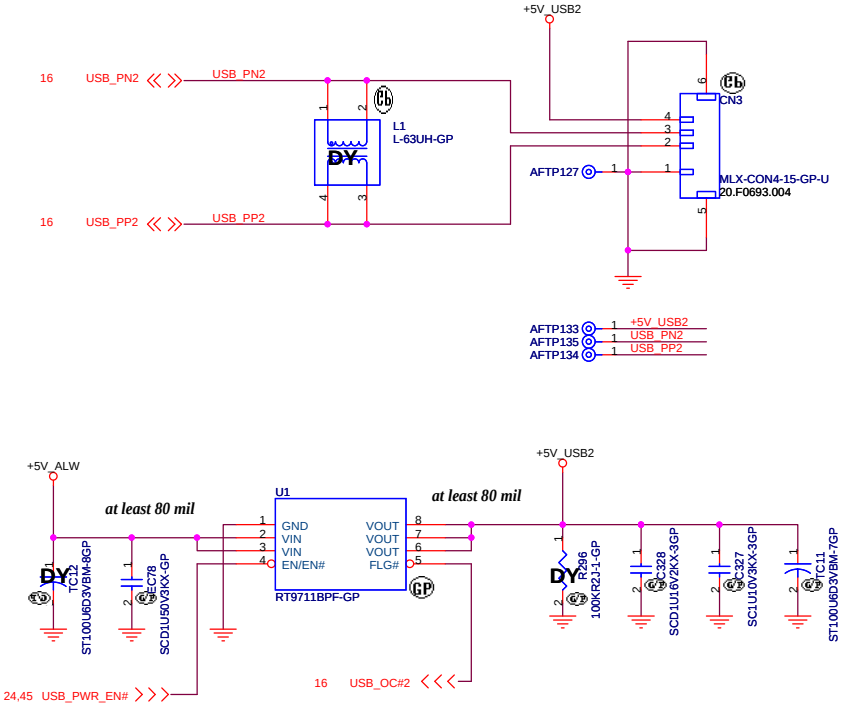
SSID = USB

Right USB Port CONN



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB		
Size: Custom	Document Number: Roberts	Rev: A00
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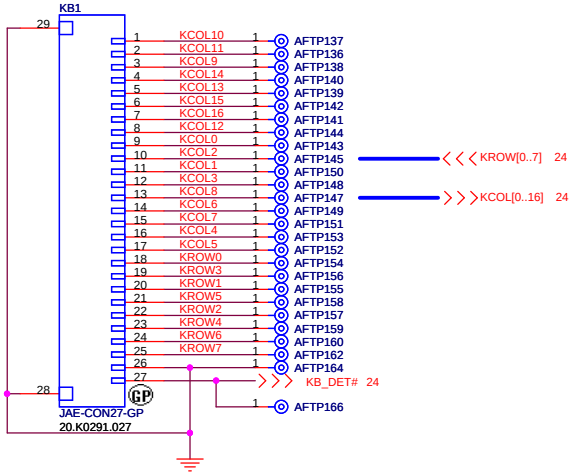
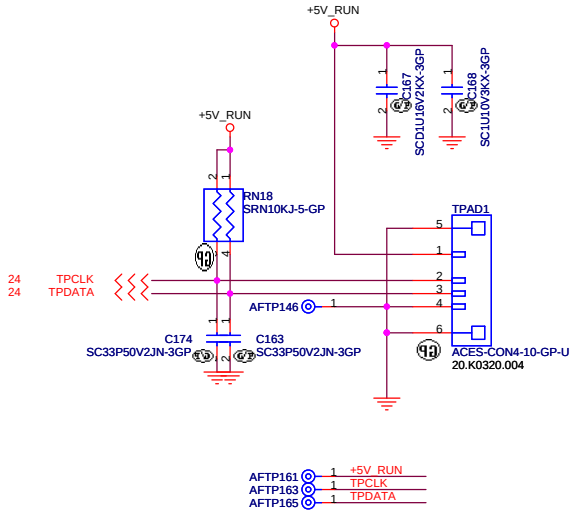
SSID = KBC

Internal KeyBoard Connector

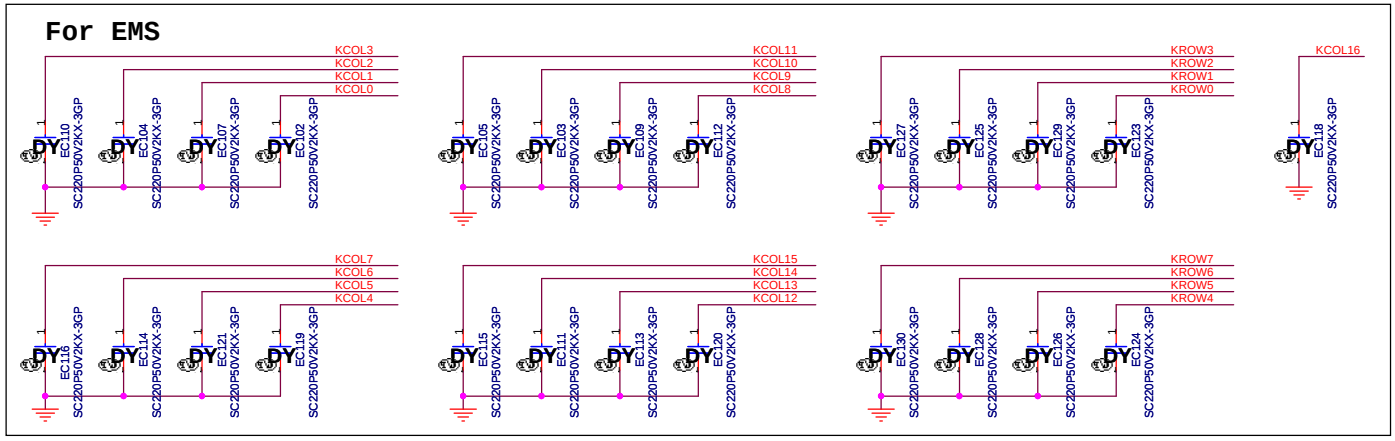


SSID = Touch.Pad

TouchPad Connector



For EMS



<Core Design>

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Title: ***KeyBoard/Touch Pad***

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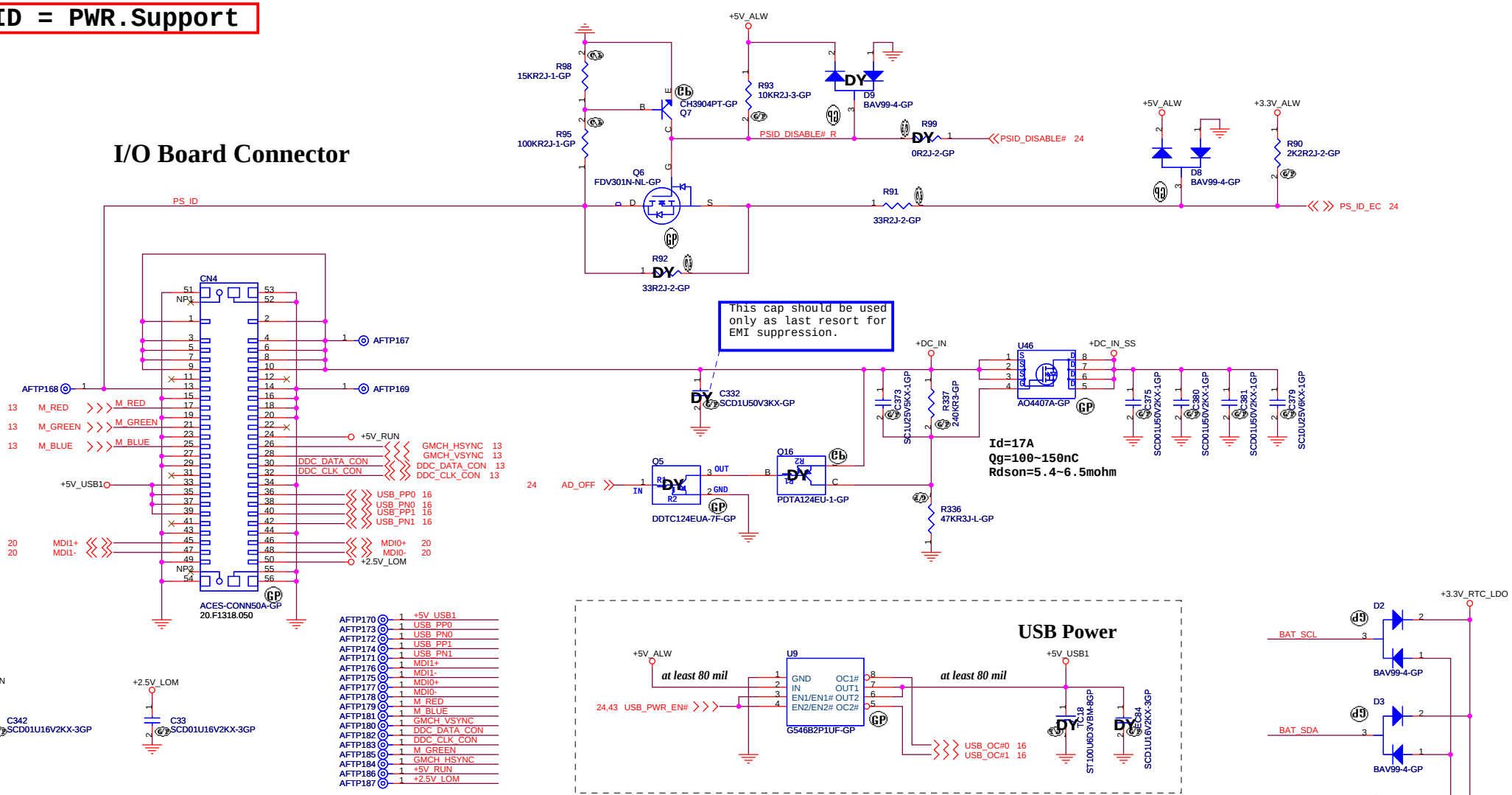
SSID = PWR.Support

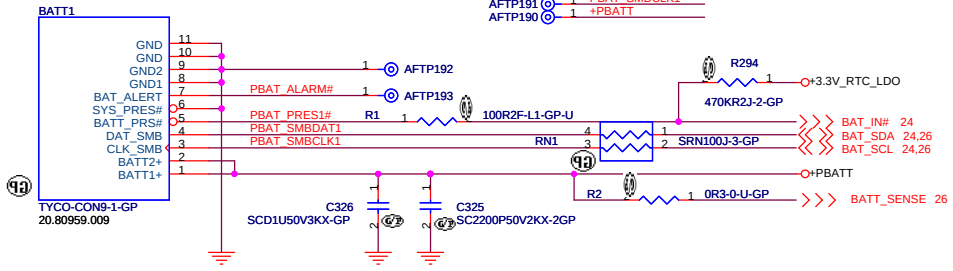
I/O Board Connector



AFTP170 +5V_USB1
AFTP173 USB_PP0
AFTP172 USB_PN0
AFTP174 USB_PP1
AFTP171 USB_PN1
AFTP176 MDI1+
AFTP175 MDI1-
AFTP177 MDI0+
AFTP178 MDI0-
AFTP179 M_RED
AFTP181 M_BLUE
AFTP180 GMCH_VSYNC
AFTP182 DDC_DATA_CON
AFTP183 DDC_CLK_CON
AFTP185 M_GREEN
AFTP184 GMCH_HSYNC
AFTP186 +5V_RUN
AFTP187 +2.5V_LOM

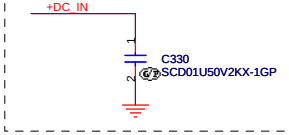
USB Power

Batt Connecter



AFTP188 PBAT_PRES1#
AFTP189 PBAT_SMBDAT1
AFTP191 PBAT_SMBCLK1
AFTP190 +PBATT

Reserved for EMI
Place near DCIN1



<Core Design>

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Title: LEFT IO/DCIN/BATT CONN

Size	Document Number	Rev
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SSID = LOM

SSID = VIDEO

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<Core Design>

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Title: LAN CONNECTOR / CRT

Size: Custom | Document Number: Roberts | Rev: A00

Date: Tuesday, September 09, 2008 | Sheet 46 of 58

SSID = Mechanical

+3.3V_RTC_LDO

EC54 SCD1U16V2KX-3GP
EC151 SCD1U16V2KX-3GP
EC81 SCD1U16V2KX-3GP
EC88 SCD1U16V2KX-3GP

+3.3V_RUN

EC93 SC47P50V2JN-3GP
EC9 SCD1U16V2KX-3GP
EC71 SCD1U16V2KX-3GP
EC122 SCD1U16V2KX-3GP
EC108 SCD1U16V2KX-3GP

+5V_ALW

EC60 SCD1U16V2KX-3GP
EC53 SCD1U16V2KX-3GP
EC96 SCD1U16V2KX-3GP
EC99 SC47P50V2JN-3GP

+DC_IN_SS

EC32 SCD1U50V3KX-GP
EC324 SCD1U50V3KX-GP

+PWR_SRC

EC97 SCD1U50V3KX-GP
EC13 SCD1U50V3KX-GP
EC1 SCD1U50V3KX-GP
EC94 SCD1U50V3KX-GP

+1.05V_VCCP

EC49 SCD1U16V2KX-3GP
EC138 SCD1U16V2KX-3GP
EC51 SCD1U16V2KX-3GP
EC89 SCD1U16V2KX-3GP
EC2 SCD1U16V2KX-3GP
EC131 SCD1U16V2KX-3GP

24,41 BLUETOOTH_EN
37,41 WLAN_ACT
37,41 BT_ACT

EC162 SCD1U25V2ZY-1GP
EC163 SCD1U25V2ZY-1GP
EC164 SCD1U25V2ZY-1GP

+5V_MOD

EC165 SCD1U16V2KX-3GP
EC166 SCD1U16V2KX-3GP

+5V_ALW +3.3V_ALW

EC167 SCD1U16V2KX-3GP
EC168 SCD1U16V2KX-3GP
EC169 SCD1U16V2KX-3GP

+0.9V_DDR_VTT

EC41 SCD1U16V2KX-3GP
EC34 SCD1U16V2KX-3GP
EC43 SCD1U16V2KX-3GP

+1.8V_SUS

EC45 SCD1U16V2KX-3GP
EC44 SCD1U16V2KX-3GP
EC47 SCD1U16V2KX-3GP
EC46 SCD1U16V2KX-3GP
EC55 SCD1U16V2KX-3GP
EC98 SCD1U16V2KX-3GP
EC106 SCD1U16V2KX-3GP
EC117 SCD1U16V2KX-3GP

+3.3V_RUN

EC91 SCD1U16V2KX-3GP

H18 H11 H5 H13 H15
H12 H9 H10 H4 H17
HOLE355X355RH-1 S1-GP

H3 HOLE
H2 HOLE
H7 HOLE
H8 HOLE
H1 HOLE

H20 HOLE355X355RH-1 S1-GP

For TP button holder touch.

+5V_RUN

EC85 SCD1U16V2KX-3GP
EC101 SCD1U16V2KX-3GP
EC92 SCD1U16V2KX-3GP

+5V_RUN

EC90 SCD1U16V2KX-3GP
EC11 SCD1U16V2KX-3GP
EC50 SCD1U16V2KX-3GP
EC68 SCD1U16V2KX-3GP
EC153 SCD1U16V2KX-3GP
EC152 SCD1U16V2KX-3GP
EC148 SCD1U16V2KX-3GP
EC67 SCD1U16V2KX-3GP
EC59 SCD1U16V2KX-3GP
EC52 SCD1U16V2KX-3GP
EC100 SCD1U16V2KX-3GP
EC95 SCD1U16V2KX-3GP

+3.3V_RUN

EC83 SCD1U16V2KX-3GP
EC137 SCD1U16V2KX-3GP
EC150 SCD1U16V2KX-3GP
EC159 SCD1U16V2KX-3GP

+3.3V_RUN

EC58 SCD1U16V2KX-3GP
EC10 SCD1U16V2KX-3GP
EC86 SCD1U16V2KX-3GP
EC64 SCD1U16V2KX-3GP
EC141 SCD1U16V2KX-3GP
EC149 SCD1U16V2KX-3GP
EC136 SCD1U16V2KX-3GP
EC72 SCD1U16V2KX-3GP
EC63 SCD1U16V2KX-3GP
EC42 SCD1U16V2KX-3GP
EC66 SCD1U16V2KX-3GP
EC73 SCD1U16V2KX-3GP

H6 HOLE

H14 HOLE
H16 HOLE
H19 HOLE

34.4W005.001
Mini Card BOSS

34.4W004.001
New Card BOSS

34.4W001.001
NB Thermal BOSS

BOSS Placement

+PWR_SRC

EC173 SCD1U25V2ZY-1GP
EC171 SCD1U25V2ZY-1GP
EC172 SCD1U25V2ZY-1GP
EC170 SCD1U25V2ZY-1GP
EC174 SCD1U25V2ZY-1GP

SPR2 SPRING-24-GP 34.45T31.001
SPR3 SPRING-24-GP 34.45T31.001
SPR5 SPRING-58-GP 34.4B312.002
SPR4 SPRING-24-GP 34.45T31.001
SPR1 SPRING-24-GP 34.45T31.001
SW1 SPRING-24-GP
Spring

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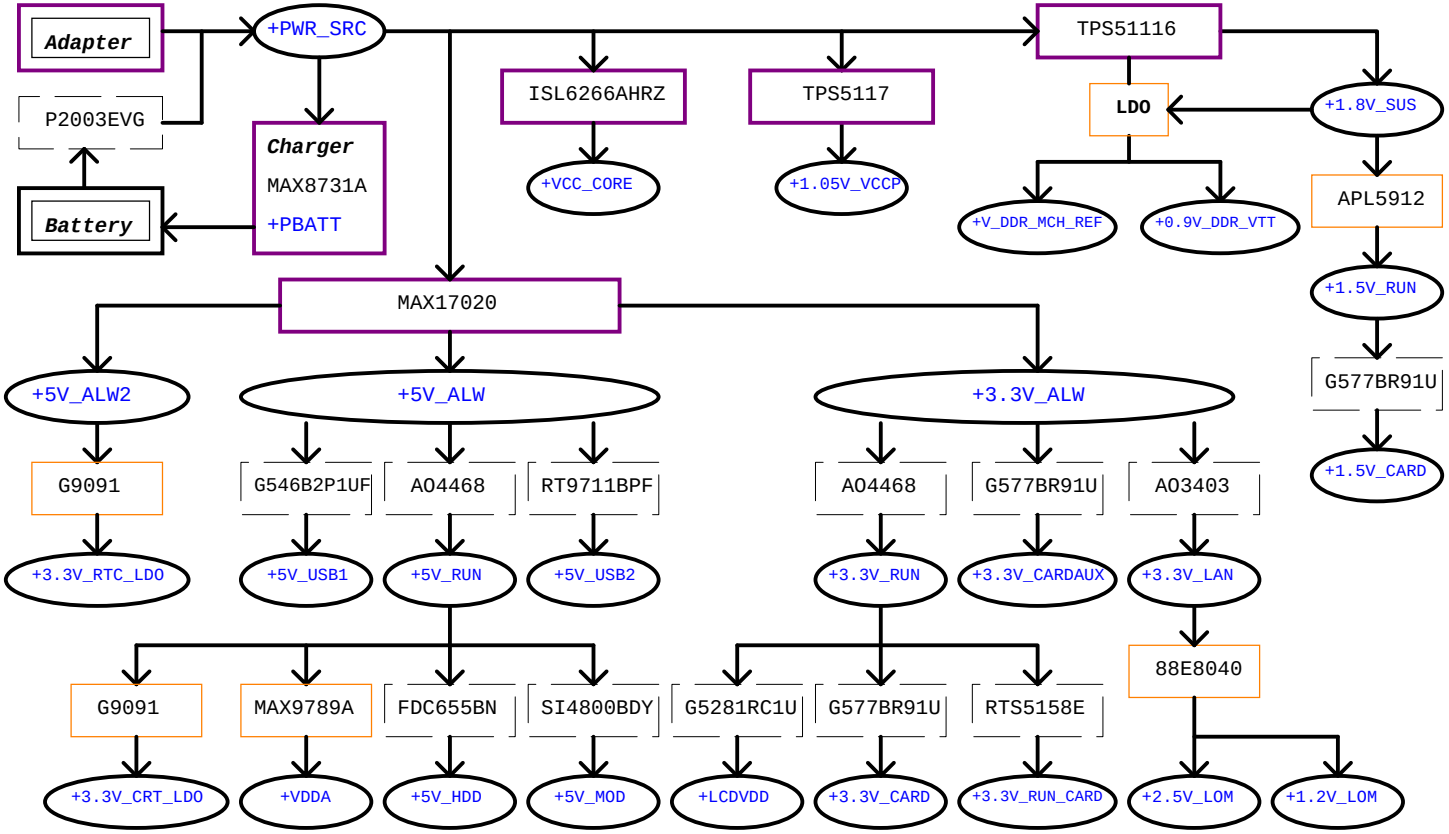

Power Shape

Regulator	LDO	Switch

<Core Design>

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Title: ***Power Block Diagram***

Size	Document Number	Rev
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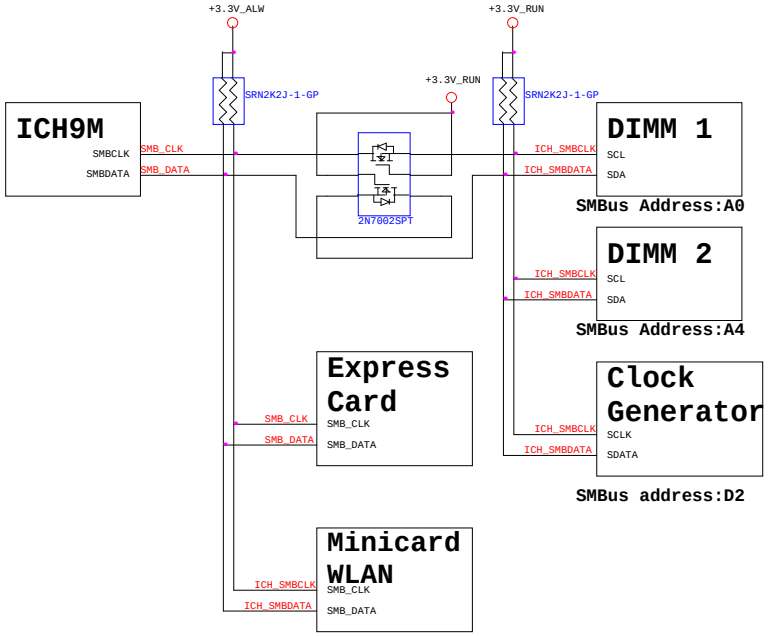
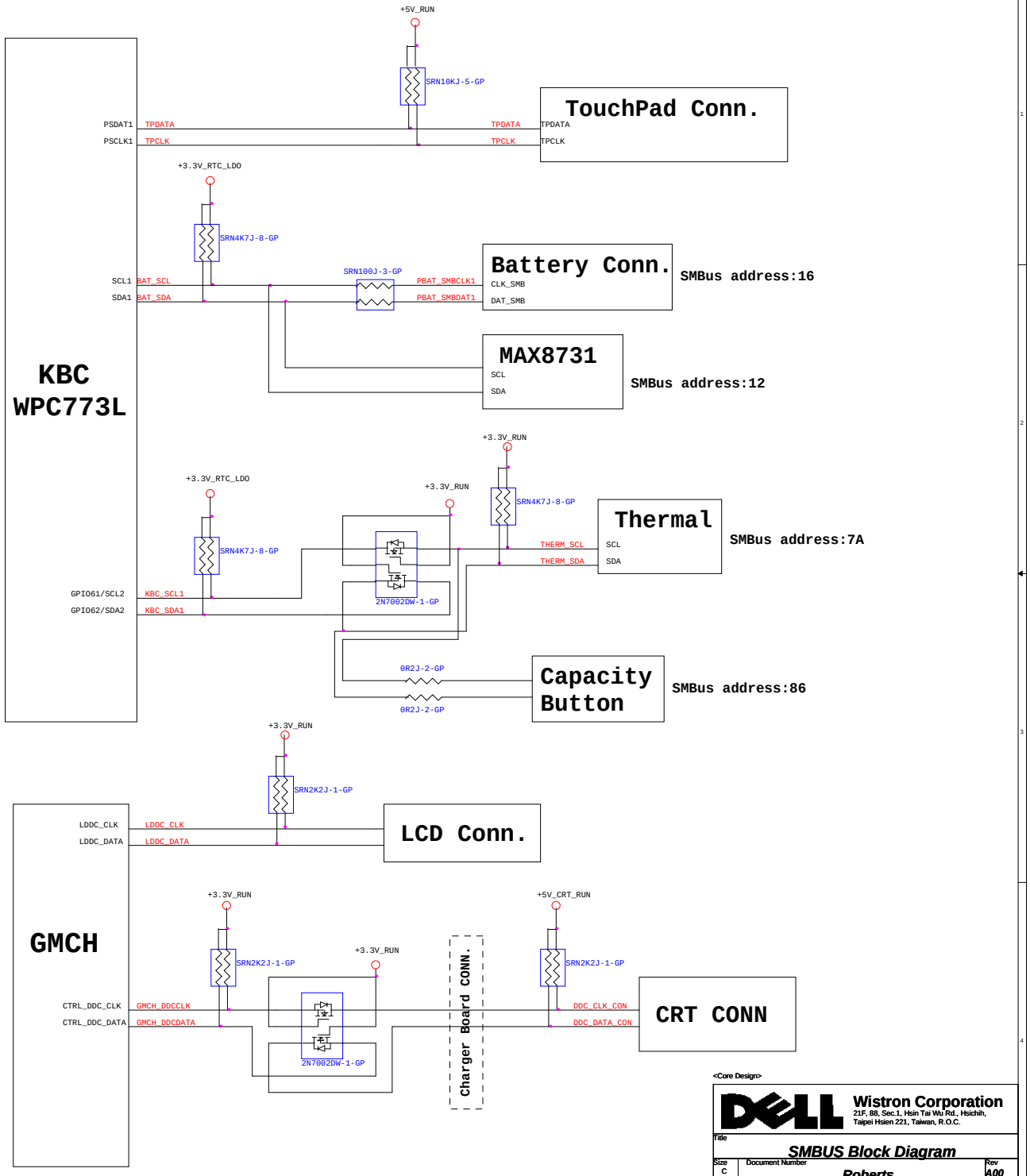
ICH9M SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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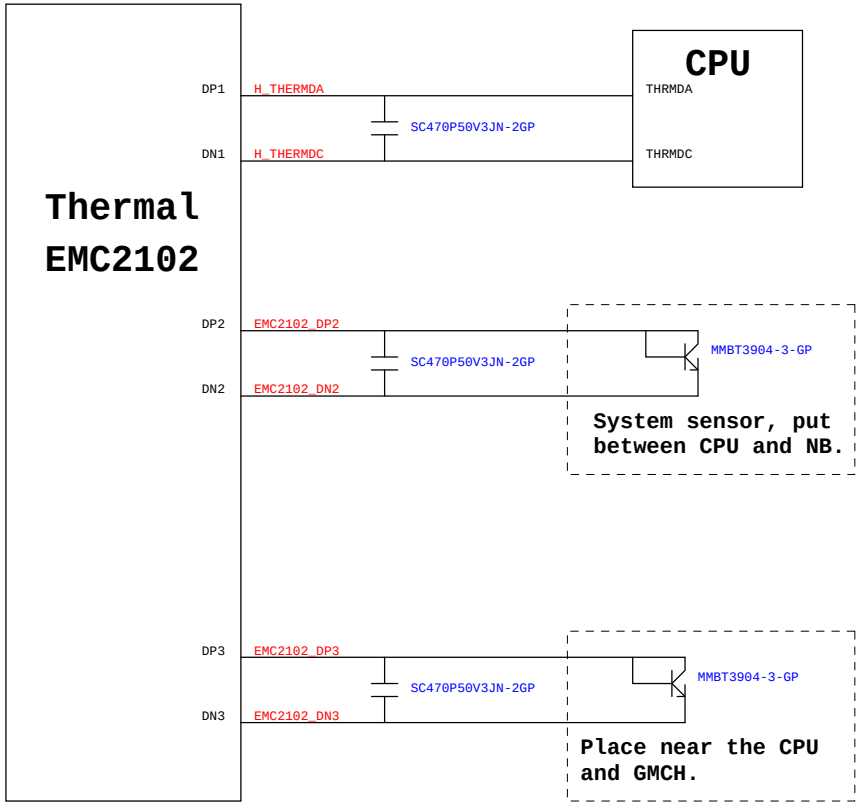
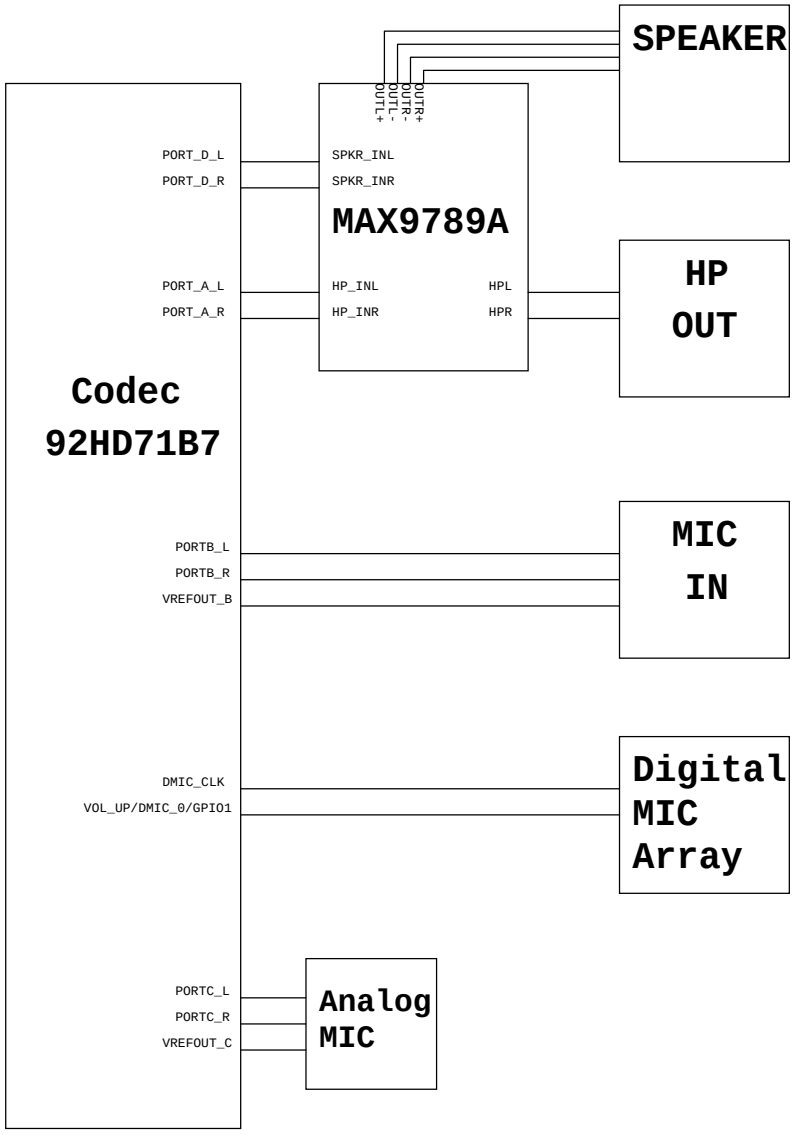
Thermal Block Diagram



Audio Block Diagram



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Title	Thermal/Audio Block Diagram	
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Title: VGA-PCIE(1/4)

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Title: *VGA-VRAM(2/4)*

Size: Custom | Document Number: *Roberts* | Rev: *A00*

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Title: *VGA-HDMI/STRAP(3/4)*

Size	Document Number	Rev
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Title

VGA-LVDS/TV/CRT/(4/4)

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Title: VRAM

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DATE	VERSON	NO	PAGE	Modified List	Issue Description	OWNER
06/03	X01	1	45	CN4 Pin.51 from +DC_IN change to GND.	CN4 Pin.51 should be ground.	EE
		2	24	Dummy R422	LID SW is push-pull type, no need pull high.	EE
		3	41	CAMERA1 conn reduce from 10 to 8 pin.	Follow camera design.	EE
		4	42	RTC1 CONN change p/n: 22.70031.001 to 62.70001.011.	Qty issue to change another.	EE
		5	46	Exchange H14 and H6 names.	Correction. H14 for mini card boss ; H6 is hole.	EE
06/05		6	42	Reverse LED1.	Correction. Amber for BAT_LED_B ; White for PWR_LED_B.	EE
		7	37,41	Remove CN5 and related circuit in page.41. Add dummy R: R493, R494, R495, R496, R497, R498, R499	Remove debug board connector. For debug mini card, change LPC Bus to mini card base. Set dummy res to avoid damaging MB or additional mini card.	EE
		8	37	Dummy R210, R211	For debug mini card. Set dummy res to avoid damaging MB or additional mini card.	EE
		9	24	Dummy R150. Staff R151.	PCB Version for SB.	EE
06/06		10	42	CN1 Pin.2 set to NC. Add R500 and dummy EC161.	Avoid shorting between KBC_PWRBTN# and GND. New R and C are for EMC pre-location.	EE
		11	24	Dummy R406. Change R425, R422, R409, R406, R401, R404 to 100K ohm.	Dummy R406 for no keyboard detect function. R change to 100k for save power.	EE
06/10		12	36	Update HDD symbol.	Update symbol and footprint for only SATA HDD. (no co-layout)	EE
		13	35~45	Change All TP near connectors to AFTP (ZZ.AFT30.101).	For AFTE test pad.	EE
		14	04	Change C461 and C462 from 15pF to 12pF.	For X3 cap choice by report suggestion.	EE
		15	17	Change C520 and C522 from 15pF to 12pF.	For X4 cap choice by report suggestion.	EE
06/12		16	24,42	Add 0 ohm R482 on EC_SPI_WP# and link to KBC/GPIO30. Change RN50 to 100k and Add R476 for EC_SPI_WP#.	KBC can control WP# of Flash ROM. R change to 100k for save power.	EE
		17	40	Change L19 and L20 to 68.00082.531.	For EMI.	EE
		18	45	Change M_RED to CN4 Pin.17 ; M_GREEN to CN4 Pin.21 ; M_BLUE to CN4 Pin.25. CN4 Pin.23 and Pin.27 to GND.	Avoiding noise to impact CRT signals.	EE
		19	47	Add H20.	Add square GND for TP button holder touch.	EE
06/16		20	42	Dummy CN2, R34.	Cap. button function is disable.	EE
		21	47	Add dummy EC162, EC163, EC164. Add dummy EC165, EC166. Add dummy EC167, EC168, EC169.	For EMI.	EE
06/17		22	04	Change R216 to 22 ohm.	The same clock dirve to U25 and U34.	EE
06/18		23	44	Dummy EC110, EC104, EC107, EC102, EC105, EC103, EC109, EC112, EC127, EC125, EC129, EC123, EC118, EC116, EC114, EC121, EC119, EC115, EC111, EC113, EC120, EC130, EC128, EC126, EC124.	For EMI.	EE
06/19		24	43	Short R26, R27.	No need 0 ohm R.	EE
		25	47	Add SW1.	ME request.	EE
		26	35	LCD1.38 link to GFX_PWR_SRC ; LCD1.37 set NC ; LCD1.35 link to +LCDVDD ; LCD1.34 link to +3.3V_RUN ; LCD1.33 link to LCD_BRIGHTNESS ; LCD1.32 to GND ; LCD1.31 link to LCD_CBL_DET#.	For LED backlight panel.	EE
		27	18	Dummy R179, R423.	SW check vender ID by SMBus.	EE
		28	24	Dummy R416, R418.	Cap. button function is disable.	EE
		29	40	Change LOUT1 and MIC1 to 22.10133.D01.	Change jack source.	EE
		30	17,18	Dummy U25.B10 link R506 to GND; U25.C18 link R501 to GND; Dummy U25.C21 link R502 to GND; U25.C11 link R503 to GND; Dummy U25.AE18 link R504 to GND; U25.AF21 link R505 to GND. Dummy R421, R424.	Avoiding abnormal action in U25(ICH9-M).	EE
06/23		31	25	Change R82 to 20K 1% ; Change R78 to 10K 1%.	For T8 shutdown is set 88 deg-C.	EE
		32	47	Add dummy EC170, EC171, EC172, EC173, EC174.	For EMI.	EE
06/27		33	42	Change U23 to 72.25X16.A01.	Better performance.	EE

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Title: Change List - EE (1/2)

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DATE	VERSON	NO	PAGE	Modified List	Issue Description	OWNER
07/30	X02	34	18	Staff R421, R424. (PT build cut-in)	Avoiding always issue interrupt event.	EE
		35	23	Dummy R290 ; Staff R291. (PT build cut-in)	Adjust audio amp. gain value.	EE
		36	20	Add dummy R507.	Add RUN power for LAN.	EE
		37	21	Short R253, R254.	No need 0 ohm R.	EE
		38	24	Staff R138, R150 ; Dummy R141, R151.	PCB Version for SC.	EE
		39	35	Add R508 ; Change R359 to 49.9k ohm.	For LCD power sequence.	EE
		40	22,23	Move C535 (Change 0.033uF), R472 to page.23. Remove C536 (Change 0.033uF), C542. Add R484 to gnd ; Add C566 for AUD_SET, C567 for AUD_BIAS. C565 for 6040 only.	For PC beep.	EE
		41	36	Material change: HDD1	ME request.	EE
		42	37	Material change: CARD1	ME request.	EE
		43	47	Material change: SPR4	ME request.	EE
		44	09	Add TP271 for U52/ SDVO_CTRLDATA.	TP.	EE
08/06		45	41	Short R79, R80.	No need 0 ohm R.	EE
		46	04	Symbol change: U54.	For clock generator co-layout.	EE
		47	-	Change to close line: R204, R200, R356, R139, R152, R408, R394, R390, R403, R402, R96, R120, R378, R360, R140, R373, R97, R405, R155, R154, R262, R266, R439, R265, R226, R269, R174, R175, R183, R432, R433, R434, R430, R431, R437, R191, R177, R270, R188, R436, R452, R259, R282, R250, R249, R467, R153, R81, R77.	No need 0 ohm R.	EE
		48	24,32	Move R182 to page.24.	Movement.	EE
		49	37	Short R428, R426 ; Add DY L21.	Pre-location for Minicard USB trace.	EE
08/07		50	-	Short R139, R96 , R155, R154, R226, R174, R175, R432, R433.	No need 0 ohm R.	EE
		51	19	Staff C488.	For DMI.	EE
08/11		52	23	Use 2.2uF C564 and C557 for Maxim U62 IC.	For improving bobo sound.	EE
		53	32	Material change: TC23. (DY)	Material issue.	EE
08/15		54	11	Material change: TC19, TC21.	Material issue.	EE
09/02	A00	55	21	USB_PP10 for U34.5 ; USB_PN10 for U34.4. (ST build cut-in)	Schematic modification.	EE
		56	24	Staff R151 ; Dummy R150.	PCB Version for -1(Xbuild).	EE
		57	24	Add dummy R509 to gnd for KBC GPIO24. (09/10 update)	For GM45.	EE
09/03		58	05,17	Dummy R76 ; Staff R167	For H_THRMTRIP# to SB.	EE
		59	12,20,24	Change to close line: R115, R246, R182, R158, R159, R170.	No need 0 ohm R.	EE
		60	37	Remove L21.	No need L21.	EE
09/09		61	19	Staff R453, C511 ; DY C521.	Follow Intel DG 2.0.	EE
09/10		62	04	Short RN42, RN43, RN44, RN45, RN48, RN22, RN23, RN54, RN53, RN52, RN51.	No need 0 ohm R.	EE
		63	21	Add dummy R510 and C568. Staff R282 0 ohm.	For U34 power bounce issue.	EE
09/22		64	04	Dummy R196.	For debug. Normally, no need it.	EE
		65	25	R82 change to 10k ; R78 change to 2.37k.	For T8 thermal shutdown setting.	EE
		66	23	Staff R288 ; Dummy R289.	For Audio amp. gain.	EE
10/02		67	21	Dummy R284, C318. Staff R282 to Bead 68.00082.531. Staff R510 to 2.2K ; Staff C568.	For U34 power bounce issue.	EE

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Title: Change List - EE (2/2)

Size: A3 | Document Number: Roberts | Rev: A00

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DATE	VERSON	NO	PAGE	Modified List	Issue Description	OWNER
06/03	X01	1	32	R189 change to 2.2K ohm, C216 dummy.	For +1.5V_RUN sequence.	Power EE
		2	30	C378 change to 0.01uF.	For +1.05V_VCCP sequence.	Power EE
		3	34	C316 change from 4.7nF to 0.01uF.	For +3.3V_RUN sequence and improve +3.3V_ALW voltage drop due to SW(U31) turn on quickly (higher loading).	Power EE
		4	34	Staff C314 and change from 4.7nF to 6.8nF.	For +5V_RUN sequence and improve +5V_ALW voltage drop due to SW(U30) turn on quickly (higher loading).	Power EE
06/05		5	36	Dummy Q20, U57, R462, R457, C527 and U58, U28, R251, R252, C293, C295 Change R258, R256 to G81, G82 Change R278, R279, R277, R276 to G83, G84, G85, G86	No sniffer function, no control HDD & ODD power.	Power EE
06/06		6	27	R136 change to 270k and R108 change to 237k	For 5V/3.3V OCP	Power EE
		7	28	R38 change to 12.1k R323 change to 3.92k , C360 change to 0.047 uF 10V X7R	R38 for VCORE OCP R323 and C360 for transient and load line.	Power EE
		8	31	PC9 to GND.	PC9 to GND otherwise DC-DC IC can not obtain power to generate 1.8V/0.9V output.	Power EE
		9	31	PR2 change to 9.31k ohm.	For 1.8V OCP.	Power EE
		10	30	Add D23.	For power sequence.	Power EE
06/10		11	18,24	Remove U60, R482, R476 and change trace name VRMPWRGD to VGATE_PWRGD.	For power sequence.	Power EE
06/18		12	31	PR7.1 link to +5116_PWR_SRC.	Reserve for other source.	Power EE
06/23		13	30	Rename "+1.05V_SUSP" to "+1.05V_RUNP"	Correct naming.	Power EE
		14	26,45	Material change: U37, U46, U47.	NIKO-SEM P2003EVG component has some risk.	Power EE
07/30	X02	15	31	Change PR7 value from 622k to 619k ohm.	For 2nd source.	Power EE
08/11		16	26,45	Material change: U37, U46, U47.	Power team request.	Power EE
09/03	A00	17	26,27, 28,31	Change to close line: R46 ,R137 ,R127,R106 ,R384 ,R391 ,R35 ,R29 ,R307 ,R308 ,R309 ,R303 ,R304 , R298 ,R301 ,R310 ,R313 ,PR14.	No need 0 ohm R.	Power EE
		18	26	R61 change 4.7k to 10k.	Power team request.	Power EE
XX		19				
XX		20				
		21				
		22				
XX		23	x	x	x	Power EE
XX		24	x	x	x	Power EE
		25	x	x	x	Power EE

<Core Design>

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