

ZZZ8
DAZ@
DAZ04300100
PCB

ZZZ1
DA2@
MAIN BOARD
DA600007E10
PCB

ZZZ2
DA2@
E board
DA40000A910
PCB

ZZZ3
DA2@
FP board
DA600007D10
PCB

ZZZ4
DA2@
Function board
DA40000AA10
PCB

ZZZ5
DA2@
USB board
DA40000AB10
PCB

ZZZ6
DA2@
IO board
DA40000AC10
PCB

ZZZ7
DA2@
Power board
DA40000AD10
PCB

Compal Confidential

JAT10 M/B Schematics Document

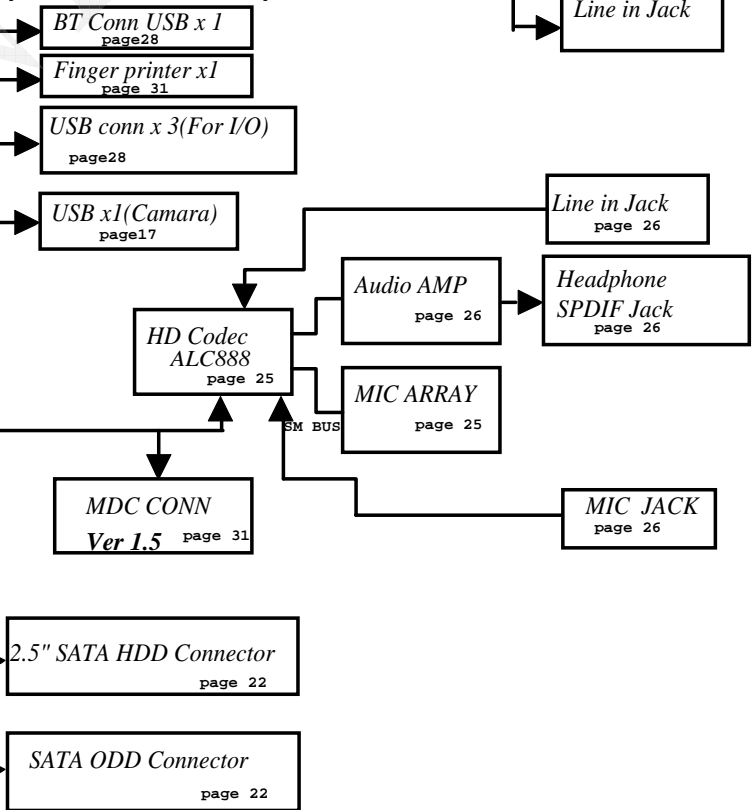
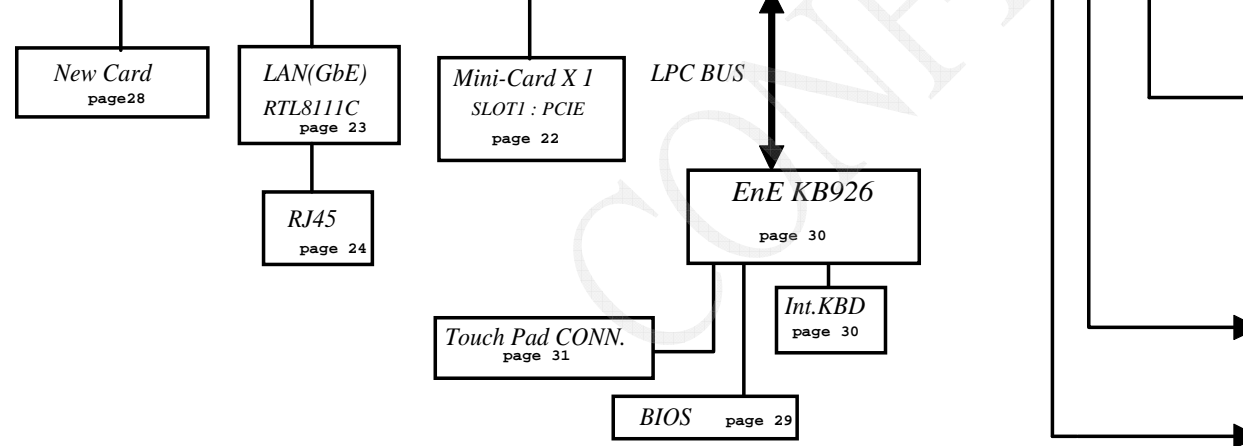
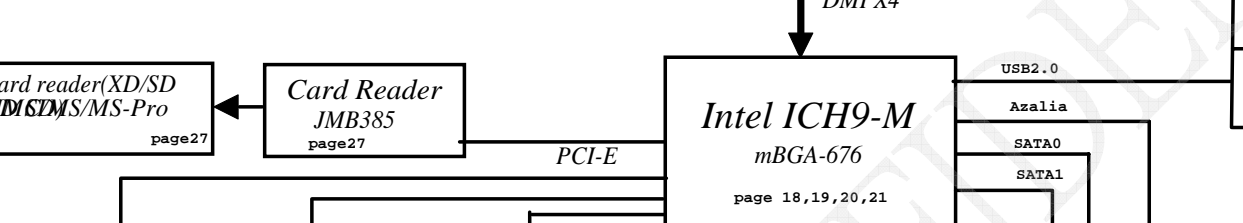
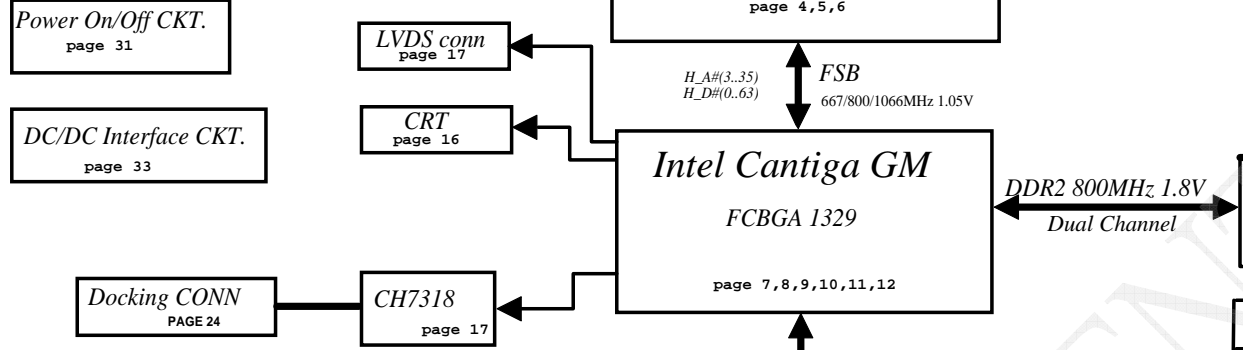
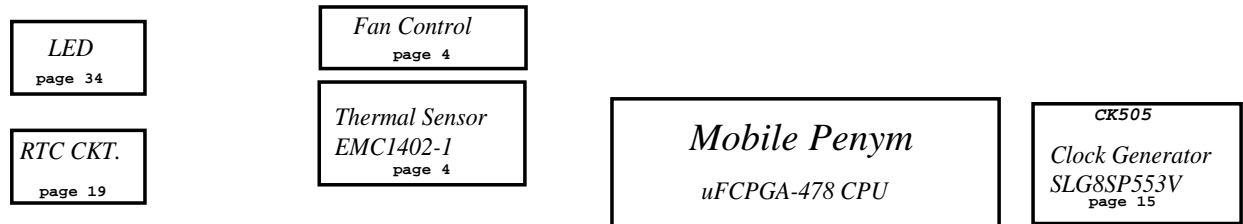
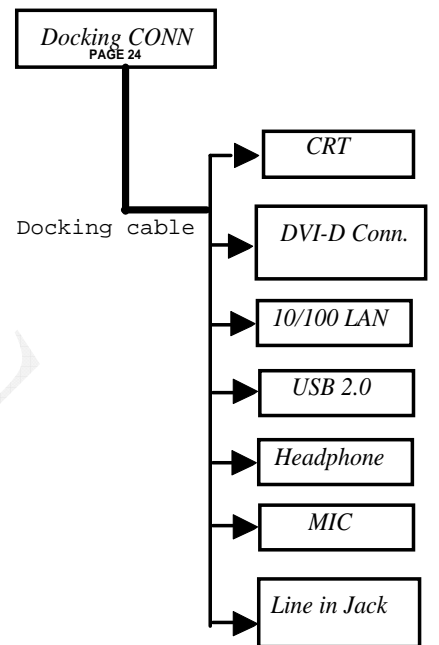
Intel Penryn Processor with Cantiga + DDRII + ICH9M

2008-04-07

REV:1.0

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				42	B

Voltage Rails O MEANS ON X MEANS OFF

power plane State		+5VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE
	+B	+3VALW		+1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

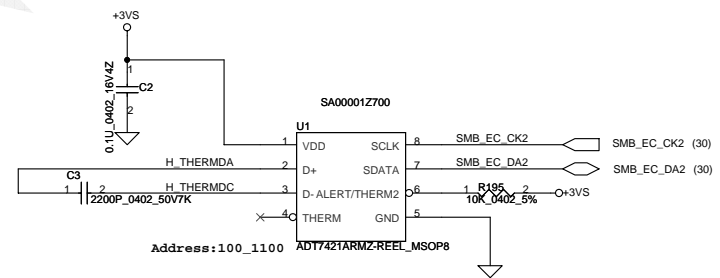
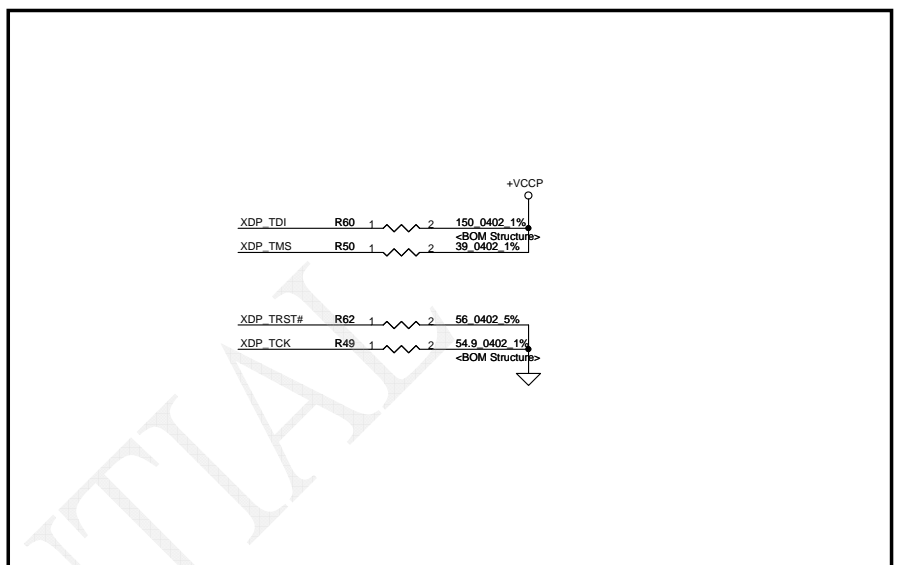
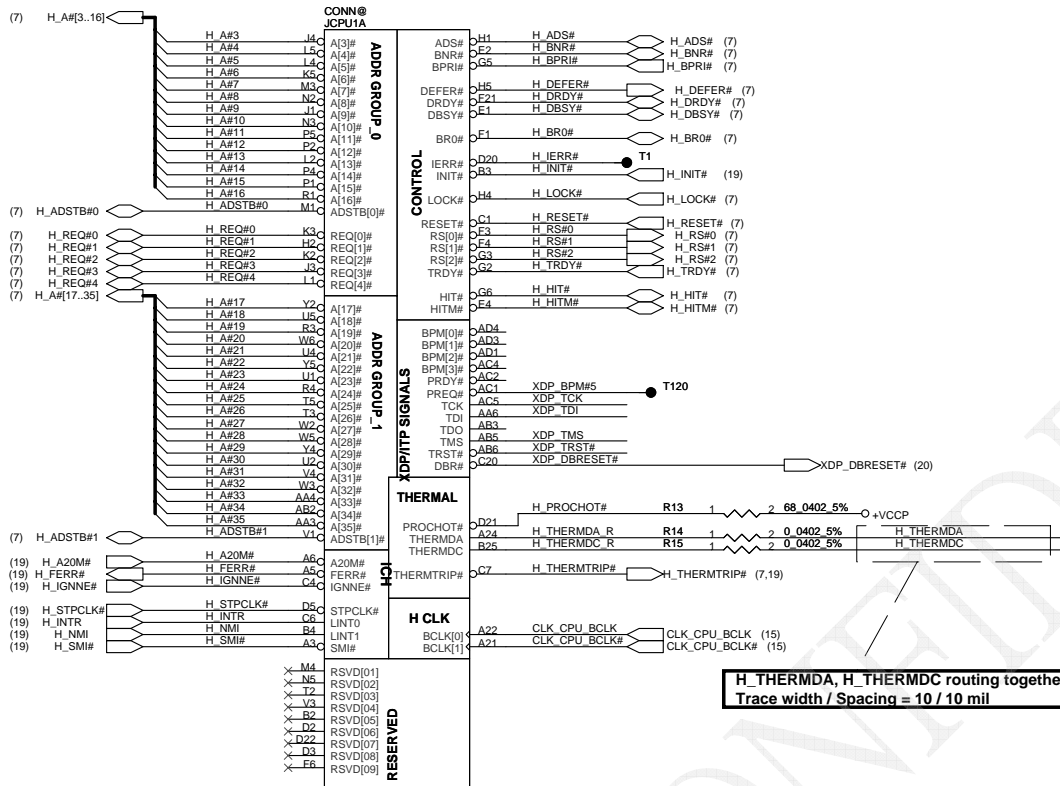
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

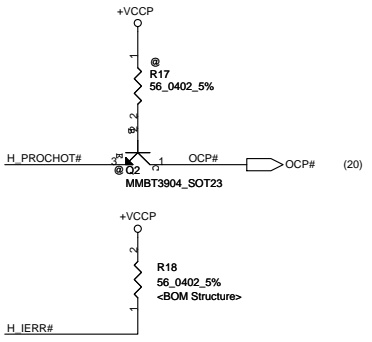
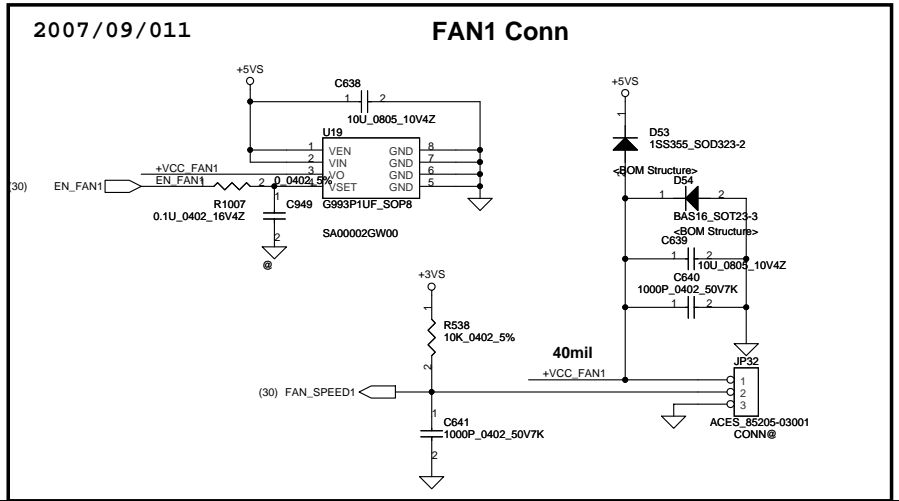
I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

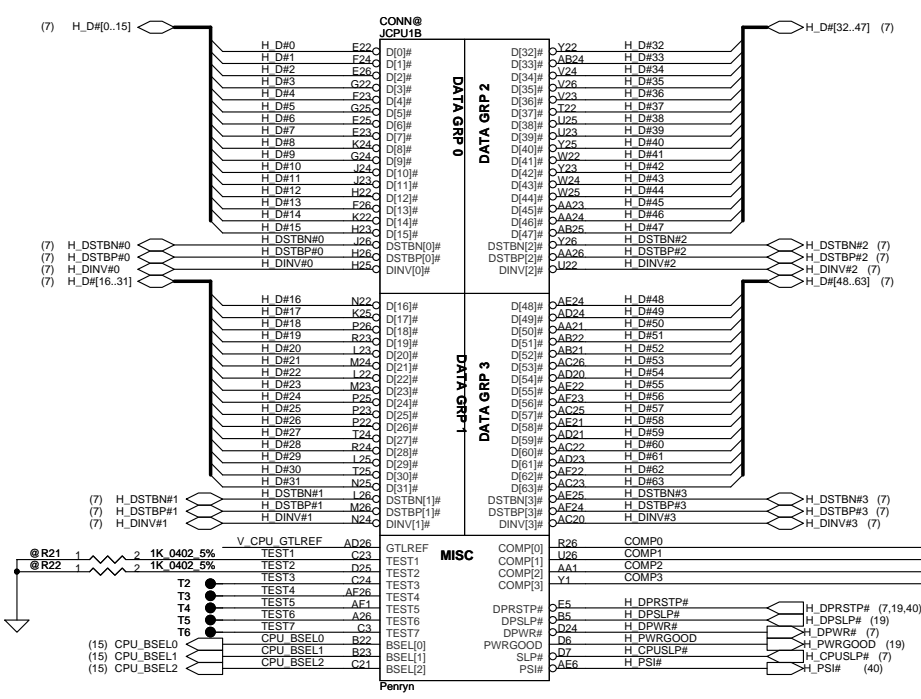
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H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

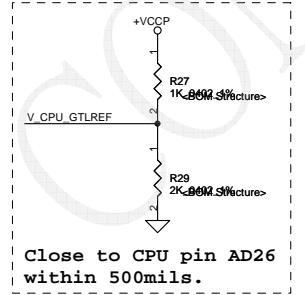


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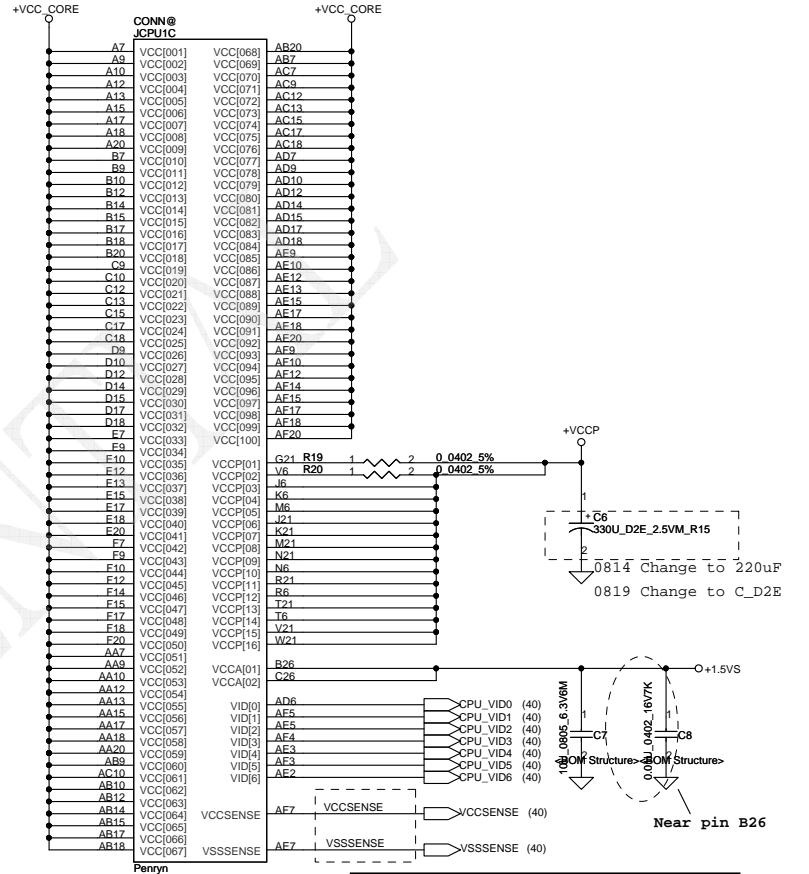


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

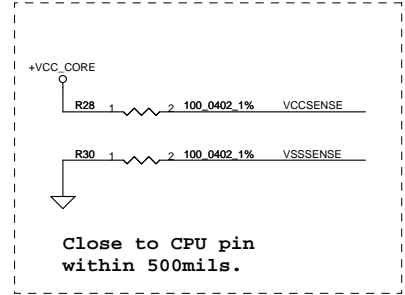
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0



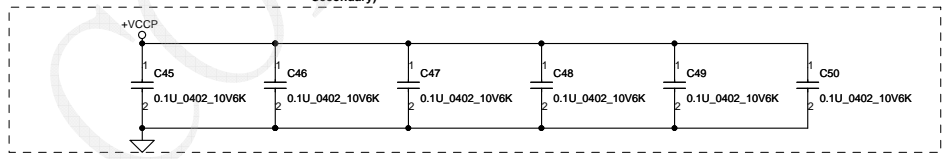
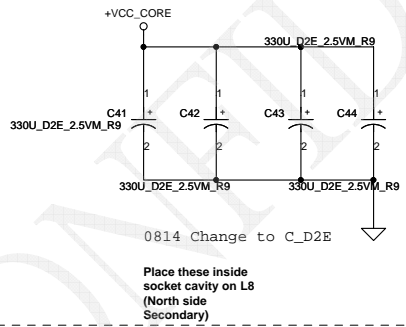
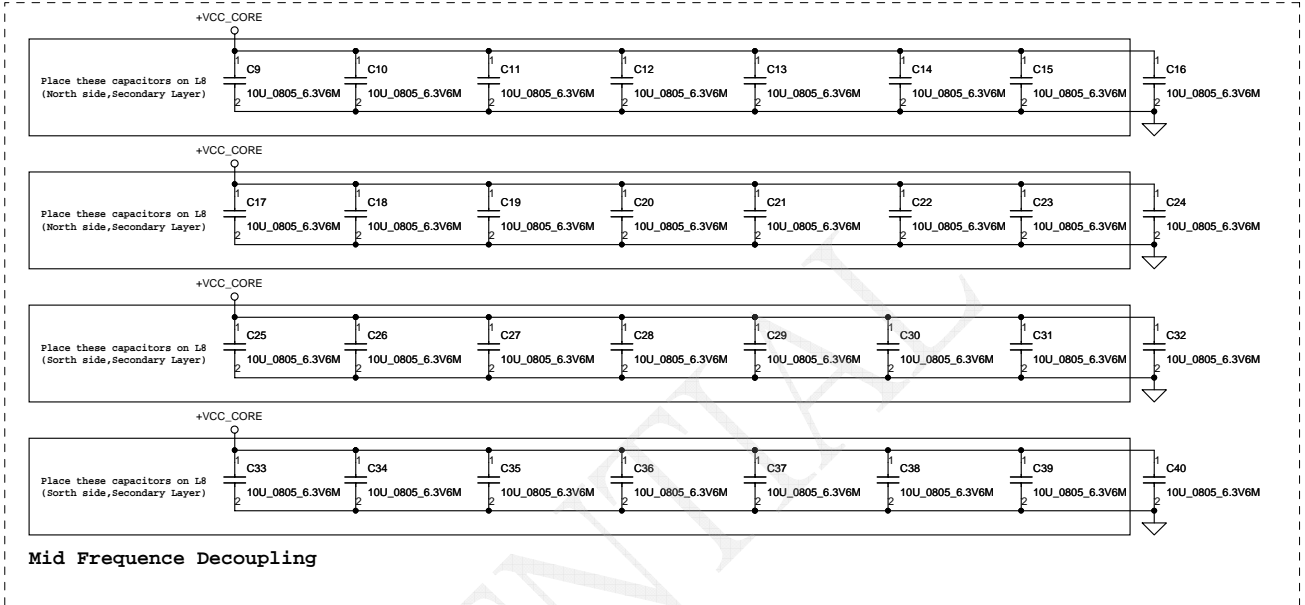
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



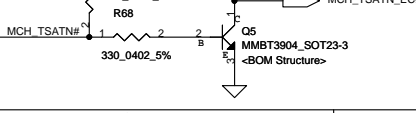
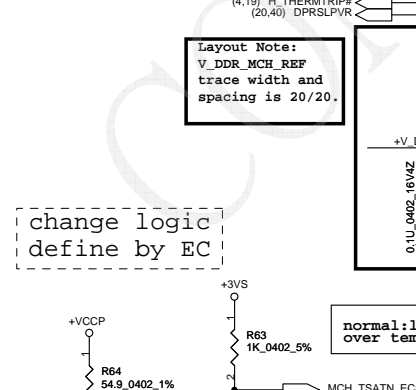
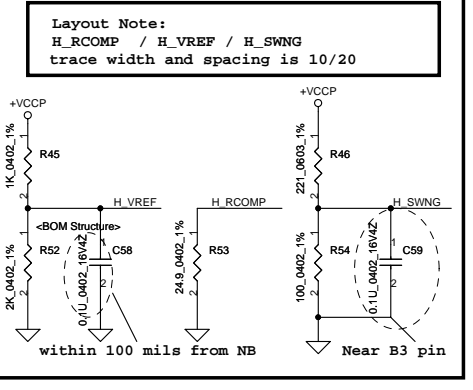
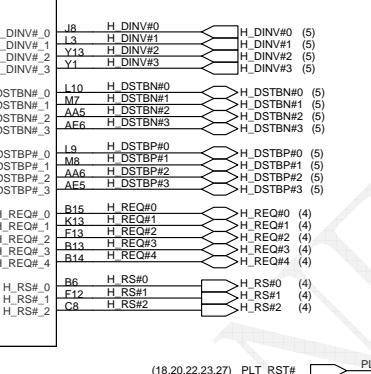
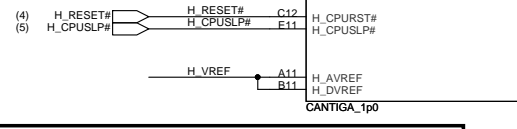
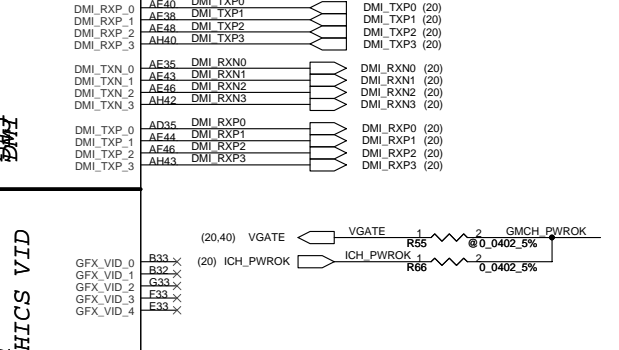
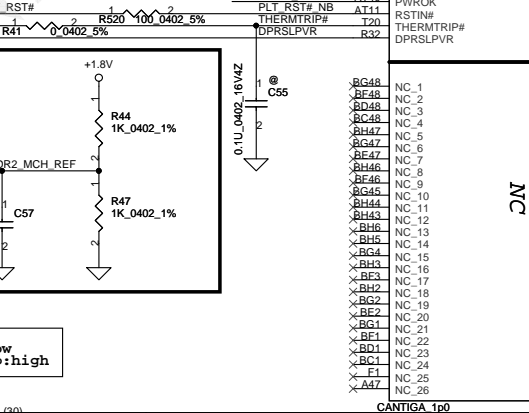
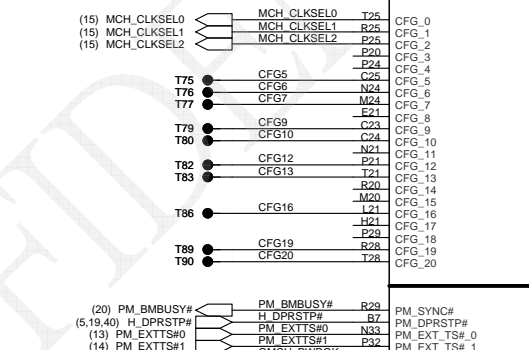
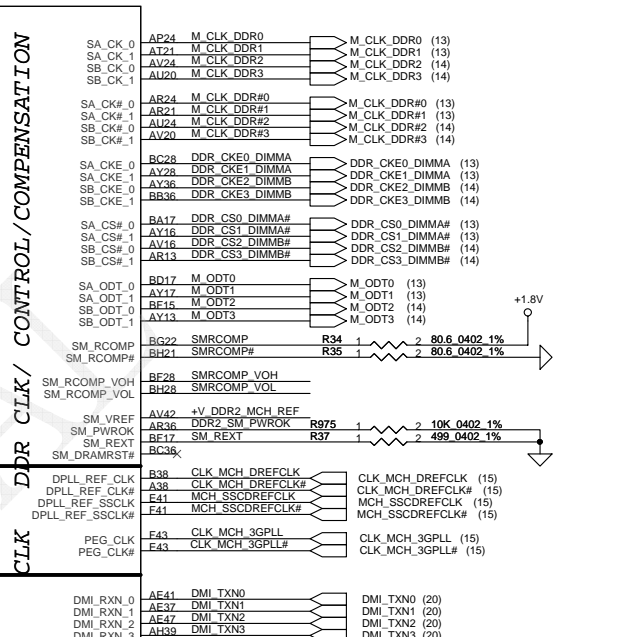
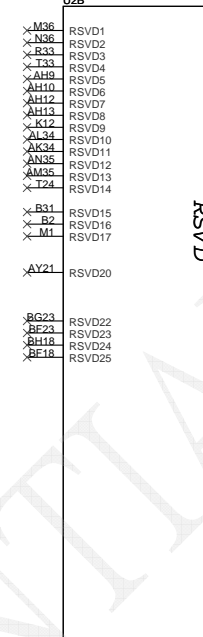
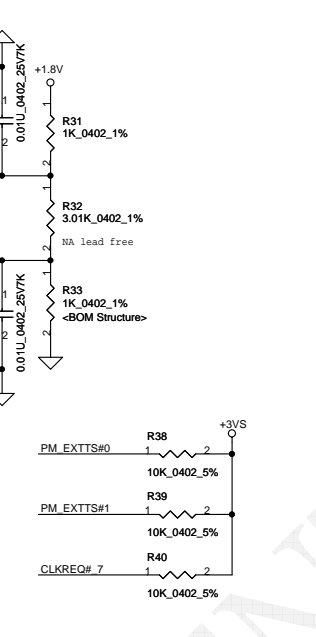
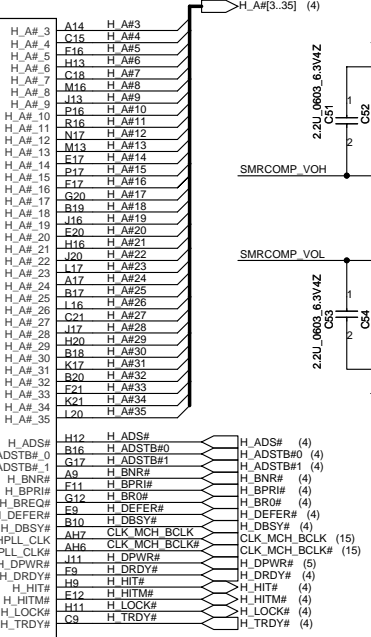
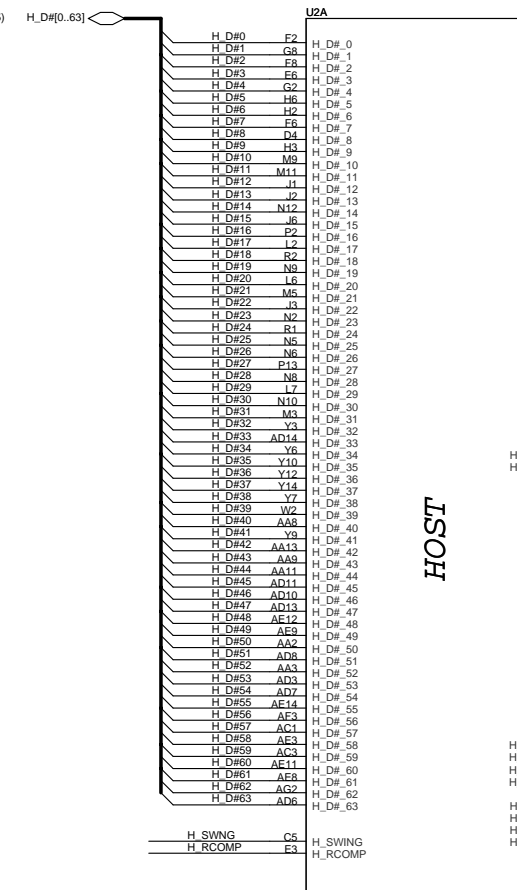
Length match within 25 mils. The trace width/space/other is 20/7/25.



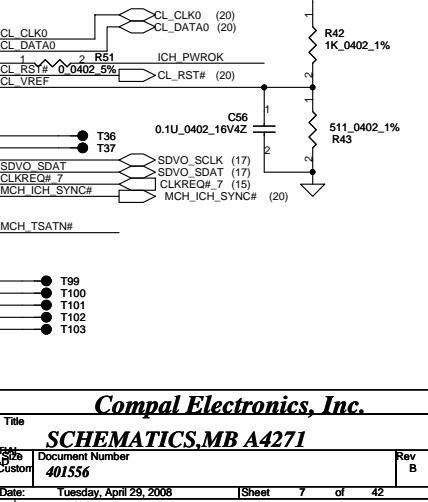
CONN#			ICPLUID		
A4	VSS001	VSS082	P6		
A8	VSS002	VSS083	P21		
A11	VSS003	VSS084	P24		
A14	VSS004	VSS085	R5		
A16	VSS005	VSS086	R22		
A19	VSS006	VSS087	R25		
A23	VSS007	VSS088	T1		
AE2	VSS008	VSS089	T4		
BE	VSS009	VSS090	T23		
B8	VSS010	VSS091	T26		
B11	VSS011	VSS092	U3		
B13	VSS012	VSS093	U6		
B16	VSS013	VSS094	U21		
B19	VSS014	VSS095	U24		
B21	VSS015	VSS096	V2		
B24	VSS016	VSS097	V5		
C5	VSS017	VSS098	V22		
C8	VSS018	VSS099	V25		
C11	VSS019	VSS100	W1		
C14	VSS020	VSS101	W4		
C16	VSS021	VSS102	W23		
C19	VSS022	VSS103	W26		
C2	VSS023	VSS104	Y3		
C22	VSS024	VSS105	Y6		
C25	VSS025	VSS106	Y21		
D1	VSS026	VSS107	Y24		
D4	VSS027	VSS108	AA2		
DR	VSS028	VSS109	AA5		
D11	VSS029	VSS110	AA8		
D16	VSS030	VSS111	AA11		
D19	VSS031	VSS112	AA14		
D23	VSS032	VSS113	AA16		
D26	VSS033	VSS114	AA19		
E3	VSS034	VSS115	AA22		
E6	VSS035	VSS116	AA25		
FR	VSS036	VSS117	AB1		
FR	VSS037	VSS118	AB4		
F11	VSS038	VSS119	AB8		
F14	VSS039	VSS120	AB11		
F16	VSS040	VSS121	AB13		
F19	VSS041	VSS122	AB16		
E21	VSS042	VSS123	AB19		
E24	VSS043	VSS124	AB23		
F6	VSS044	VSS125	AB26		
FR	VSS045	VSS126	AC3		
F11	VSS046	VSS127	AC6		
F14	VSS047	VSS128	AC8		
F16	VSS048	VSS129	AC14		
F19	VSS049	VSS130	AC16		
F2	VSS050	VSS131	AC19		
F25	VSS051	VSS132	AC21		
F22	VSS052	VSS133	AC24		
G4	VSS053	VSS134	AD2		
G1	VSS054	VSS135	AD5		
G26	VSS055	VSS136	AD8		
H3	VSS056	VSS137	AD11		
HR	VSS057	VSS138	AD13		
H21	VSS058	VSS139	AD16		
H24	VSS059	VSS140	AD19		
J2	VSS060	VSS141	AD22		
J5	VSS061	VSS142	AD25		
J2	VSS062	VSS143	AE1		
J25	VSS063	VSS144	AE4		
K1	VSS064	VSS145	AE8		
K4	VSS065	VSS146	AE11		
K23	VSS066	VSS147	AE14		
K26	VSS067	VSS148	AE16		
L3	VSS068	VSS149	AE19		
L6	VSS069	VSS150	AE23		
L21	VSS070	VSS151	AE26		
L24	VSS071	VSS152	A2		
M2	VSS072	VSS153	AE6		
L24	VSS073	VSS154	AE8		
M5	VSS074	VSS155	AE11		
M22	VSS075	VSS156	AE13		
N1	VSS076	VSS157	AE16		
N4	VSS077	VSS158	AE19		
N23	VSS078	VSS159	AE21		
N26	VSS079	VSS160	AE25		
P3	VSS080	VSS161	AE25		
V2	VSS081	VSS162			
V2	VSS081	VSS163			

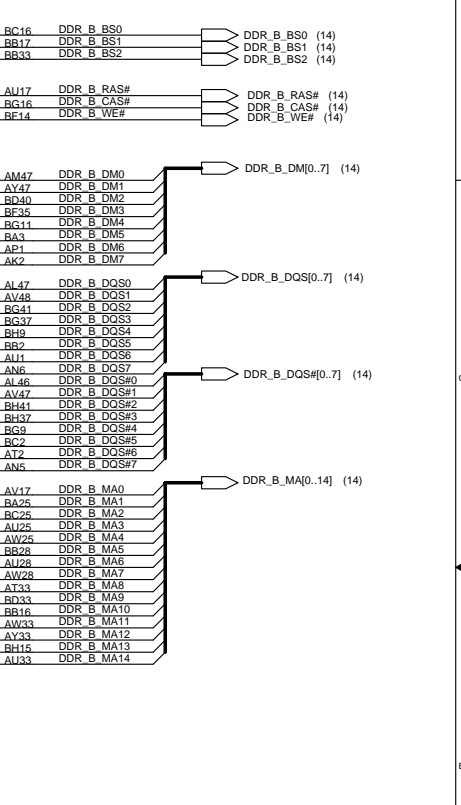
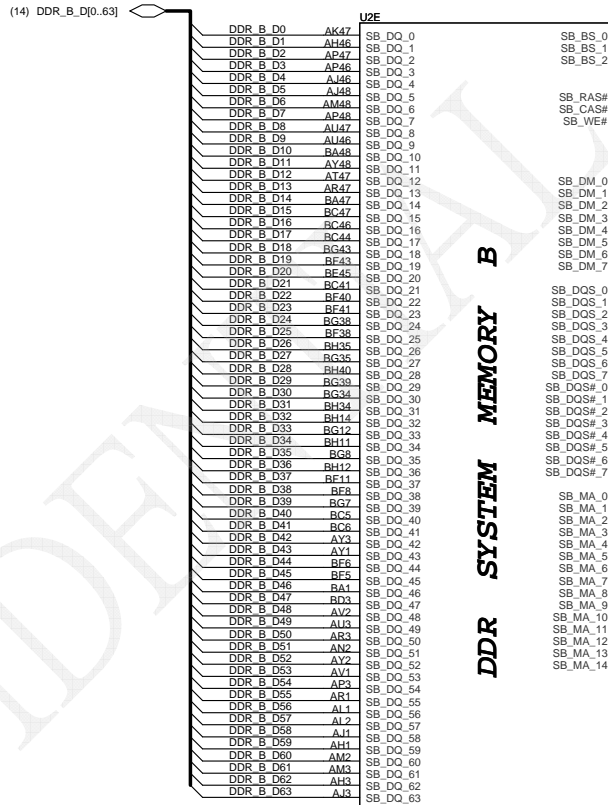
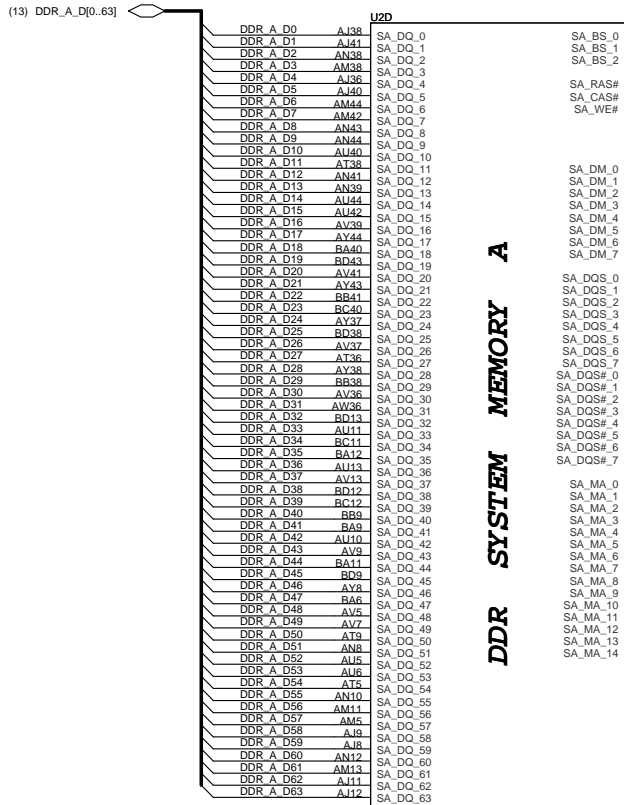


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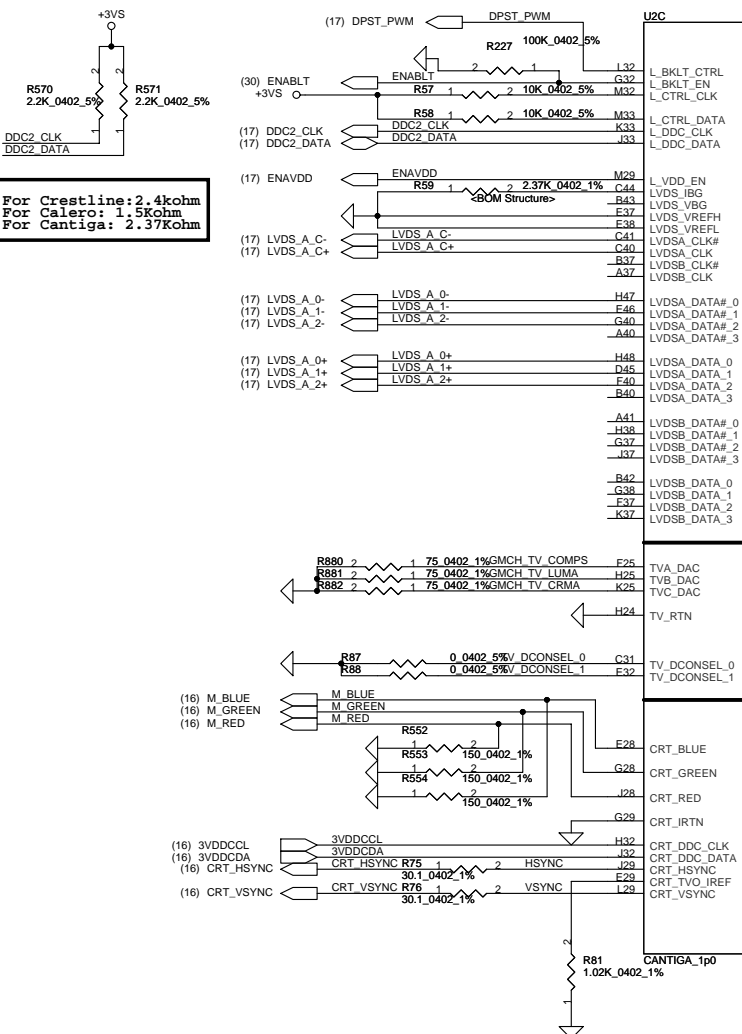


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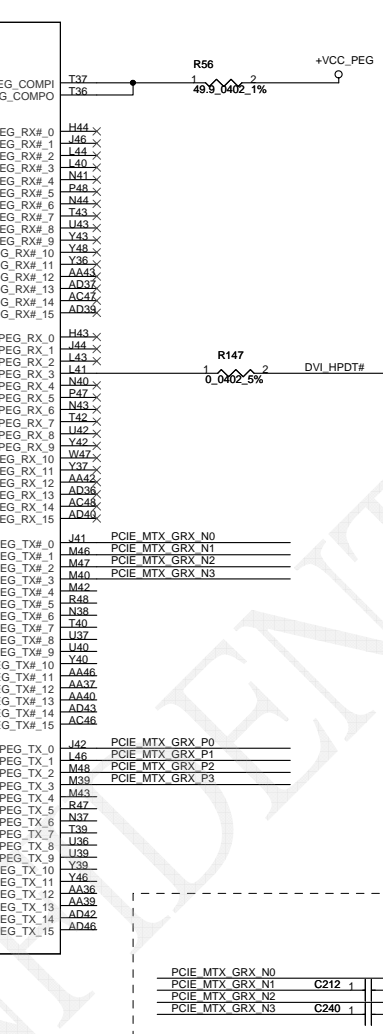
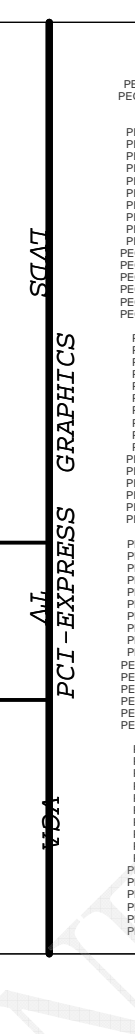




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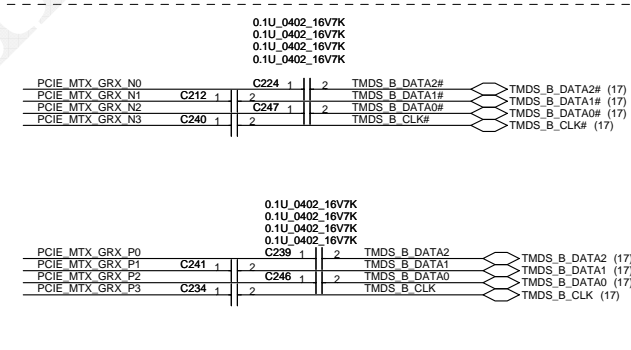


For Crestline: 2.4kOhm
 For Calero: 1.5kOhm
 For Cantiga: 2.37kOhm

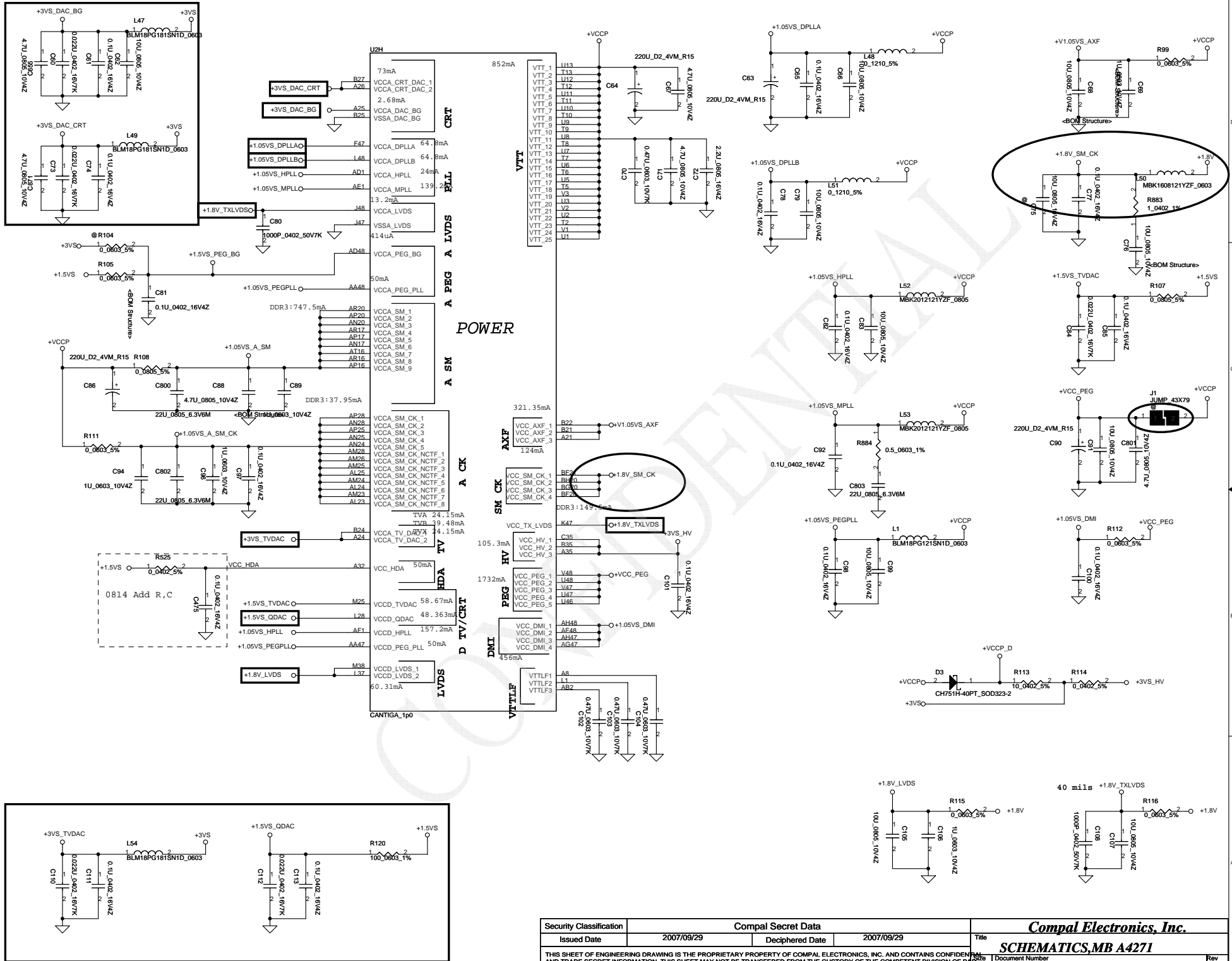


PEGCOMP trace width and spacing is 20/25 mils.

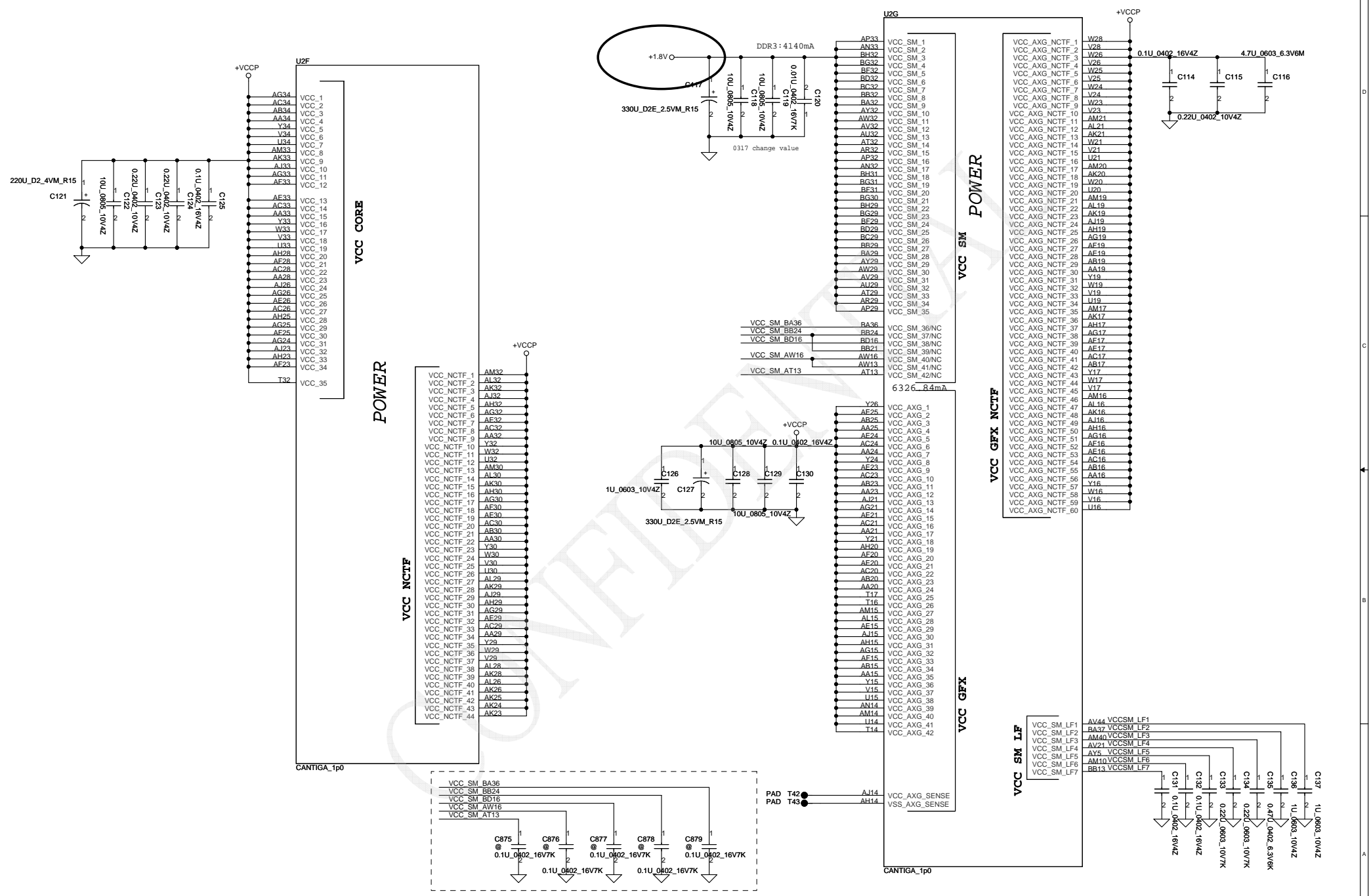
Strap Pin Table	
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 = (TLS)chiper suite with no confidentiality 1 = (TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane, 15->0, 14->1 1 = Normal Operation, Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.



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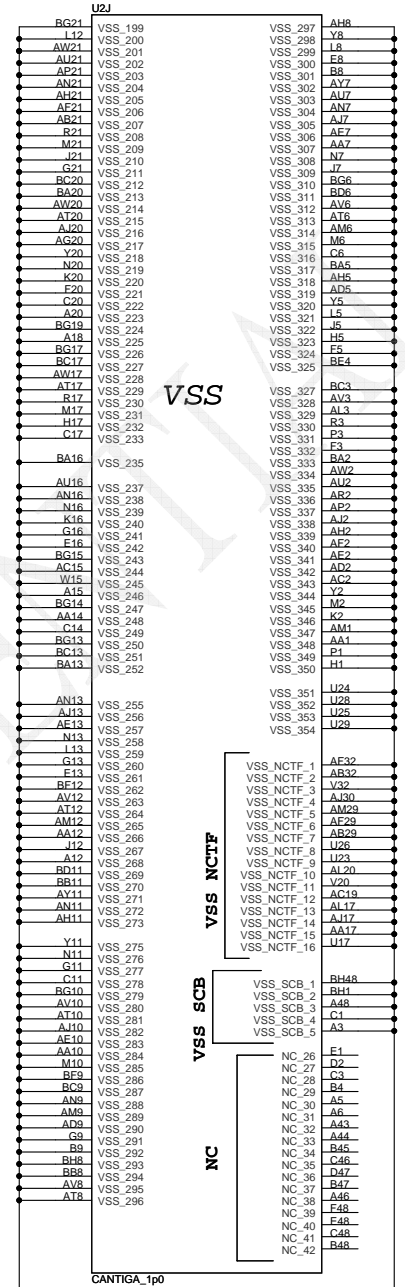
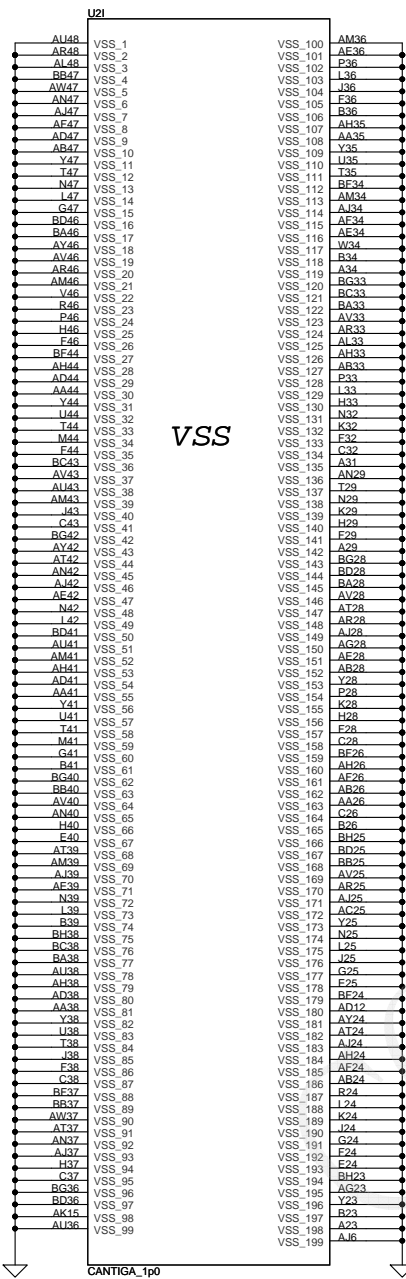


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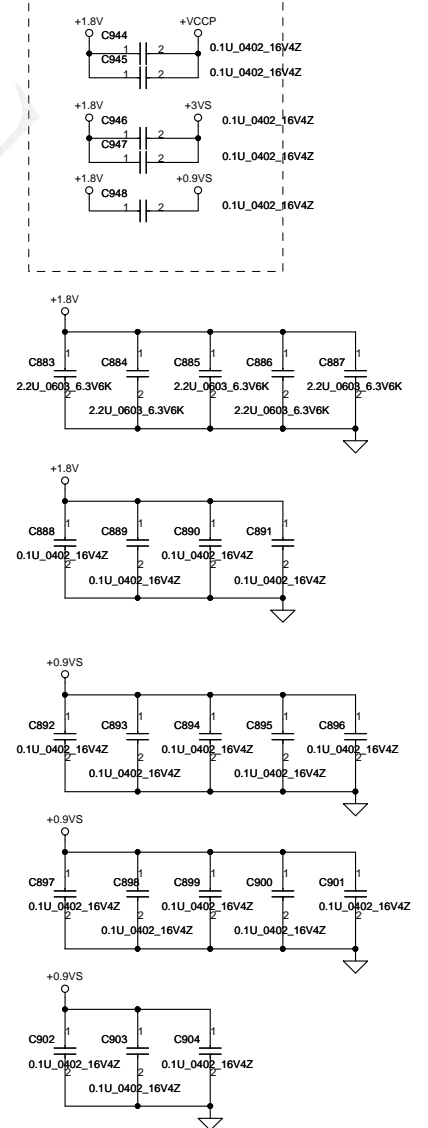
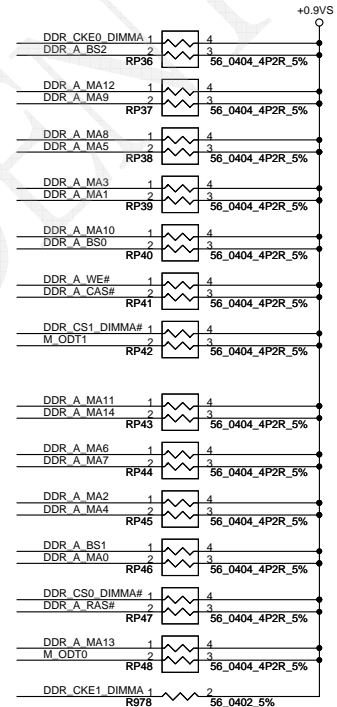
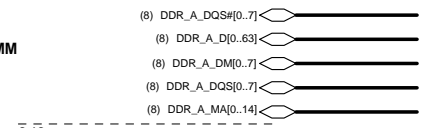
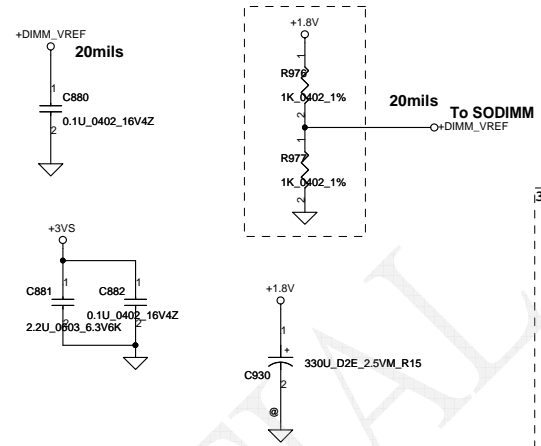
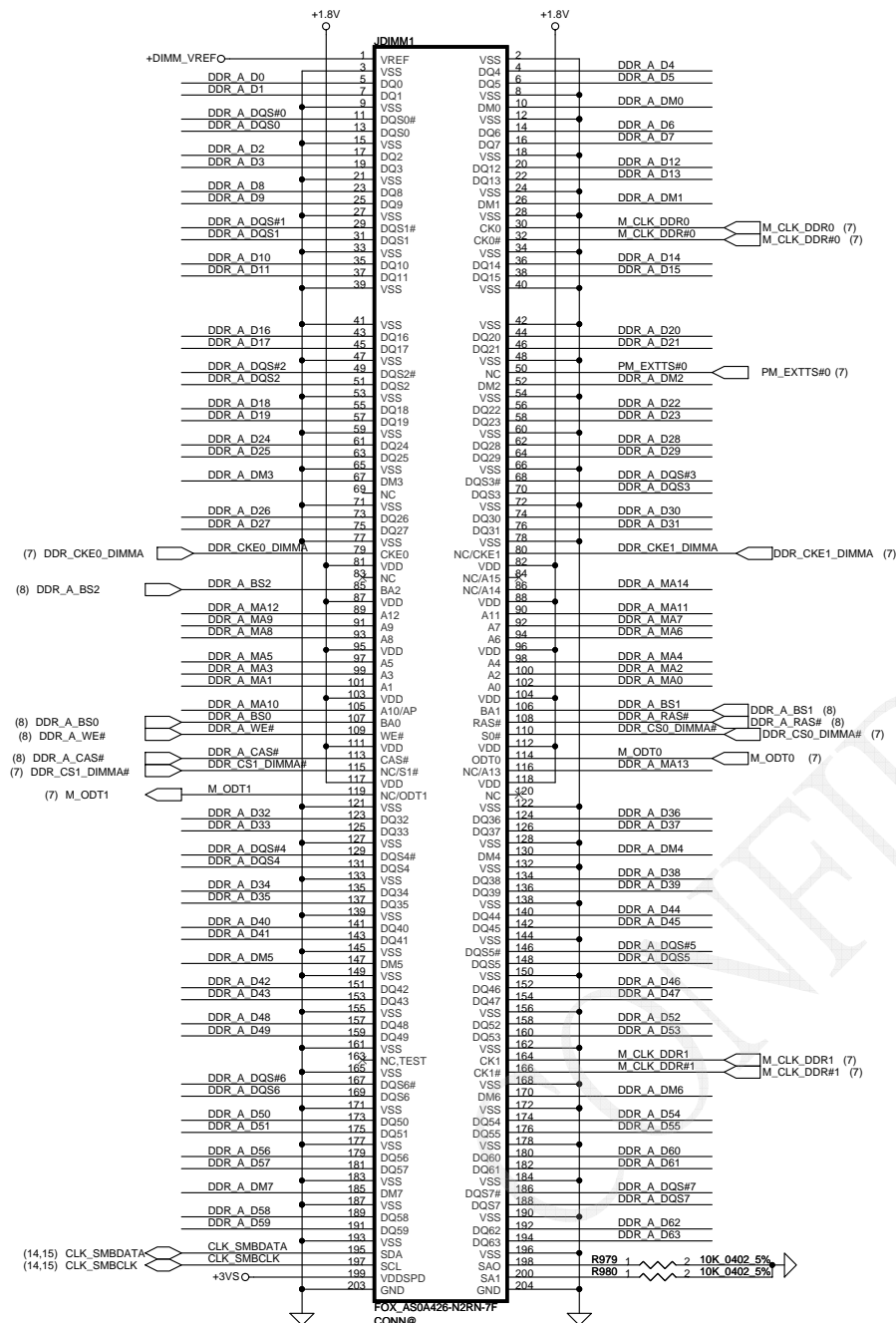


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Compal Electronics, Inc.
SCHEMATICS, MB A4271

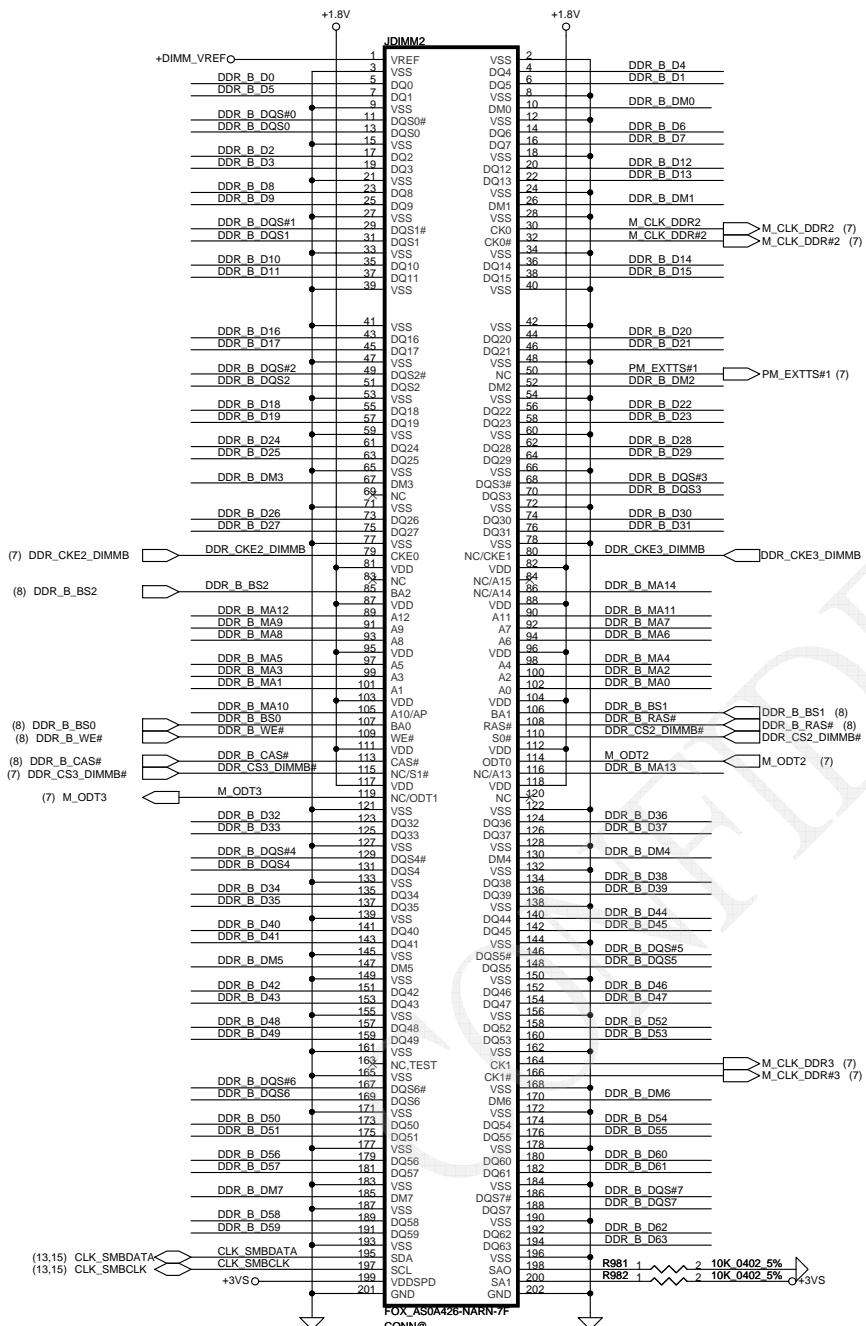


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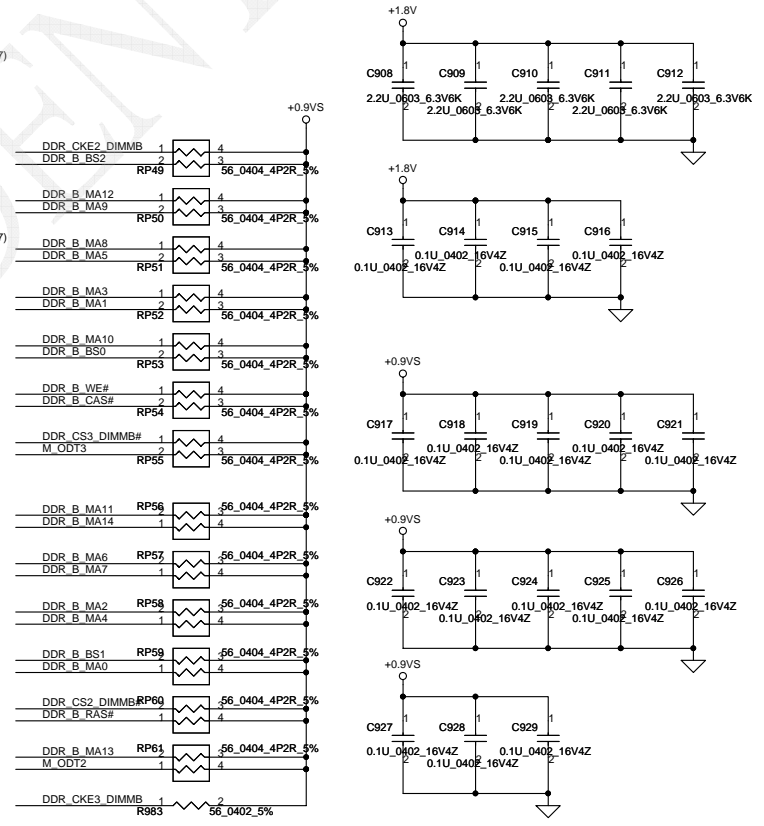
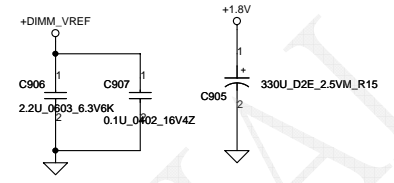


DIMM0 REV H:5.2mm (BOT)

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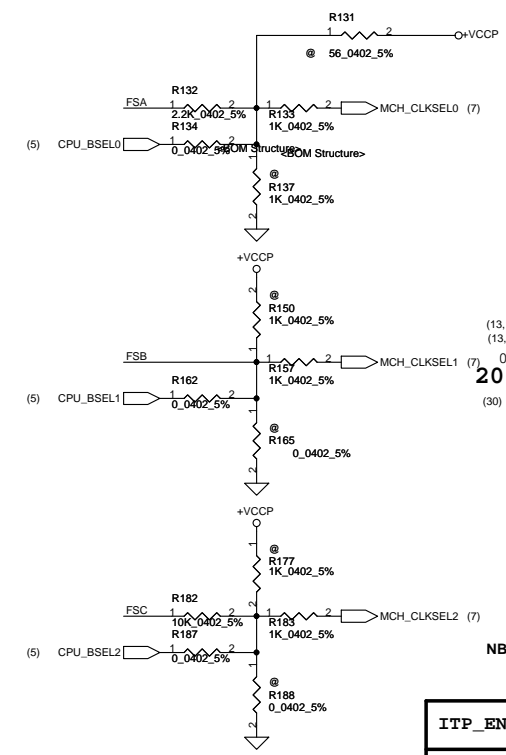
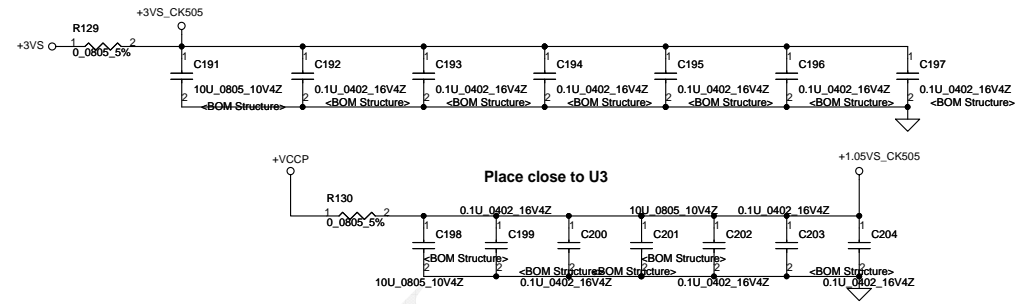
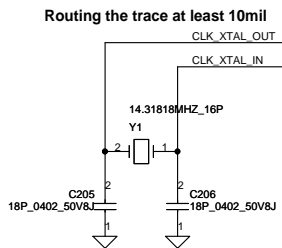
- (8) DDR_B_DQS#[0..7]
- (8) DDR_B_D[0..63]
- (8) DDR_B_DM[0..7]
- (8) DDR_B_DQS[0..7]
- (8) DDR_B_MA[0..14]



DIMM1 REV H:9.2mm (BOT)

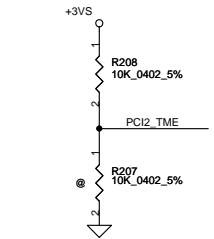
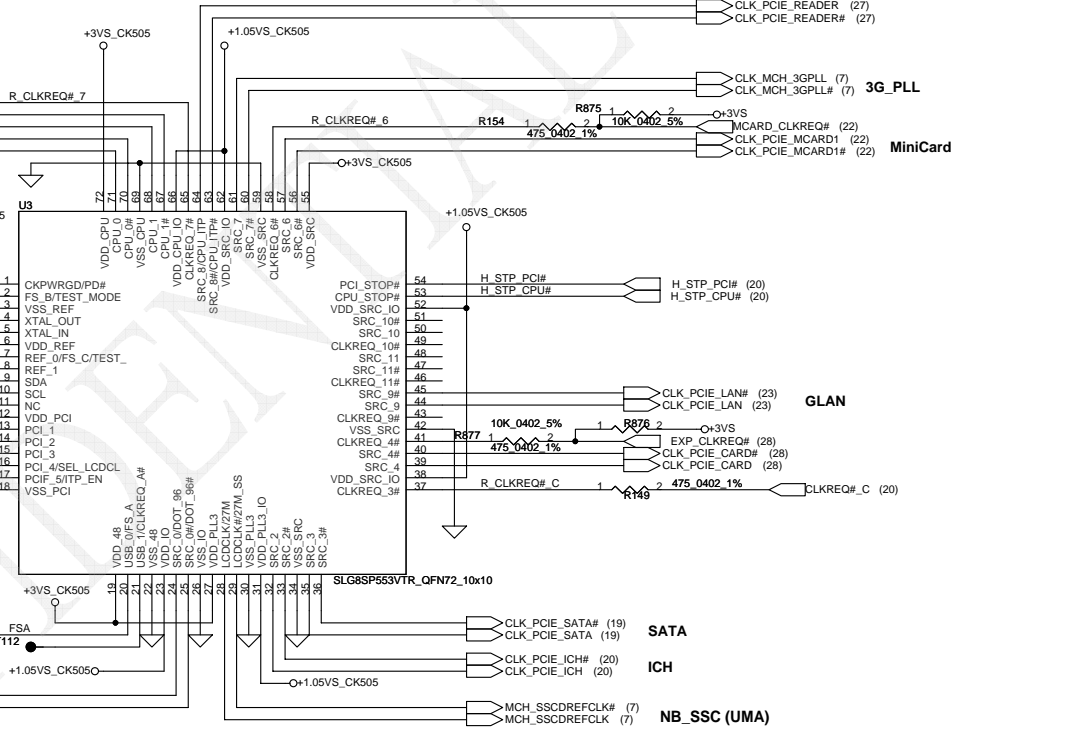
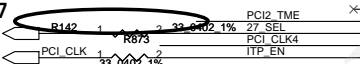
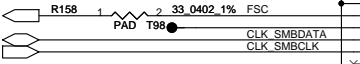
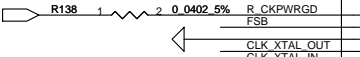
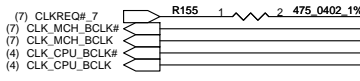
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FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB	
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz	
0	0	0	266	100	33.3	14.318	96.0	48.0	
0	0	1	133	100	33.3	14.318	96.0	48.0	
0	1	0	200	100	33.3	14.318	96.0	48.0	
0	1	1	166	100	33.3	14.318	96.0	48.0	
1	0	0	333	100	33.3	14.318	96.0	48.0	
1	0	1	100	100	33.3	14.318	96.0	48.0	
1	1	0	400	100	33.3	14.318	96.0	48.0	
1	1	1	Reserved						



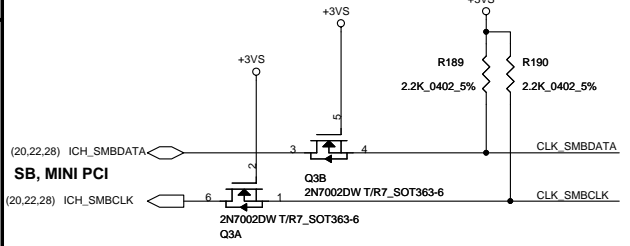
NB CPU

NB (UMA)

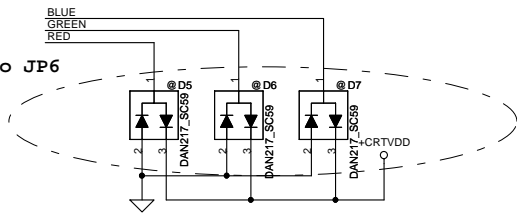
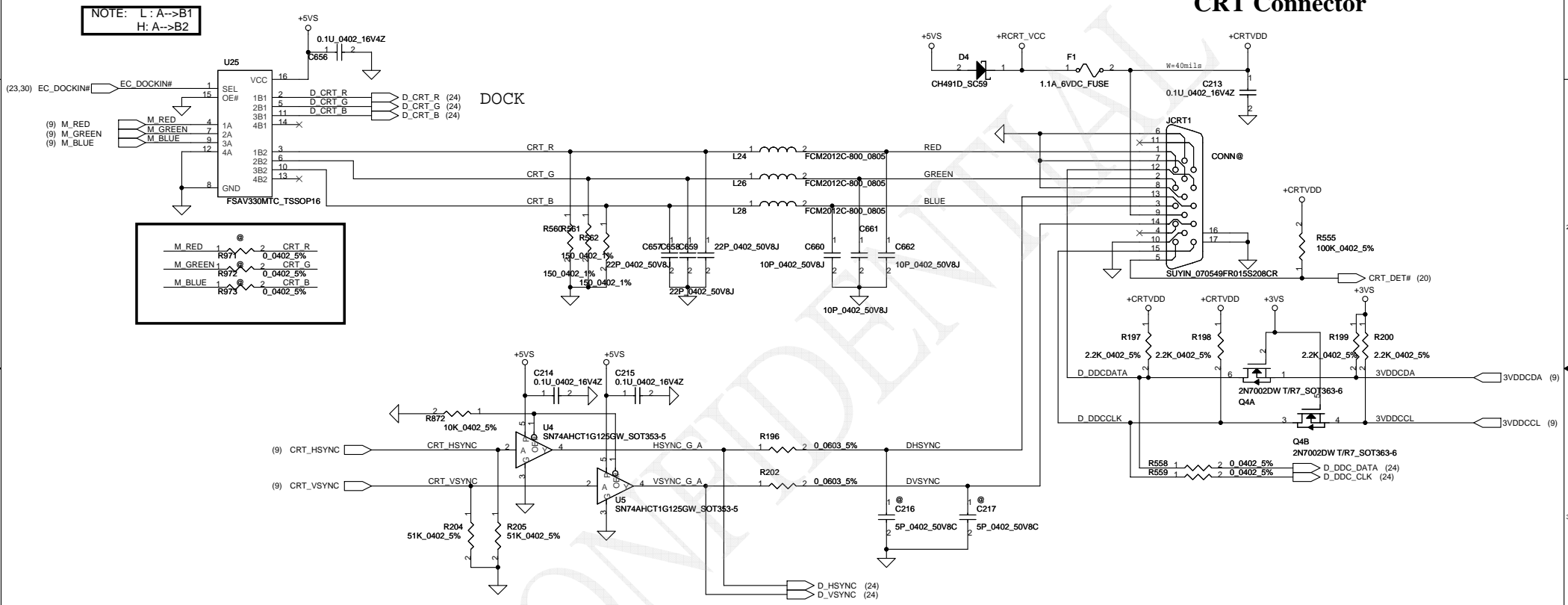


for ICS Overclocking setting
 0=Overclocking of CPU and SRC allowed
 1=Overclocking of CPU and SRC NOT allowed

ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
PCI_CLK3	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)

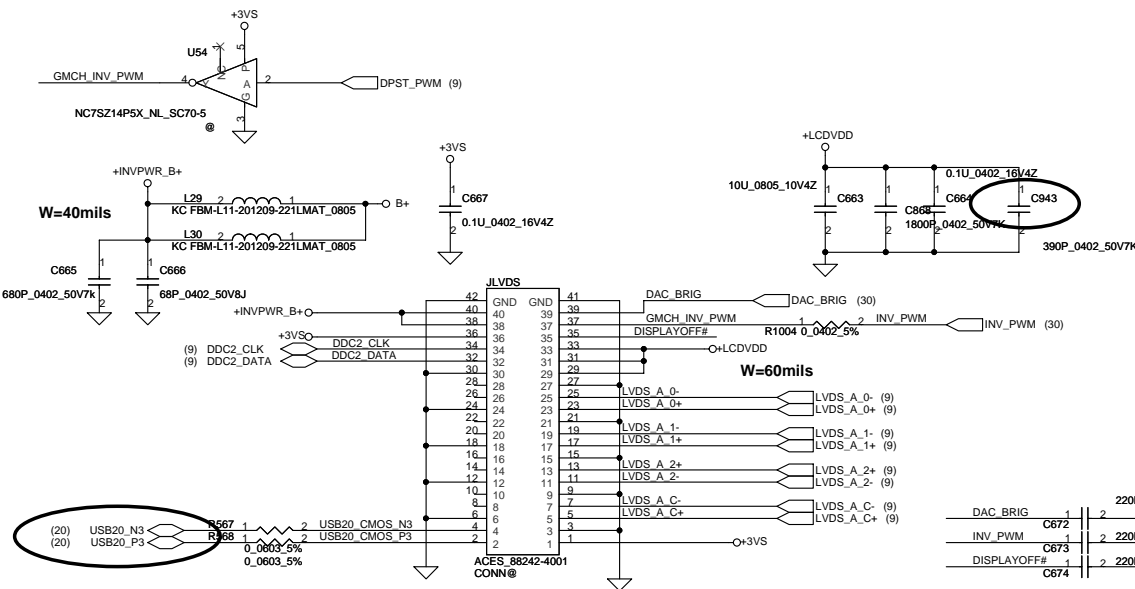


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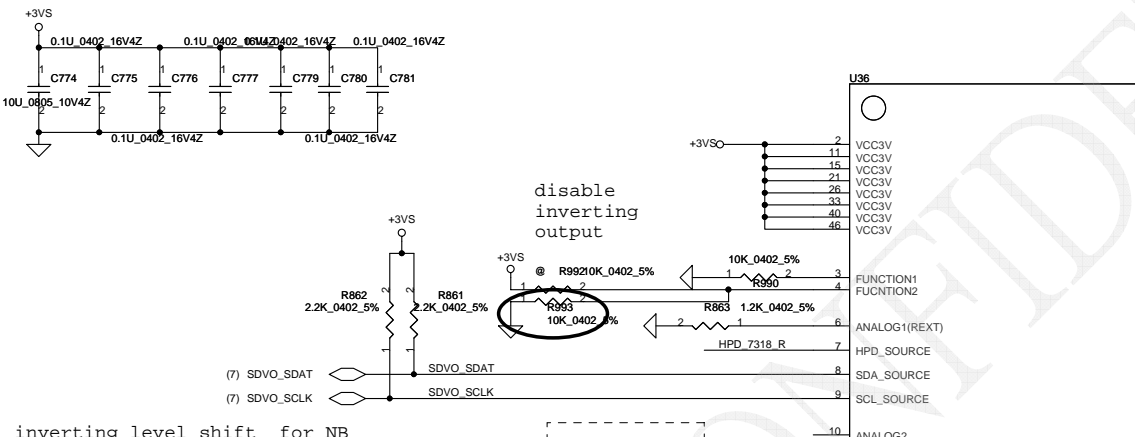
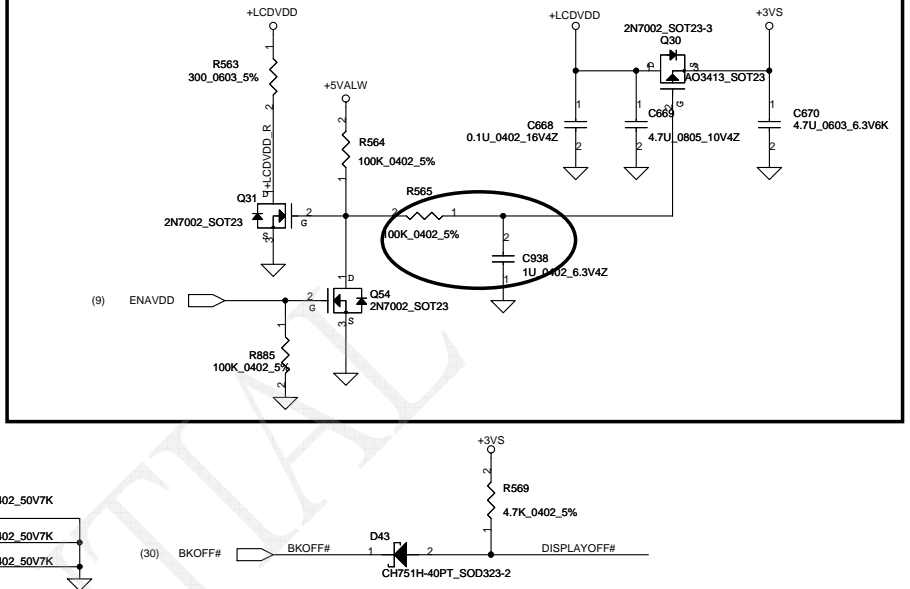


CRT Connector

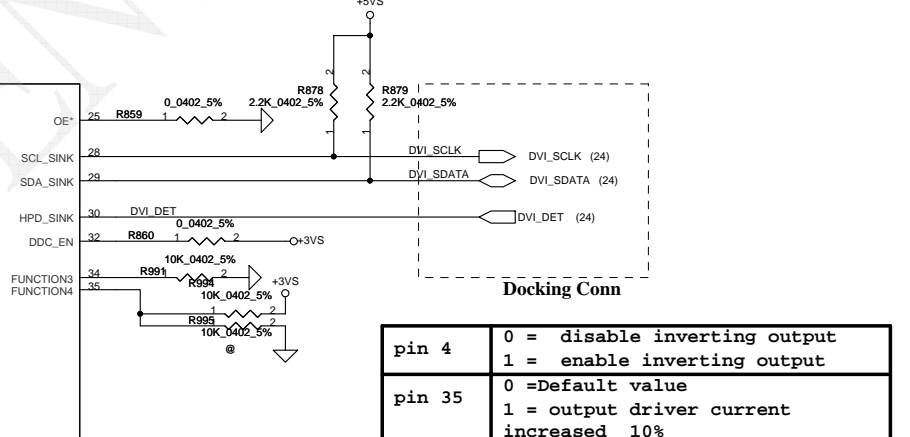
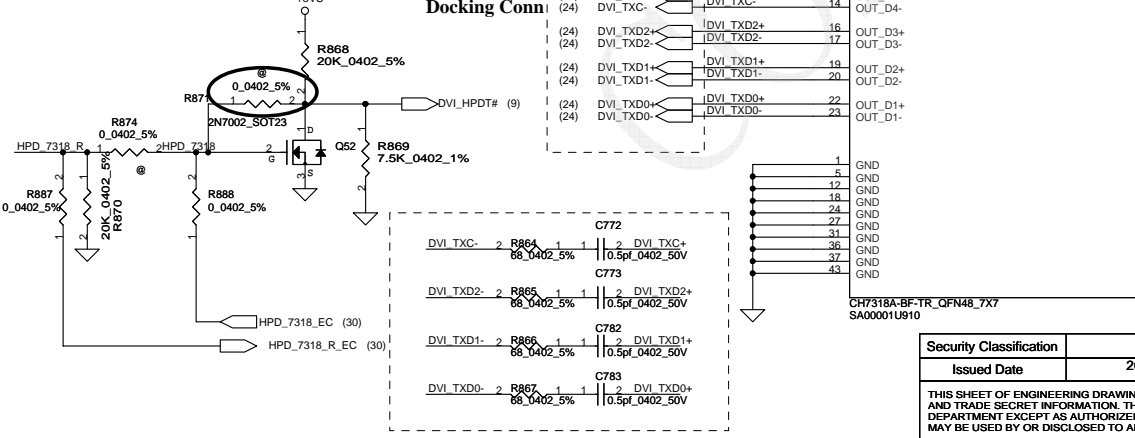
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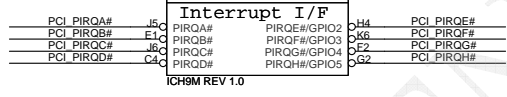
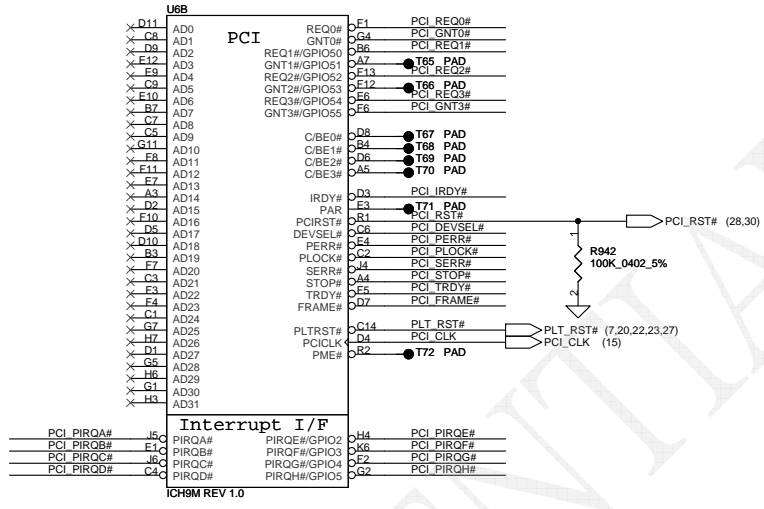
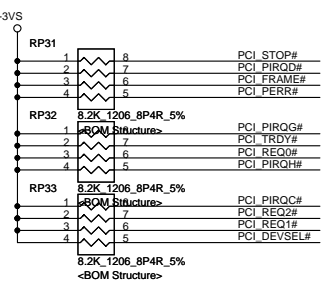
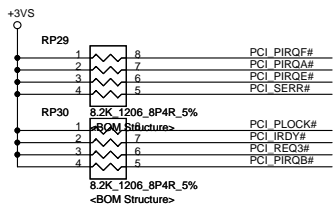
LVDS and USB CAM connector



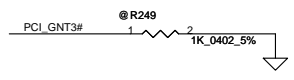
inverting level shift for NB



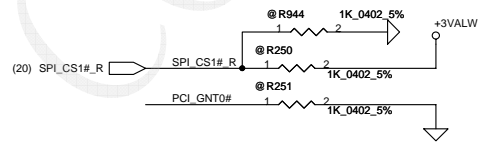
pin 4	0 = disable inverting output 1 = enable inverting output
pin 35	0 = Default value 1 = output driver current increased 10%



A16 swap override Strap
 Low= A16 swap override Enable
 High= Default *



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

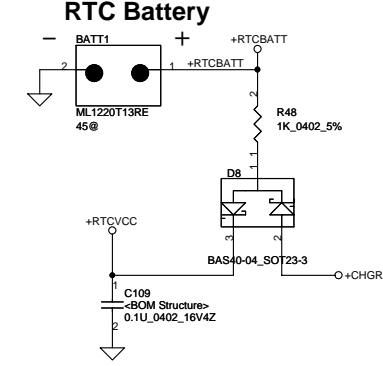
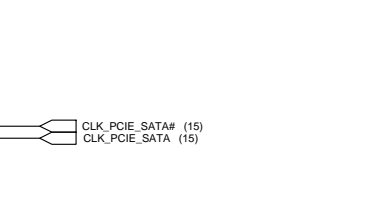
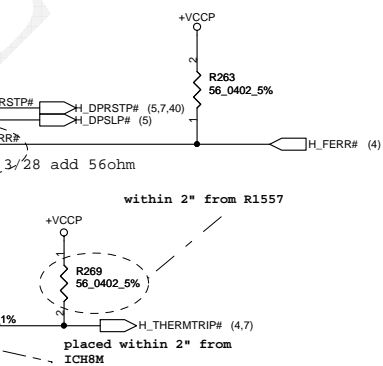
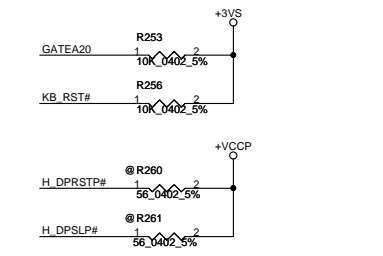
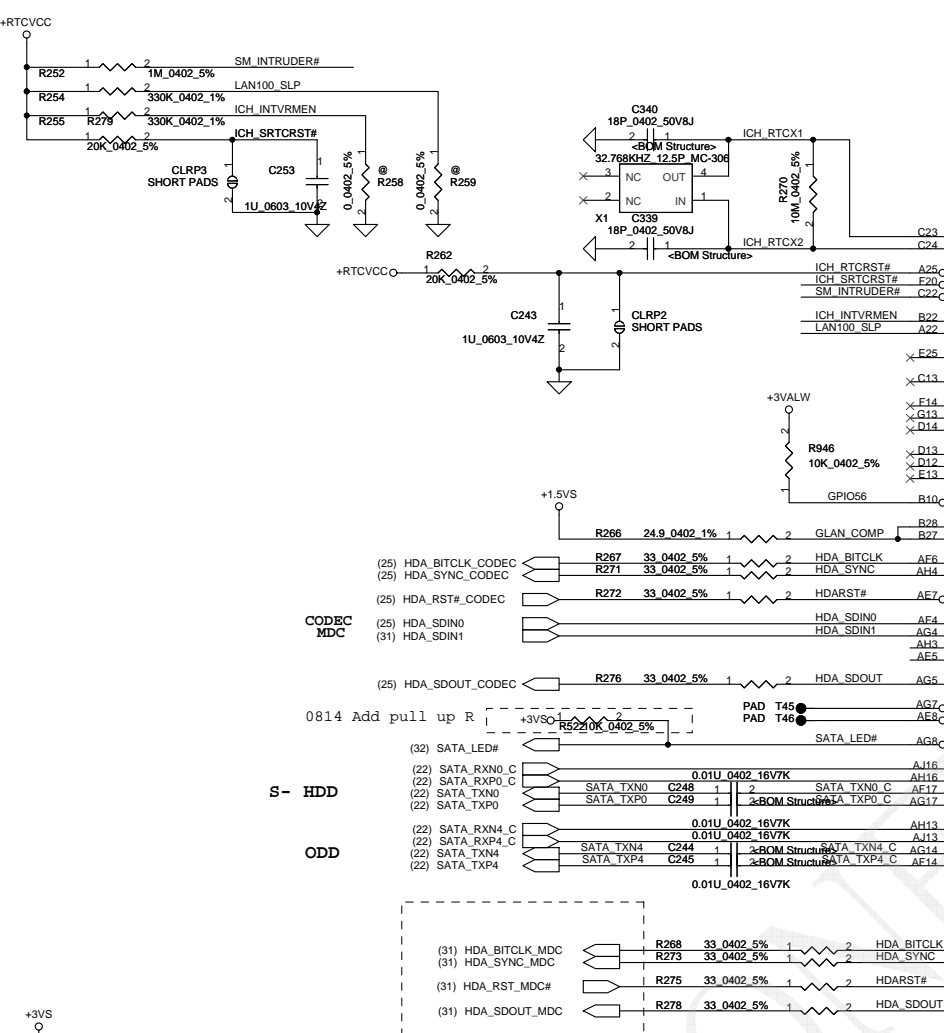


ICH8M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

ICH_INTVRMEN Low = Internal VR Disabled
High = Internal VR Enabled(Default)

ICH8M LAN100 SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)

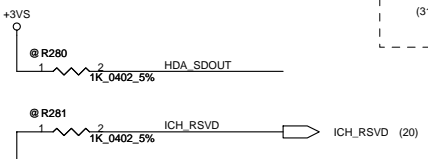
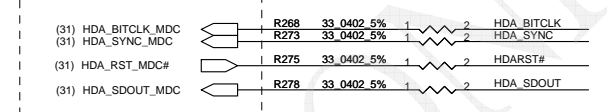
ICH_LAN100_SLP Low = Internal VR Disabled
High = Internal VR Enabled(Default)



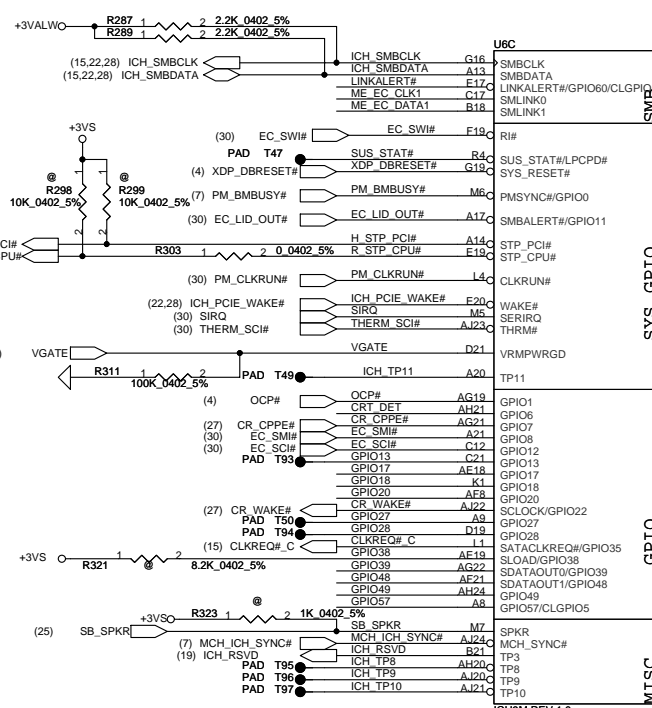
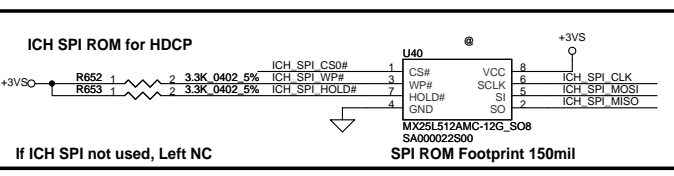
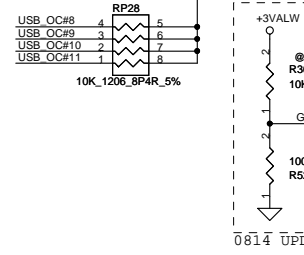
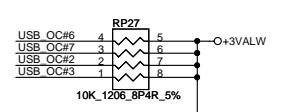
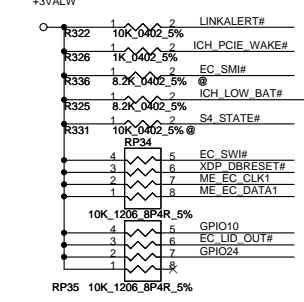
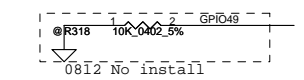
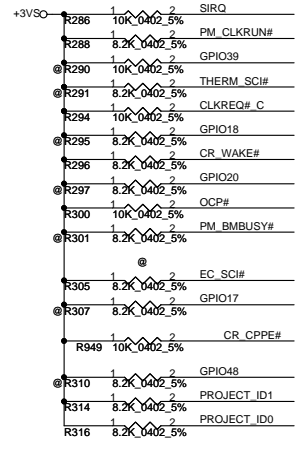
CODEC MDC

S- HDD

ODD



ICH_RSVD	HDA_SDOUT_CODEC	
0	0	
0	1	
1	0	
1	1	



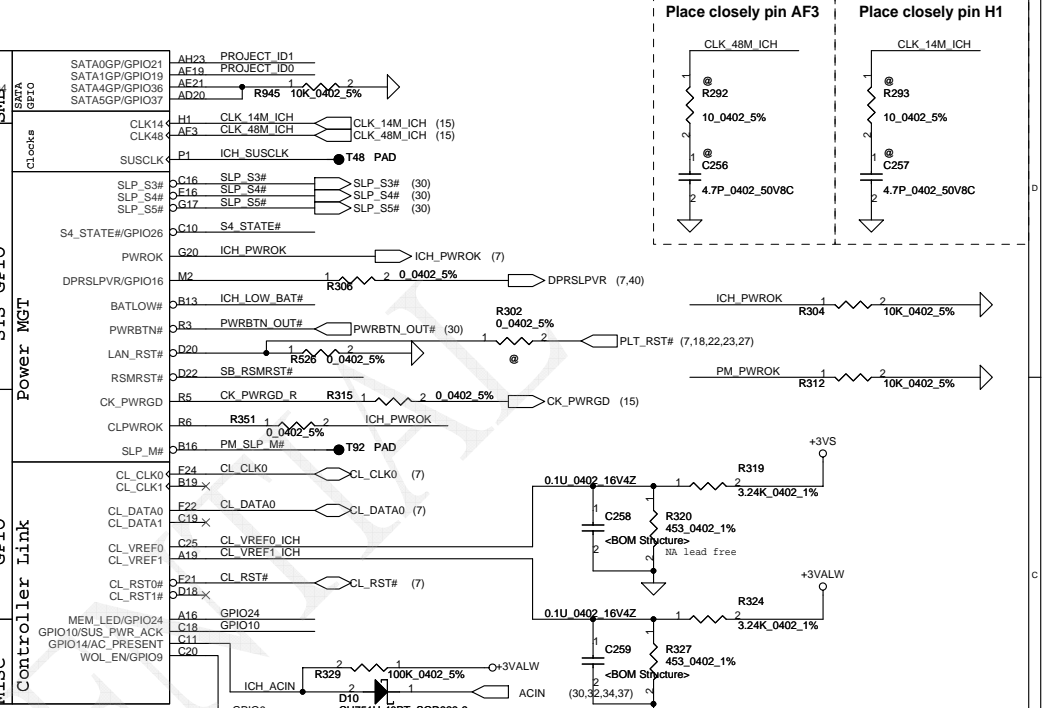
New Card

GIGA LAN

MINI CARD

CARD READER

GLAN

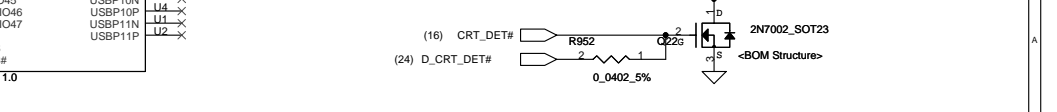
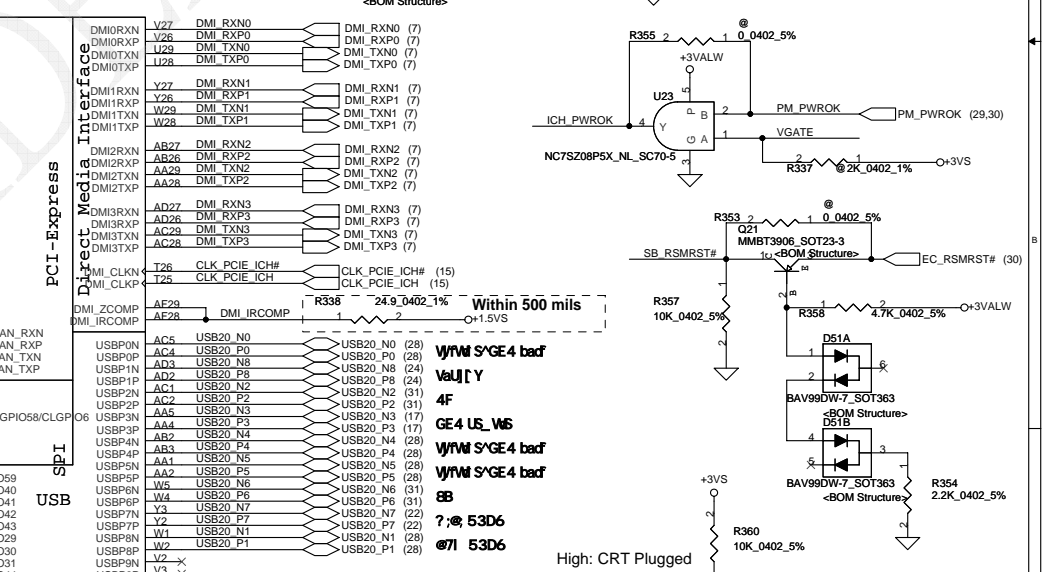
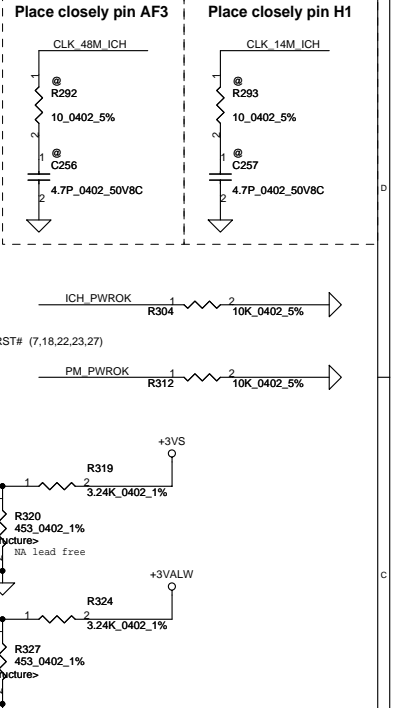


U6D

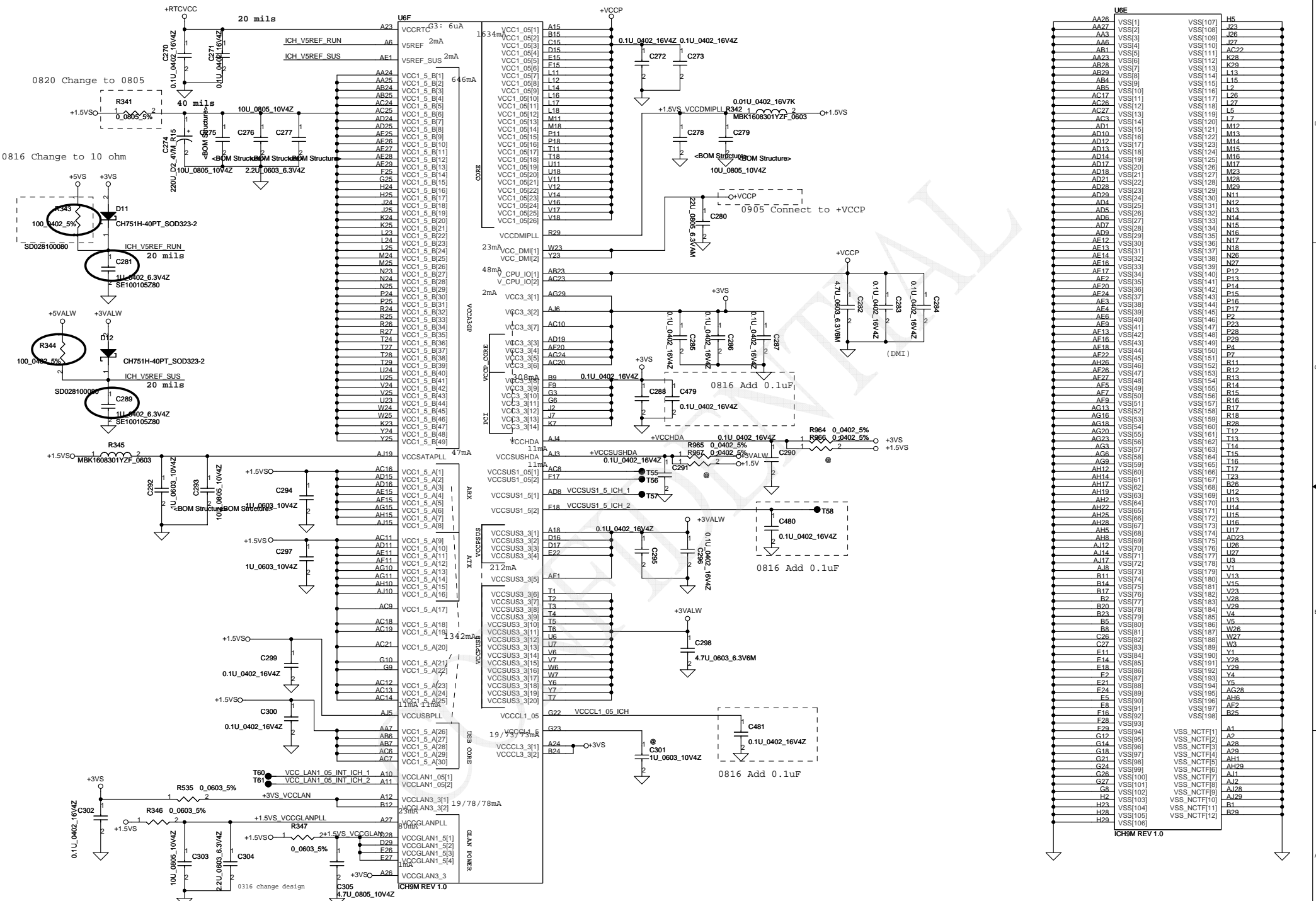
PCI-Express

USB

SPIC



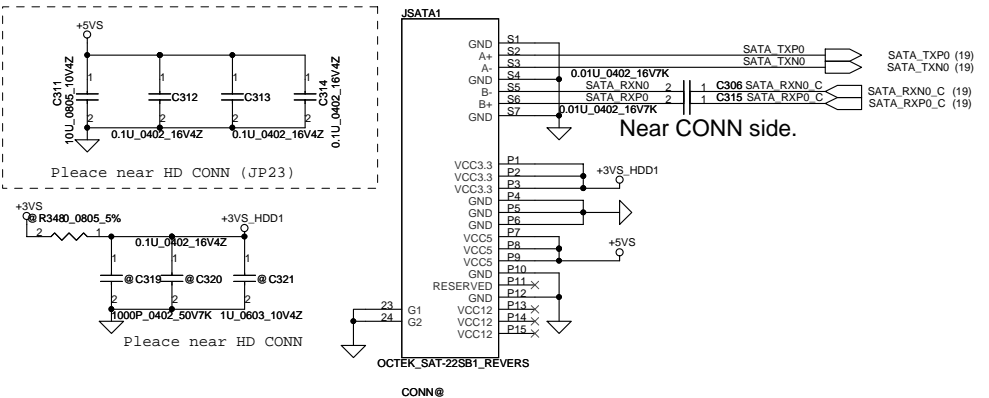
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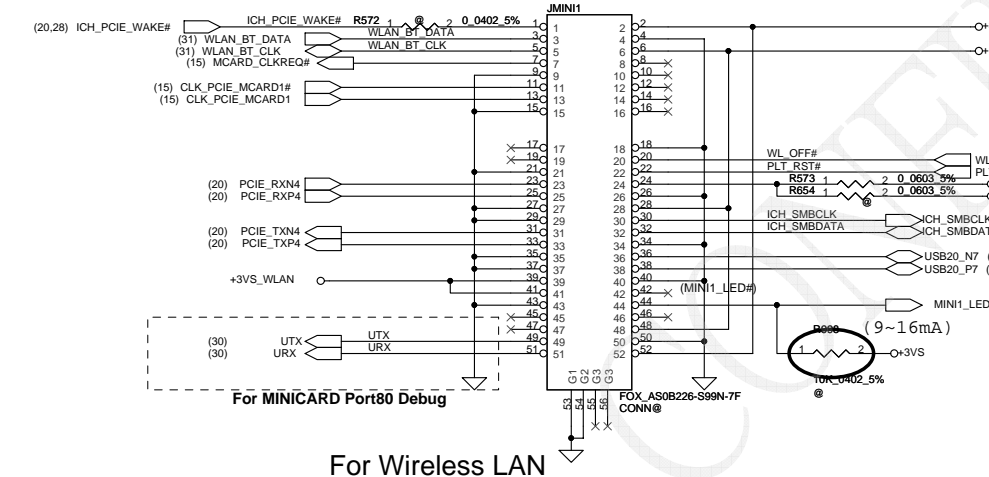
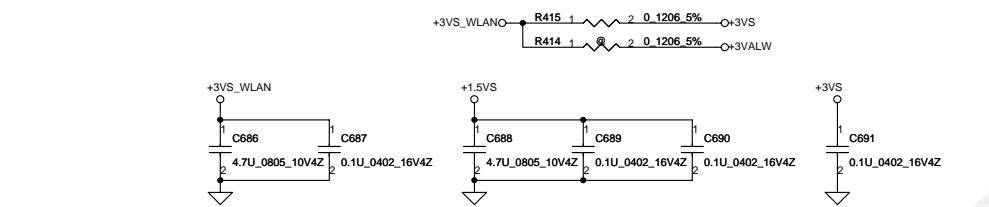
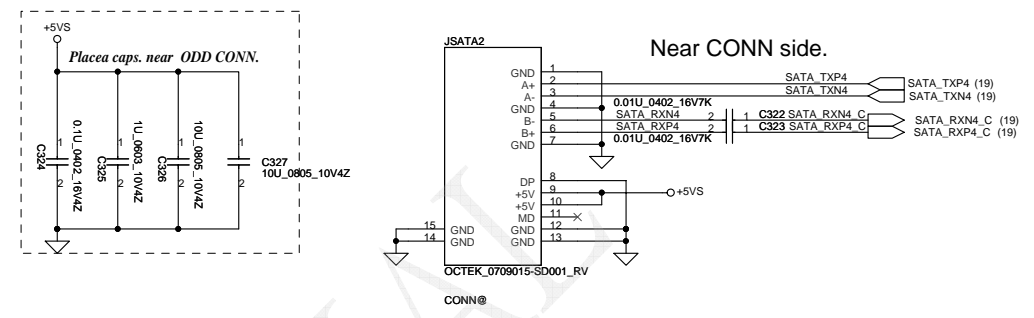
Pin	Internal Connection	Pin	Internal Connection	Pin	Internal Connection
AA26	VSS[1]	VSS[107]	H5		
AA27	VSS[2]	VSS[108]	J23		
AA3	VSS[3]	VSS[109]	J26		
AA4	VSS[4]	VSS[110]	J27		
AA5	VSS[5]	VSS[111]	AC22		
AA6	VSS[6]	VSS[112]	K28		
AA7	VSS[7]	VSS[113]	K29		
AA8	VSS[8]	VSS[114]	L13		
AA9	VSS[9]	VSS[115]	L14		
AA10	VSS[10]	VSS[116]	L15		
AA11	VSS[11]	VSS[117]	L16		
AA12	VSS[12]	VSS[118]	L17		
AA13	VSS[13]	VSS[119]	L18		
AA14	VSS[14]	VSS[120]	M12		
AA15	VSS[15]	VSS[121]	M13		
AA16	VSS[16]	VSS[122]	M14		
AA17	VSS[17]	VSS[123]	M15		
AA18	VSS[18]	VSS[124]	M16		
AA19	VSS[19]	VSS[125]	M17		
AA20	VSS[20]	VSS[126]	M18		
AA21	VSS[21]	VSS[127]	M19		
AA22	VSS[22]	VSS[128]	M20		
AA23	VSS[23]	VSS[129]	M21		
AA24	VSS[24]	VSS[130]	M22		
AA25	VSS[25]	VSS[131]	M23		
AA26	VSS[26]	VSS[132]	M24		
AA27	VSS[27]	VSS[133]	M25		
AA28	VSS[28]	VSS[134]	N15		
AA29	VSS[29]	VSS[135]	N16		
AA30	VSS[30]	VSS[136]	N17		
AA31	VSS[31]	VSS[137]	N18		
AA32	VSS[32]	VSS[138]	N19		
AA33	VSS[33]	VSS[139]	N20		
AA34	VSS[34]	VSS[140]	N21		
AA35	VSS[35]	VSS[141]	N22		
AA36	VSS[36]	VSS[142]	N23		
AA37	VSS[37]	VSS[143]	N24		
AA38	VSS[38]	VSS[144]	N25		
AA39	VSS[39]	VSS[145]	P2		
AA40	VSS[40]	VSS[146]	P3		
AA41	VSS[41]	VSS[147]	P4		
AA42	VSS[42]	VSS[148]	P5		
AA43	VSS[43]	VSS[149]	P6		
AA44	VSS[44]	VSS[150]	P7		
AA45	VSS[45]	VSS[151]	P8		
AA46	VSS[46]	VSS[152]	P9		
AA47	VSS[47]	VSS[153]	P10		
AA48	VSS[48]	VSS[154]	P11		
AA49	VSS[49]	VSS[155]	P12		
AA50	VSS[50]	VSS[156]	P13		
AA51	VSS[51]	VSS[157]	P14		
AA52	VSS[52]	VSS[158]	P15		
AA53	VSS[53]	VSS[159]	P16		
AA54	VSS[54]	VSS[160]	P17		
AA55	VSS[55]	VSS[161]	P18		
AA56	VSS[56]	VSS[162]	P19		
AA57	VSS[57]	VSS[163]	P20		
AA58	VSS[58]	VSS[164]	P21		
AA59	VSS[59]	VSS[165]	P22		
AA60	VSS[60]	VSS[166]	P23		
AA61	VSS[61]	VSS[167]	P24		
AA62	VSS[62]	VSS[168]	P25		
AA63	VSS[63]	VSS[169]	R11		
AA64	VSS[64]	VSS[170]	R12		
AA65	VSS[65]	VSS[171]	R13		
AA66	VSS[66]	VSS[172]	R14		
AA67	VSS[67]	VSS[173]	R15		
AA68	VSS[68]	VSS[174]	R16		
AA69	VSS[69]	VSS[175]	R17		
AA70	VSS[70]	VSS[176]	R18		
AA71	VSS[71]	VSS[177]	R19		
AA72	VSS[72]	VSS[178]	R20		
AA73	VSS[73]	VSS[179]	R21		
AA74	VSS[74]	VSS[180]	R22		
AA75	VSS[75]	VSS[181]	R23		
AA76	VSS[76]	VSS[182]	R24		
AA77	VSS[77]	VSS[183]	R25		
AA78	VSS[78]	VSS[184]	R26		
AA79	VSS[79]	VSS[185]	R27		
AA80	VSS[80]	VSS[186]	R28		
AA81	VSS[81]	VSS[187]	R29		
AA82	VSS[82]	VSS[188]	R30		
AA83	VSS[83]	VSS[189]	R31		
AA84	VSS[84]	VSS[190]	R32		
AA85	VSS[85]	VSS[191]	R33		
AA86	VSS[86]	VSS[192]	R34		
AA87	VSS[87]	VSS[193]	R35		
AA88	VSS[88]	VSS[194]	R36		
AA89	VSS[89]	VSS[195]	R37		
AA90	VSS[90]	VSS[196]	R38		
AA91	VSS[91]	VSS[197]	R39		
AA92	VSS[92]	VSS[198]	R40		
AA93	VSS[93]	VSS[199]	R41		
AA94	VSS[94]	VSS[200]	R42		
AA95	VSS[95]	VSS[201]	R43		
AA96	VSS[96]	VSS[202]	R44		
AA97	VSS[97]	VSS[203]	R45		
AA98	VSS[98]	VSS[204]	R46		
AA99	VSS[99]	VSS[205]	R47		
AA100	VSS[100]	VSS[206]	R48		
AA101	VSS[101]	VSS[207]	R49		
AA102	VSS[102]	VSS[208]	R50		
AA103	VSS[103]	VSS[209]	R51		
AA104	VSS[104]	VSS[210]	R52		
AA105	VSS[105]	VSS[211]	R53		
AA106	VSS[106]	VSS[212]	R54		

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Date:	Tuesday, April 29, 2008	Sheet	21 of 42

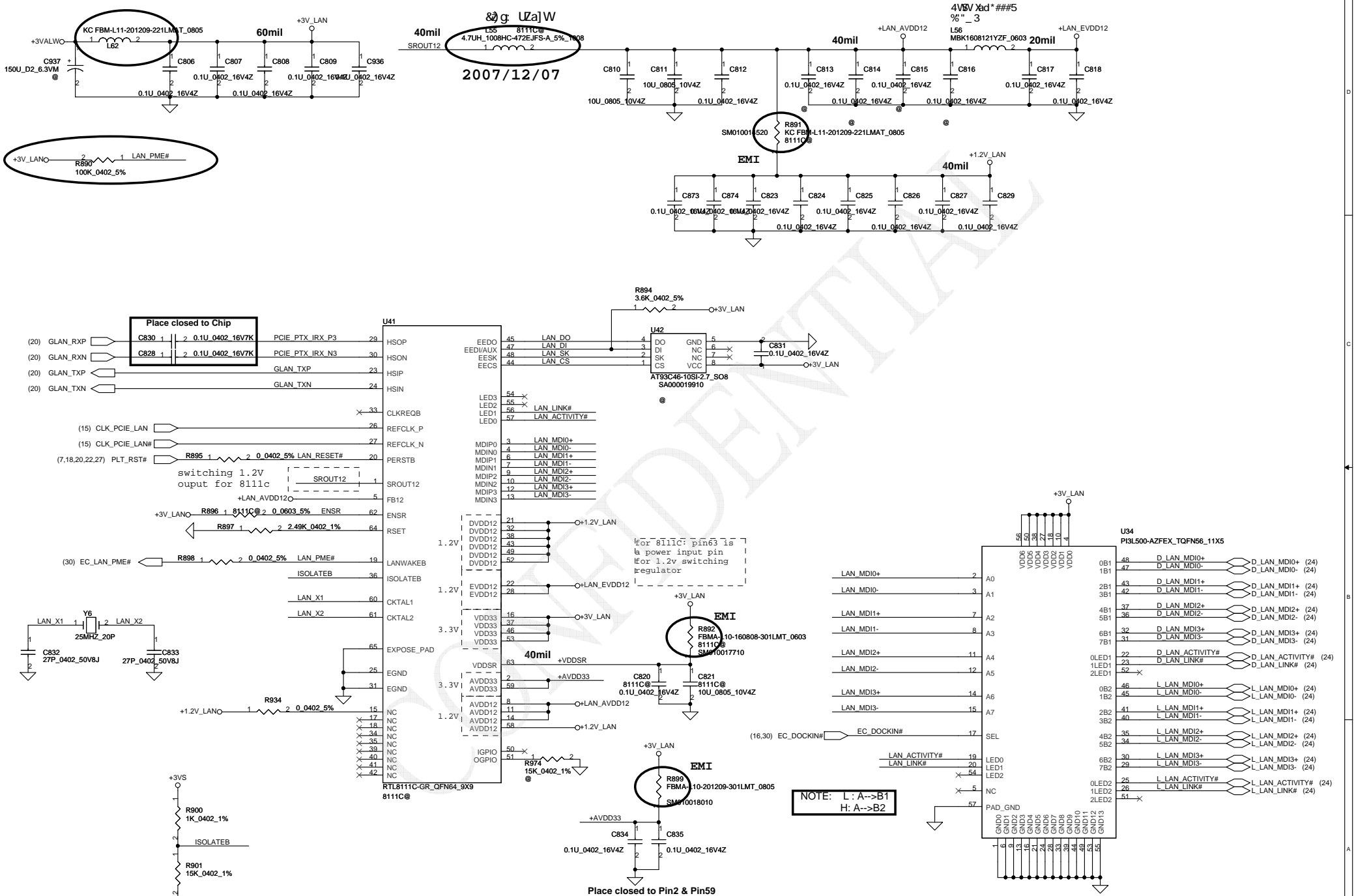
HDD Connector



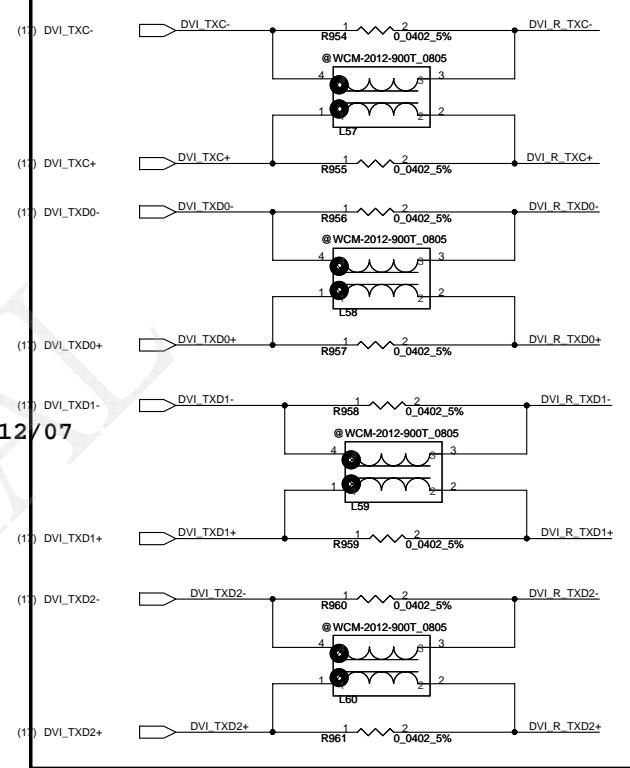
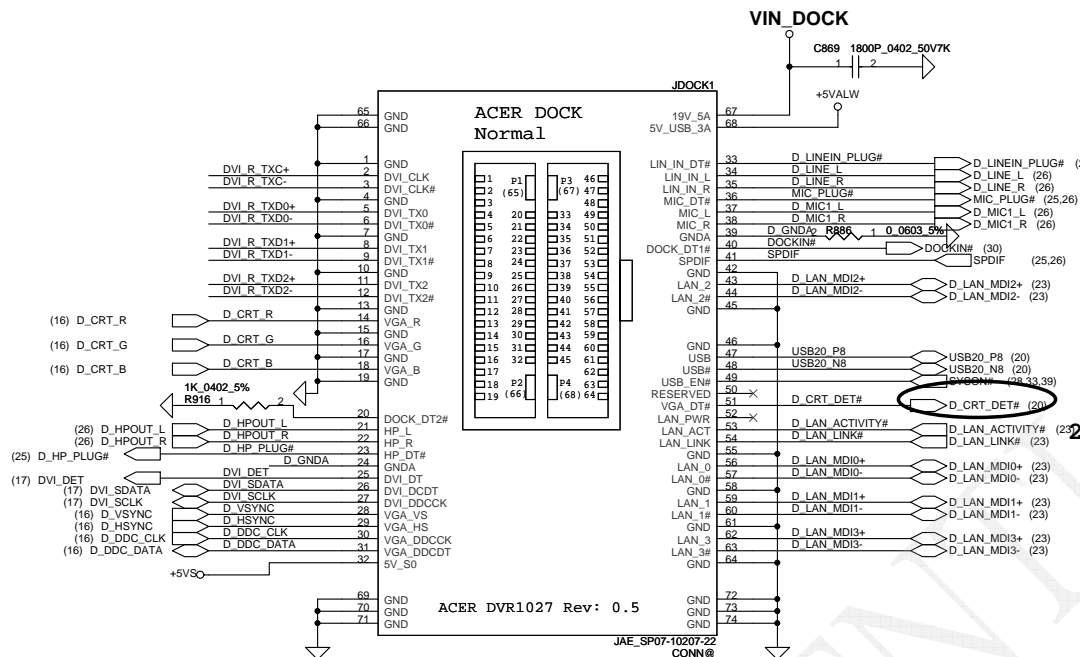
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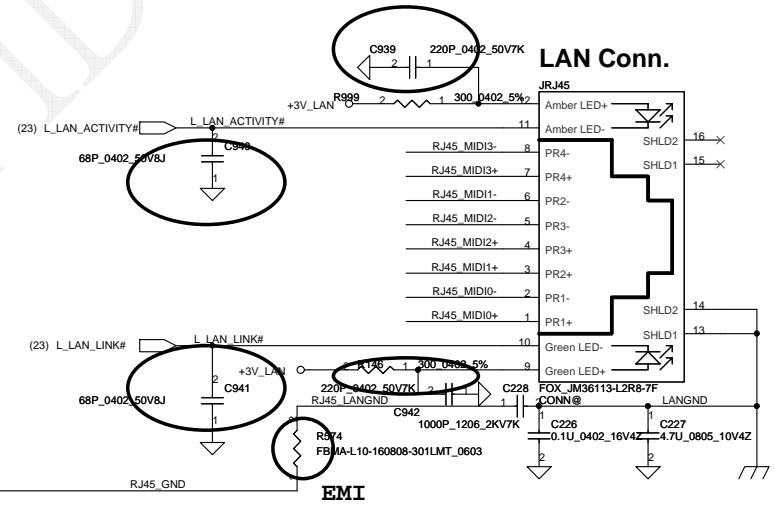
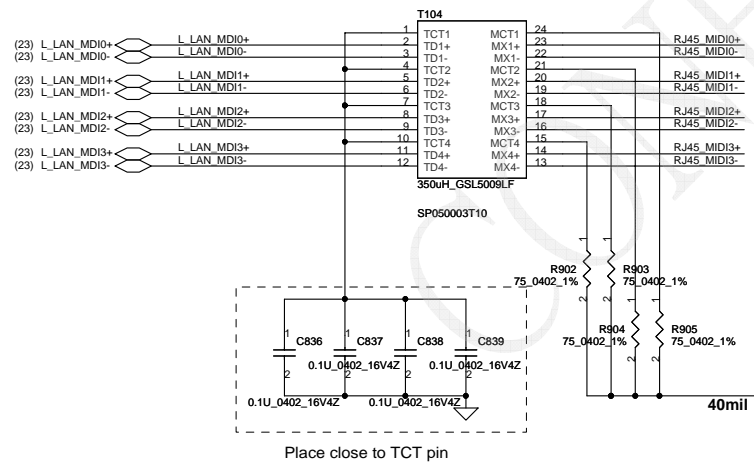
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EMI

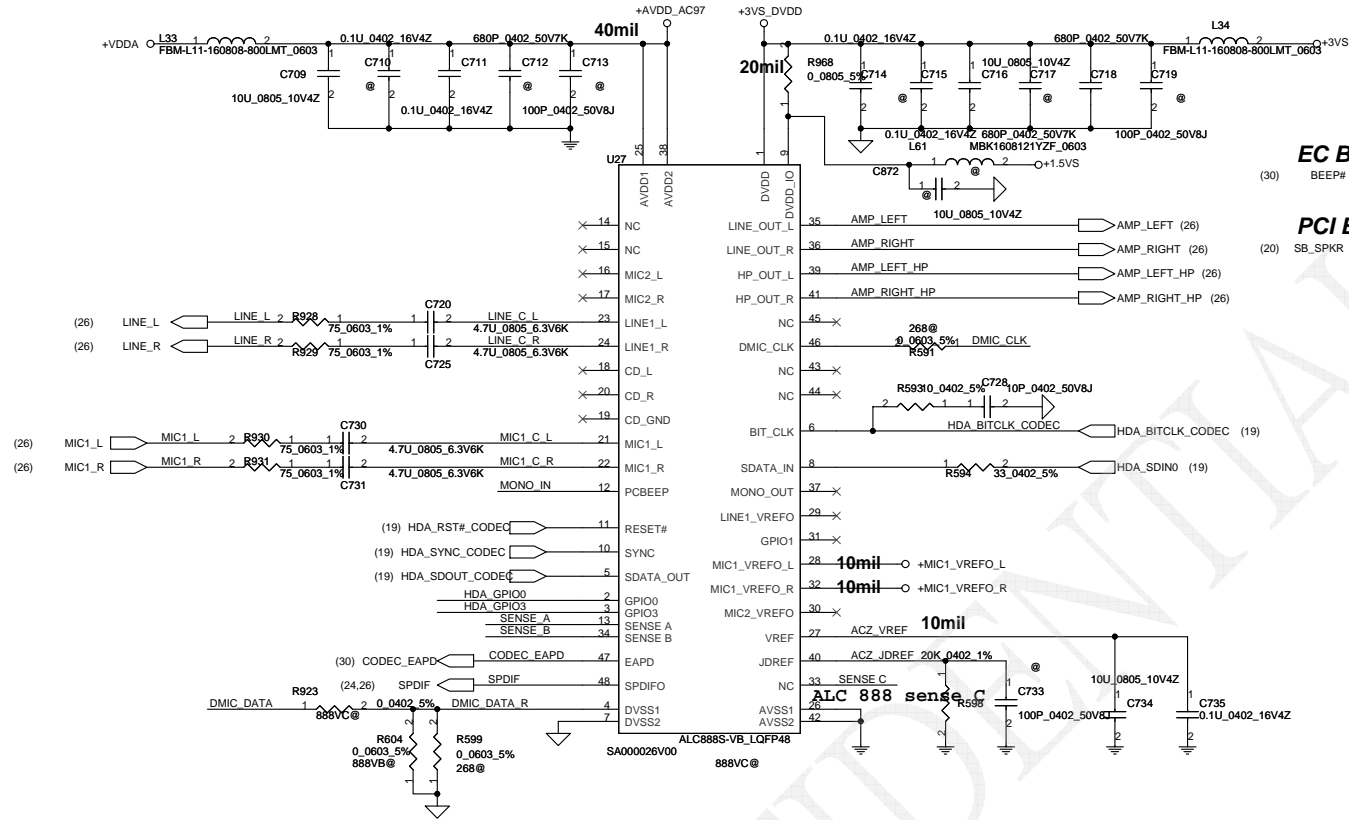


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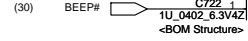
Place close to TCT pin

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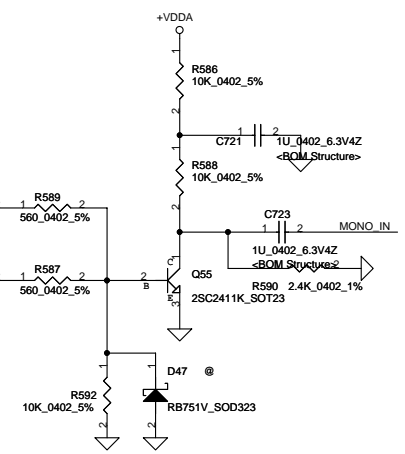
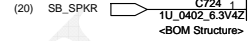
HD Audio Codec



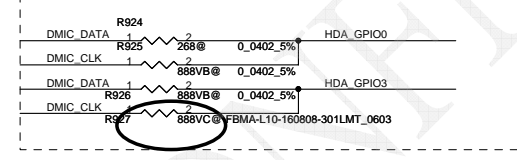
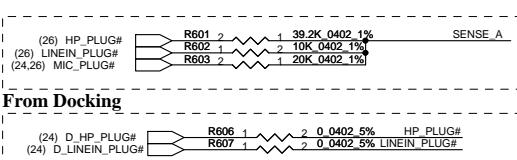
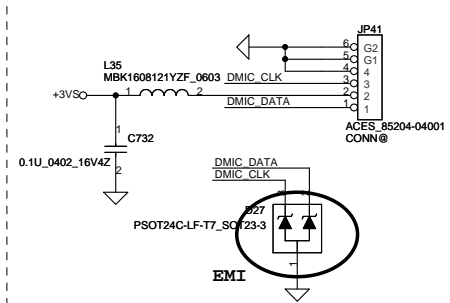
EC BEEP



PCI BEEP

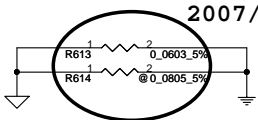
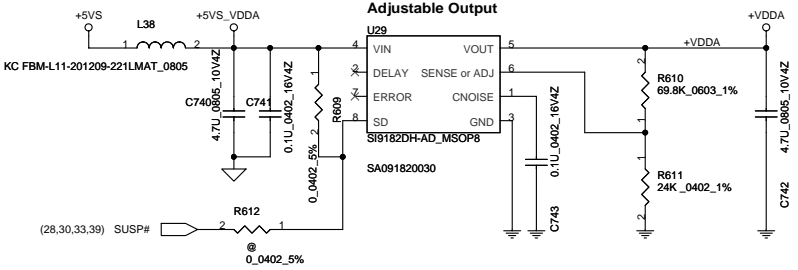


DMIC Conn.



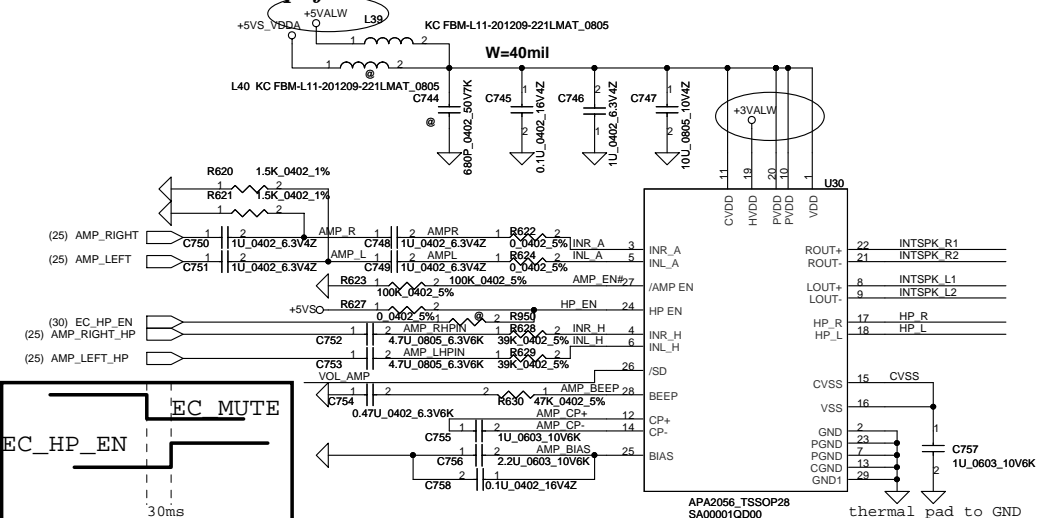
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
SENSE B	5.1K	PORT-D (PIN 35, 36)
	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
SENSE C	5.1K	PORT-H (PIN 45, 46)
	39.2K	CD
	20K	1st S/PDIF Out
	10K	2nd S/PDIF Out
	5.1K	S/PDIF-IN

Regulator for CODEC

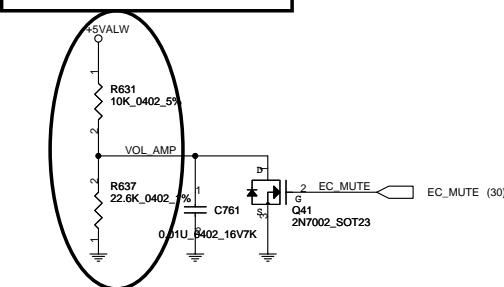


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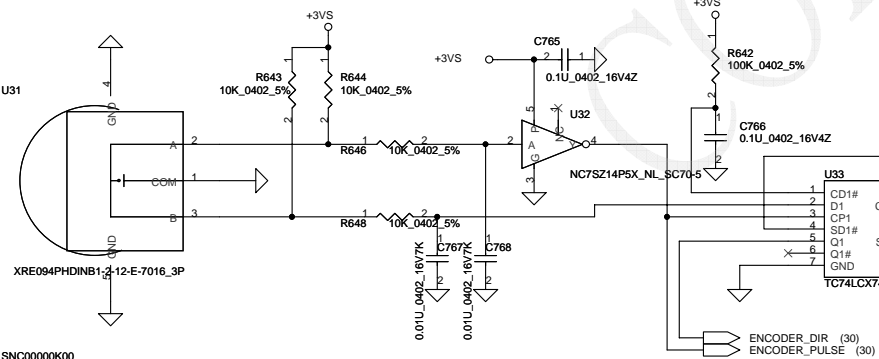
APA2057 SPK/HP Amplifier



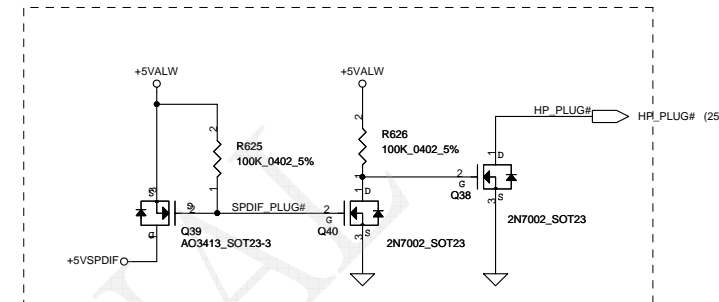
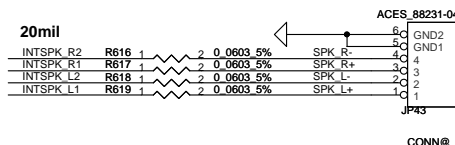
IN_A Gain = 10dB (Internal Speaker)
IN_H Gain = 0dB (Headphone)



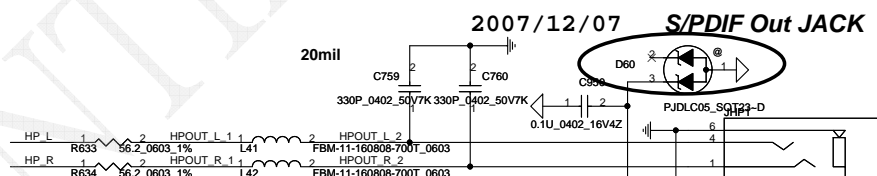
Volume Control Circuit



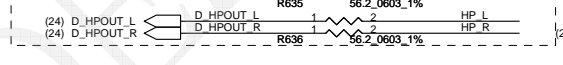
Int. Speaker Conn.



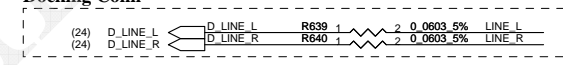
LINE Out/Headphone Out



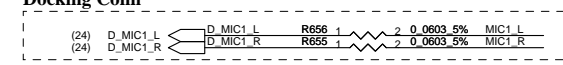
Docking Conn



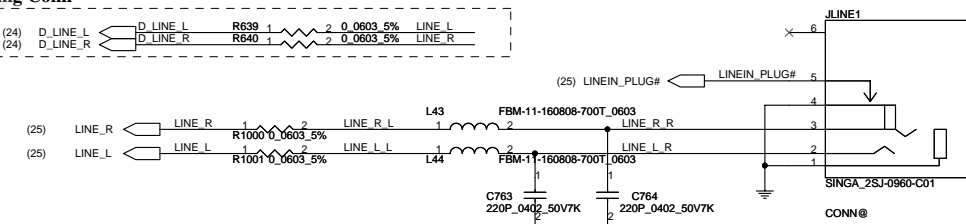
Docking Conn



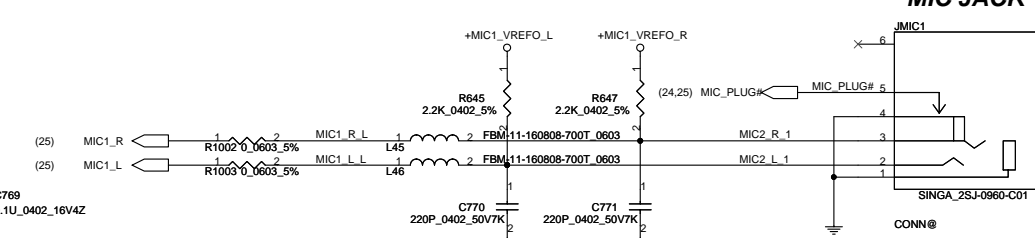
Docking Conn



LINE-IN JACK

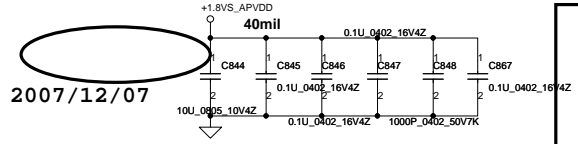
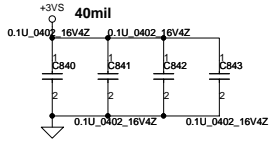


MIC JACK



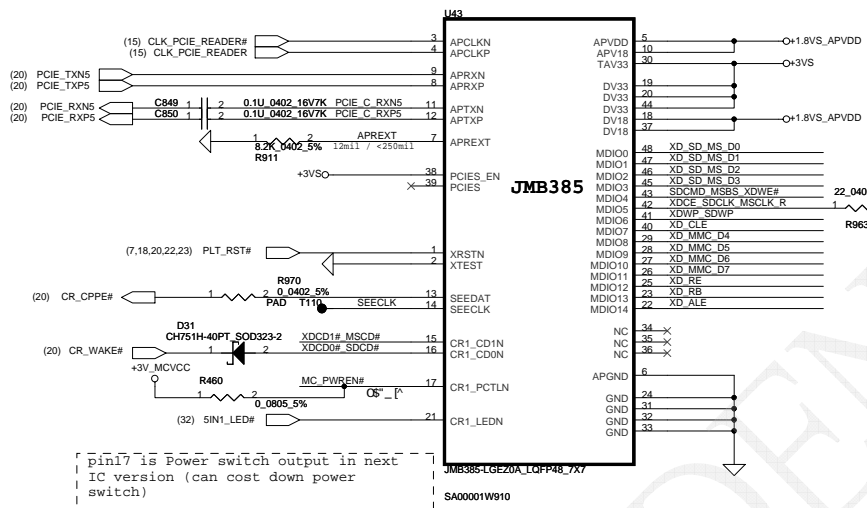
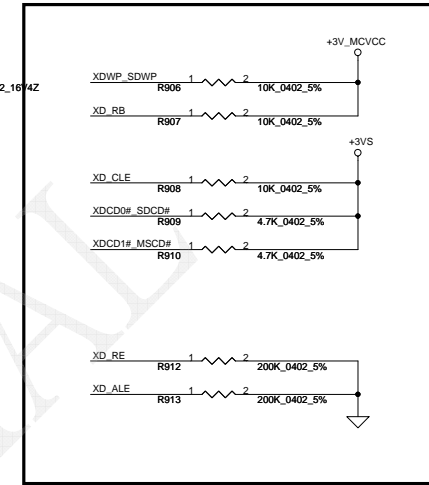
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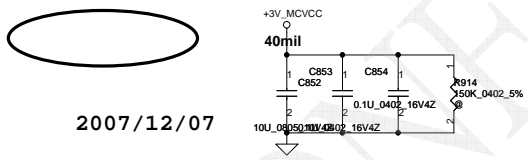
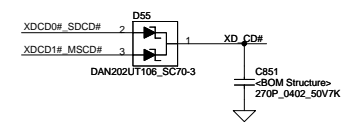


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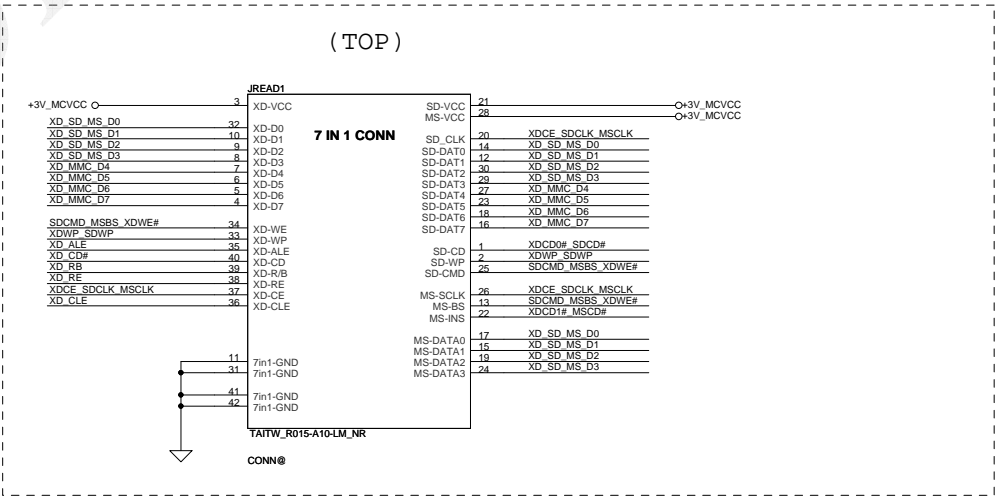
MDIO PULL HIGH/LOW ?



pin17 is Power switch output in next IC version (can cost down power switch)

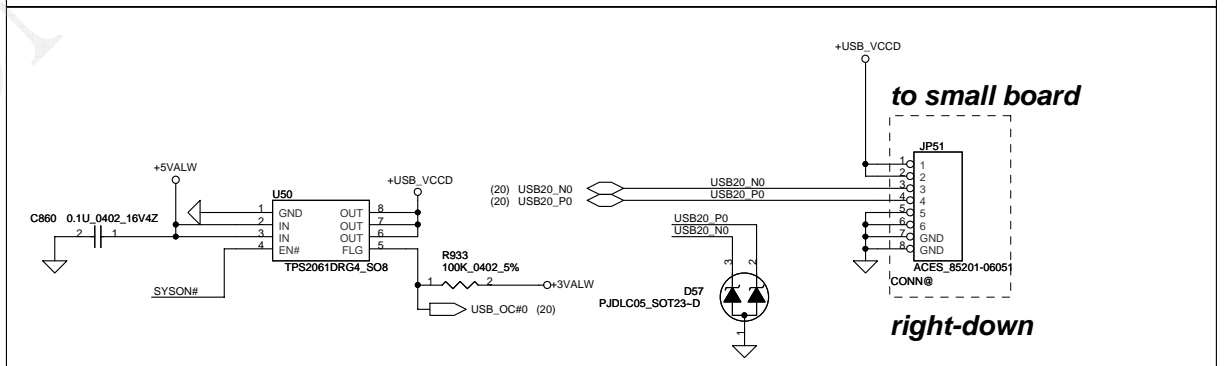
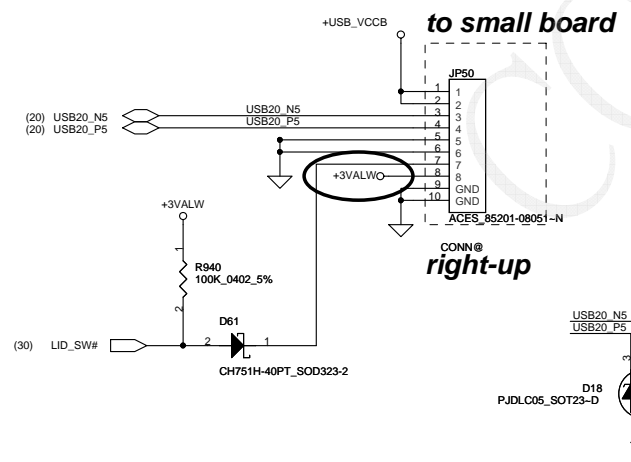
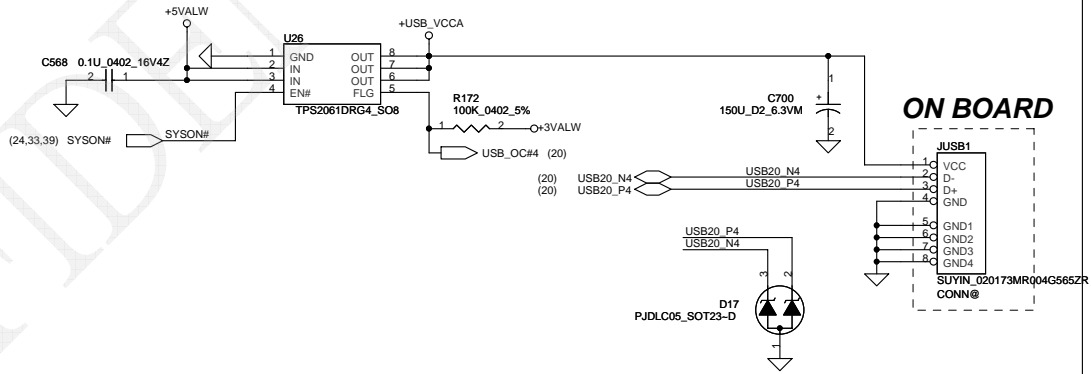
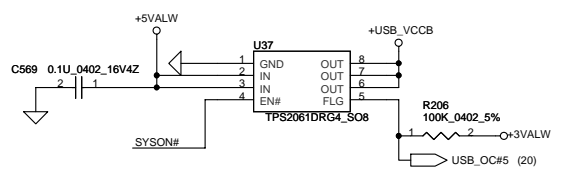
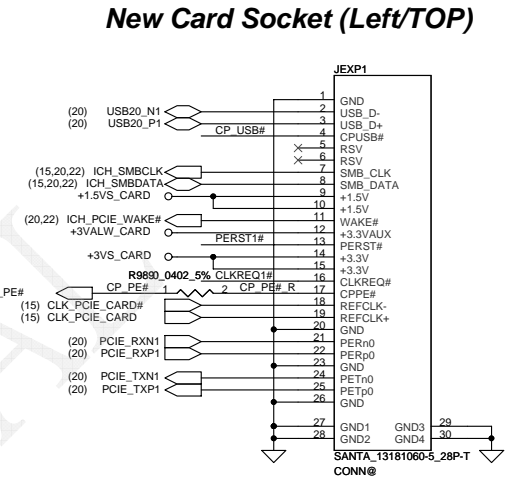
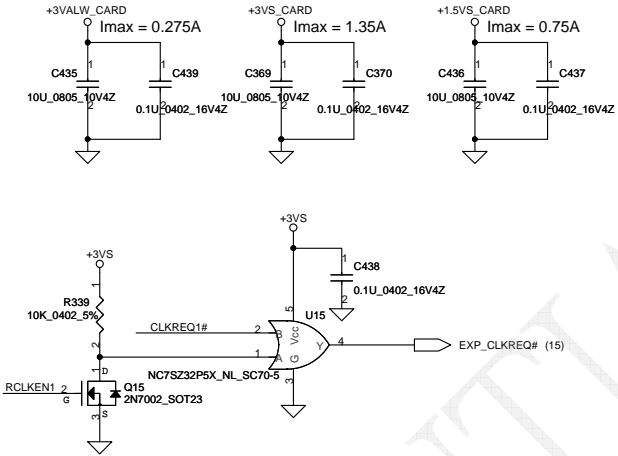
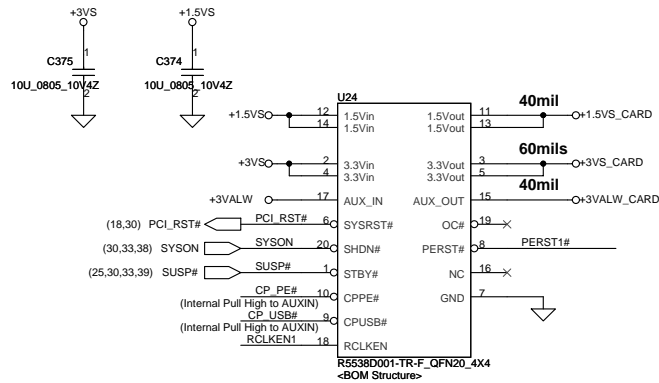


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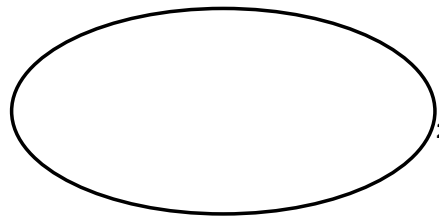
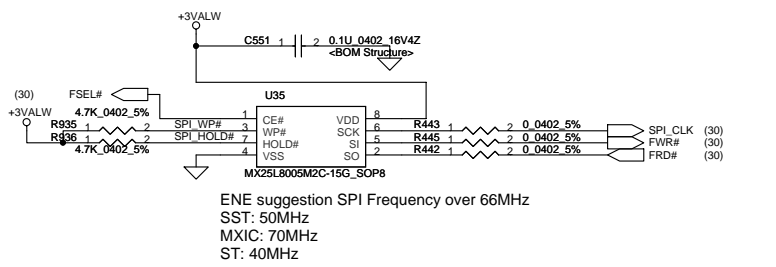
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New Card Power Switch



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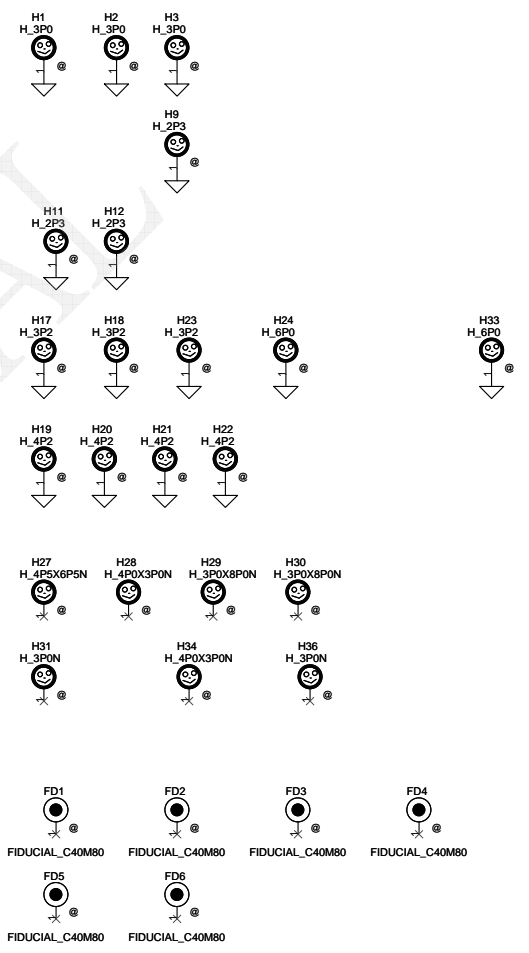
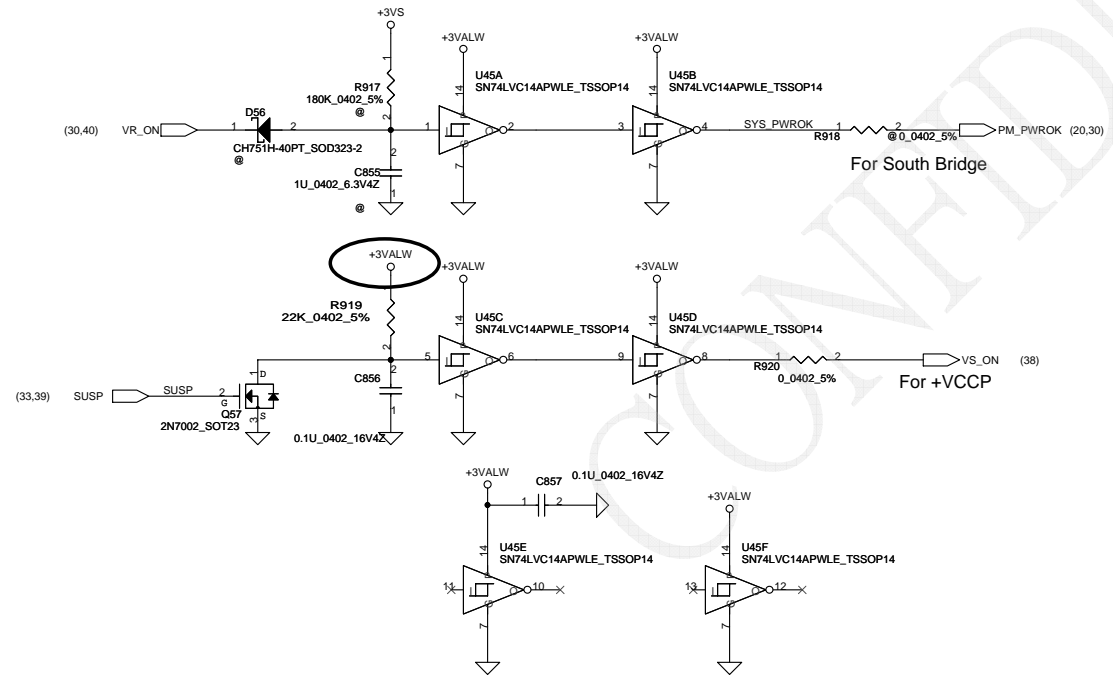
BIOS



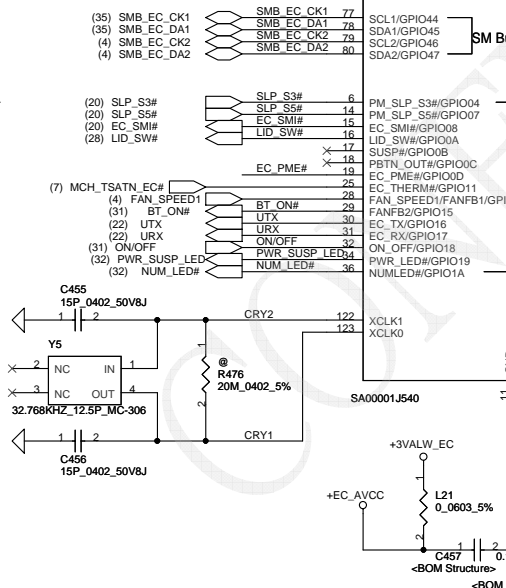
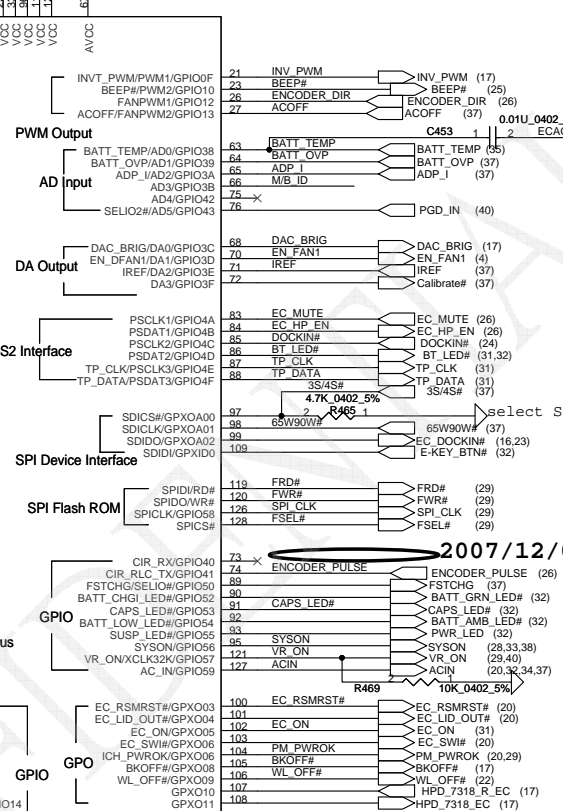
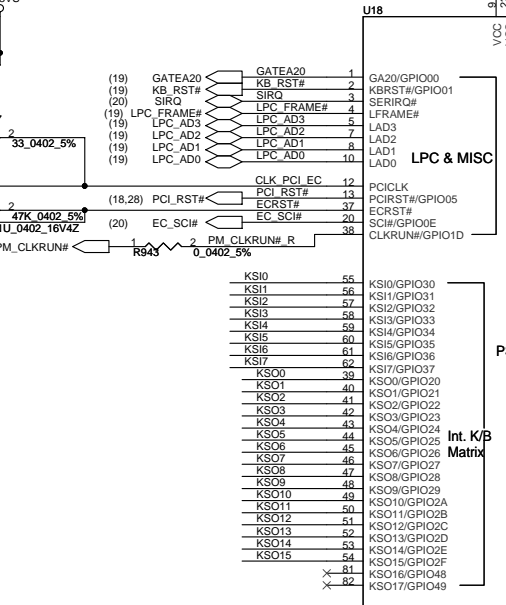
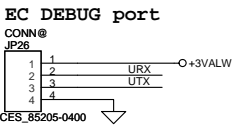
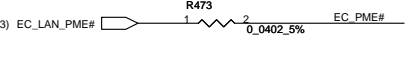
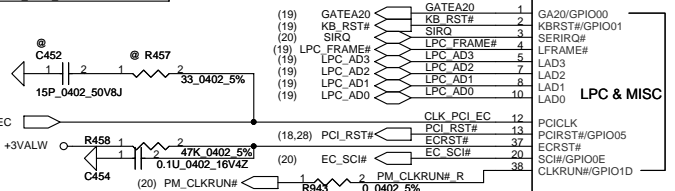
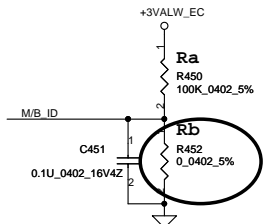
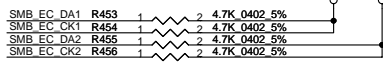
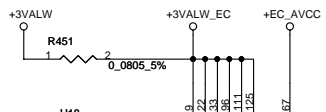
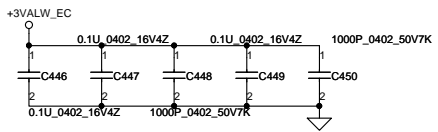
2007/12/07

reserve VS_ON will be driven by EC

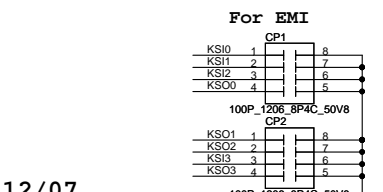
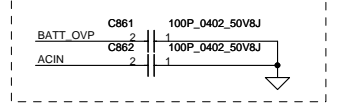
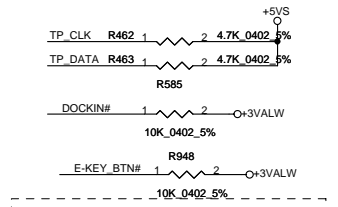
Power ON Circuit



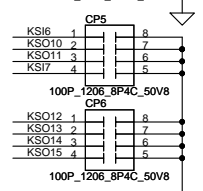
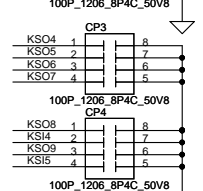
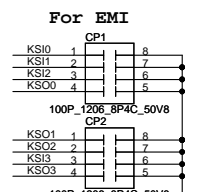
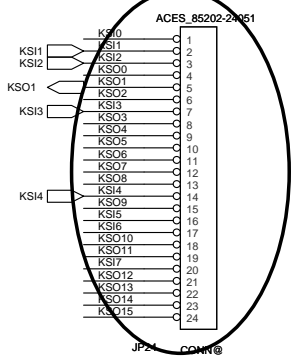
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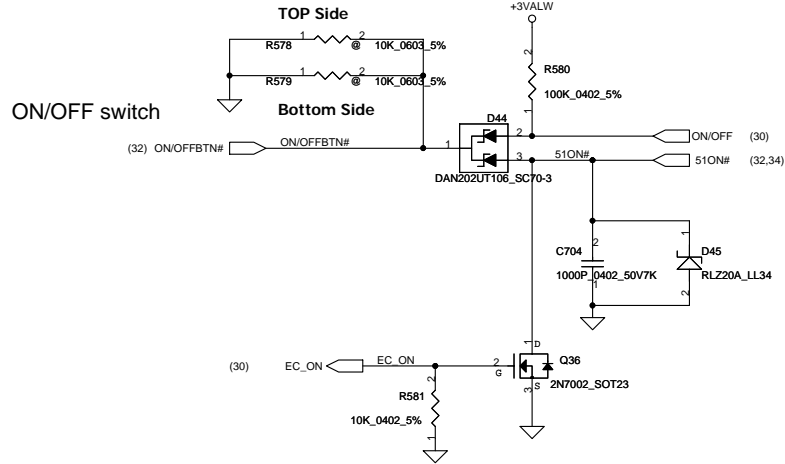
VCC	3.3V+/-5%			
Ra	100K+/-5%			
Board ID	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0V	0V	0V
1	8.2K+/-5%	0.216V	0.250V	0.289V
2	18K+/-5%	0.436V	0.503V	0.538V
3	33K+/-5%	0.712V	0.819V	0.875V
4	56K+/-5%	1.036V	1.185V	1.264V
5	100K+/-5%	1.453V	1.650V	1.759V
6	200K+/-5%	1.935V	2.200V	2.341V
7	NC	2.500V	3.300V	3.300V



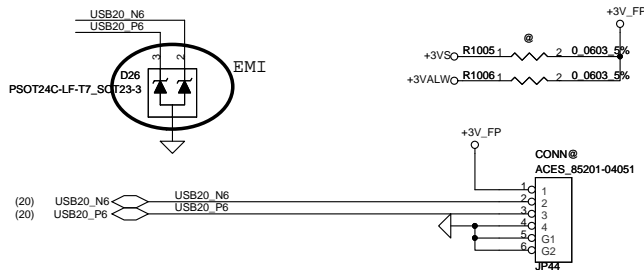
2007/12/07



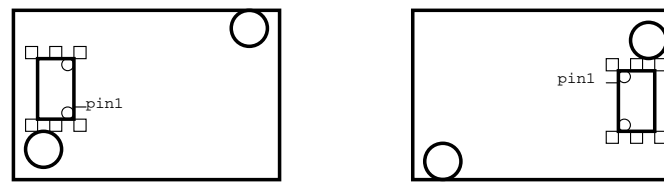
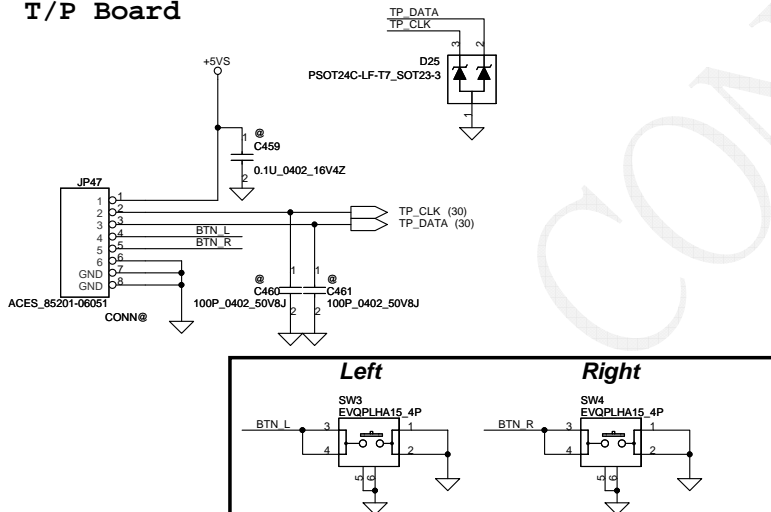
Power Button



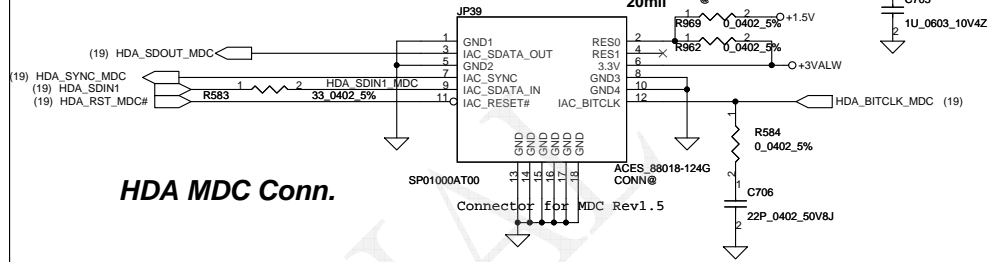
Finger Print Conn



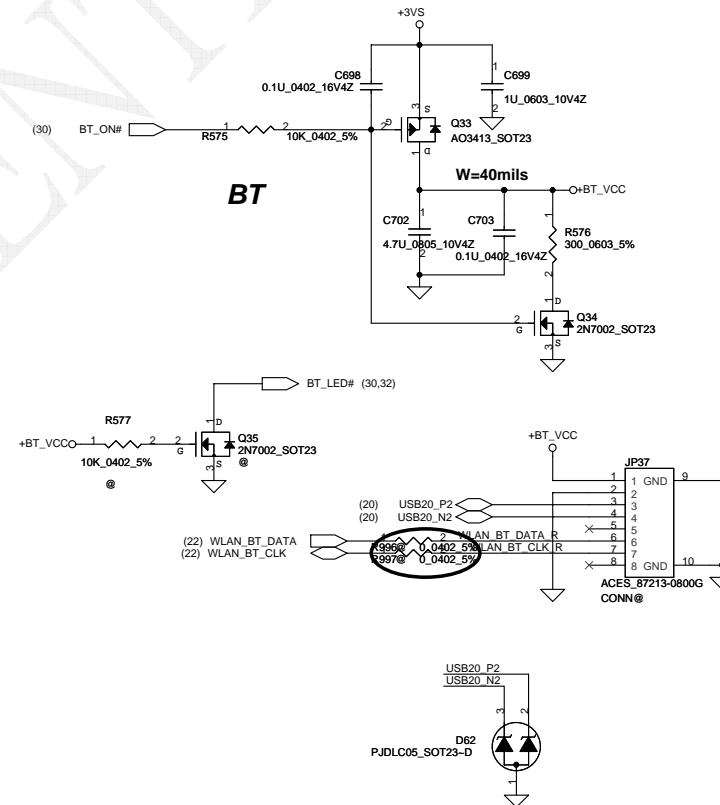
T/P Board



HDA MDC Conn.

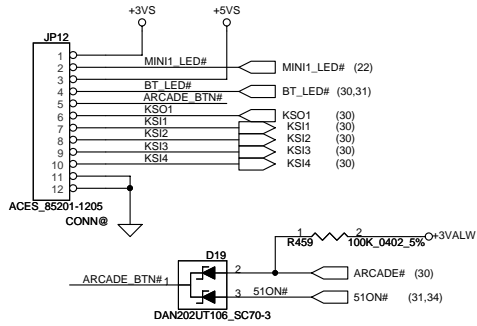


BT



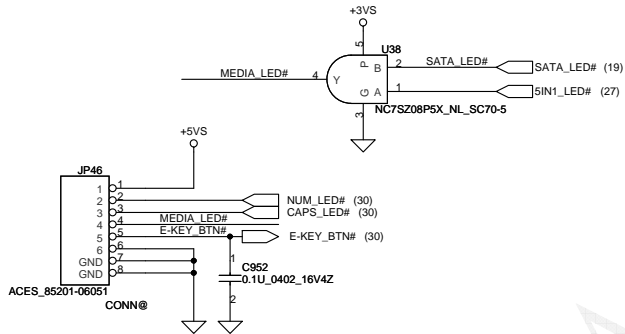
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TO S/W B

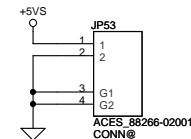
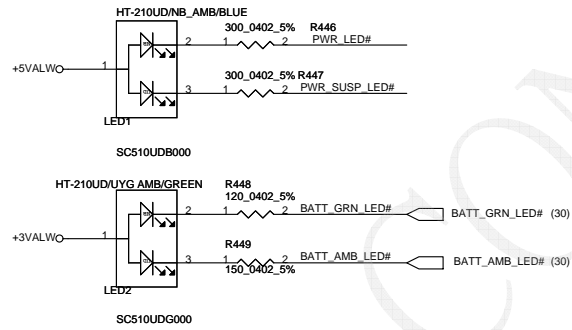
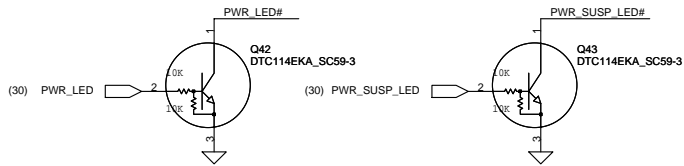
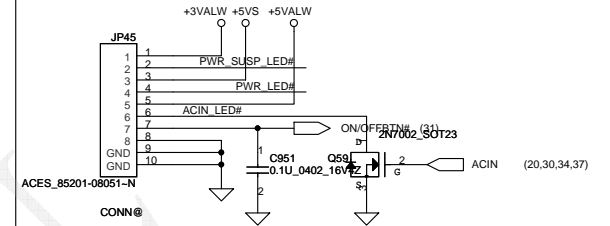


KSO1	
KSI1	WL_BTN#
KSI2	BT_BTN#
KSI3	EMAIL_BTN#
KSI4	IE_BTN#

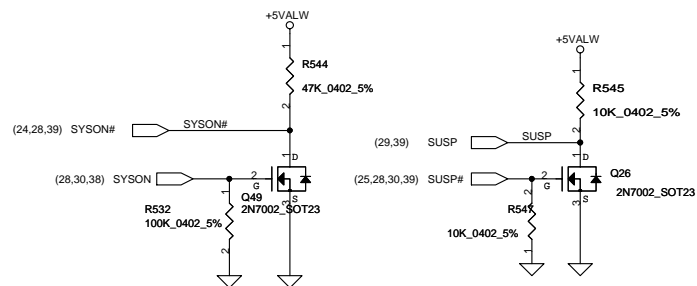
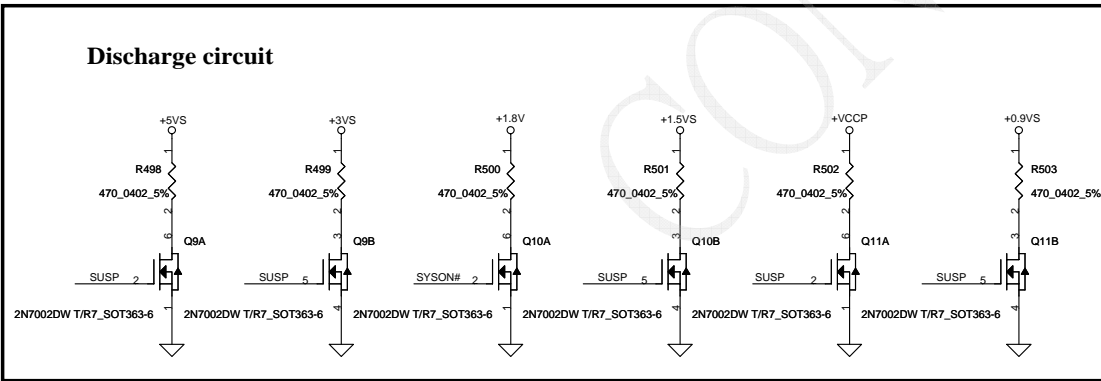
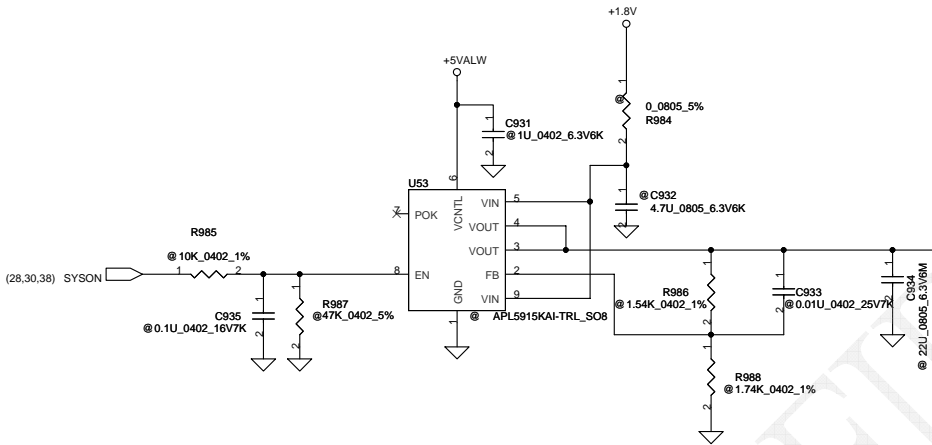
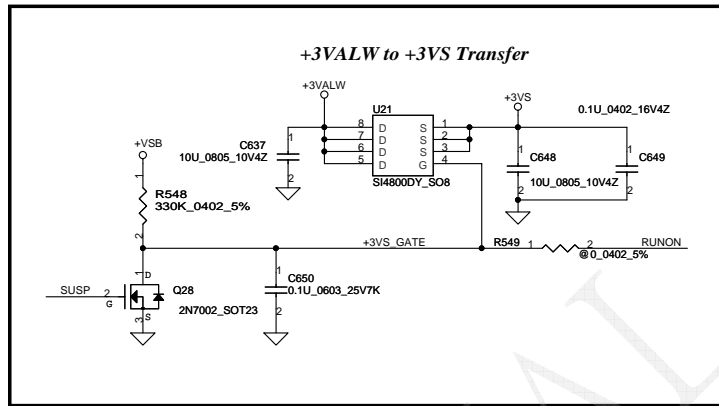
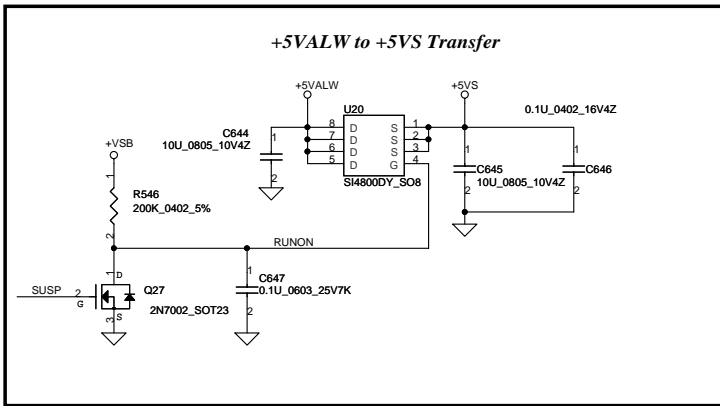
LED & E-BTN/B



TO POWER BTN/B

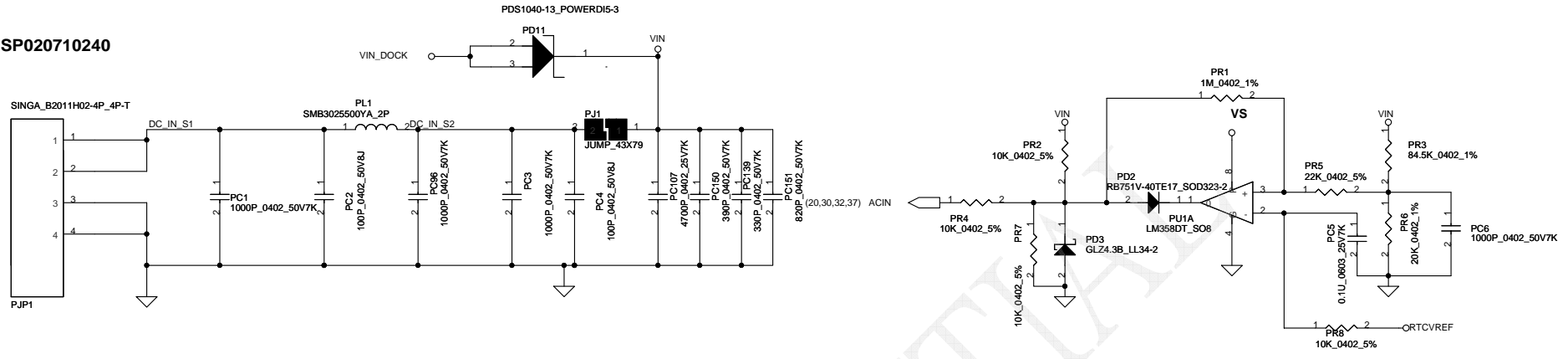


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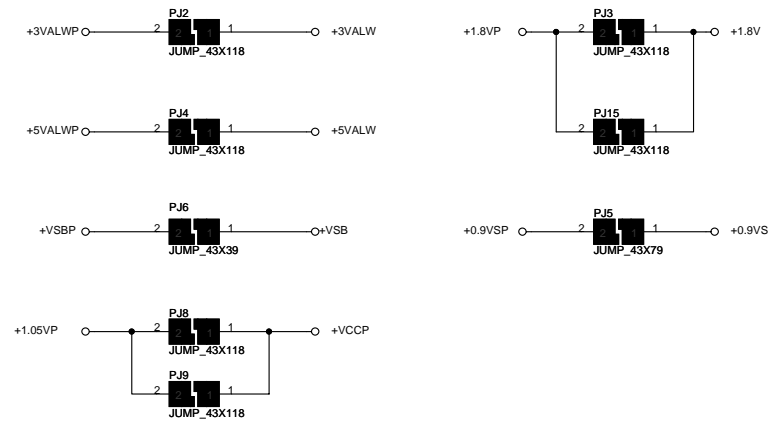
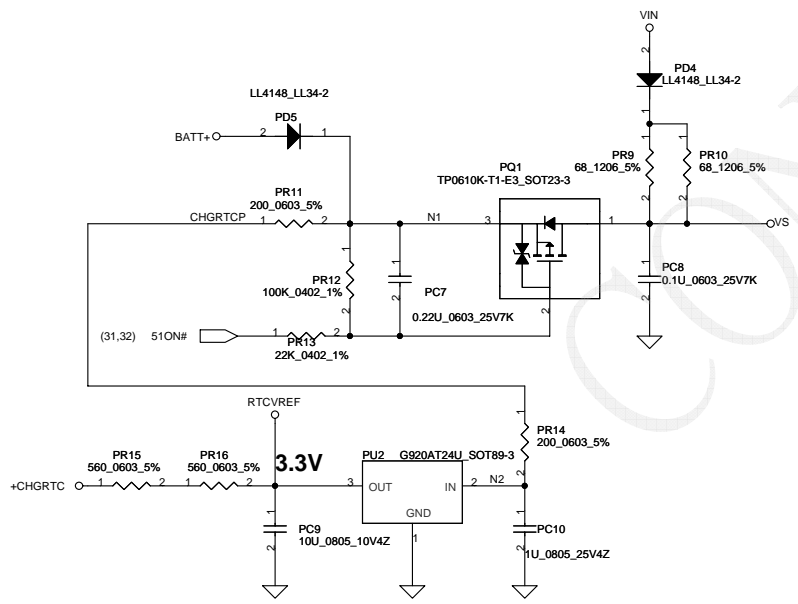


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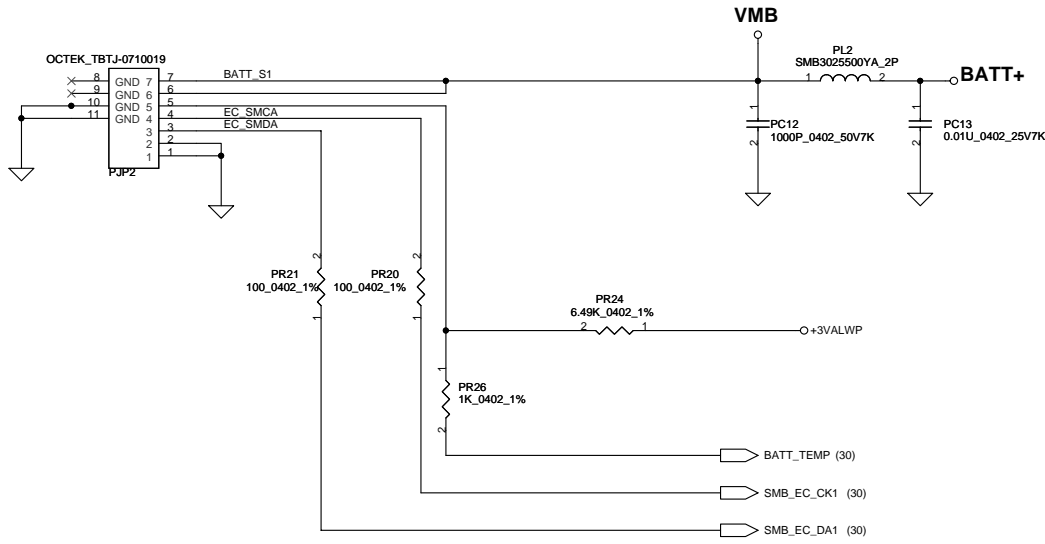
SP020710240



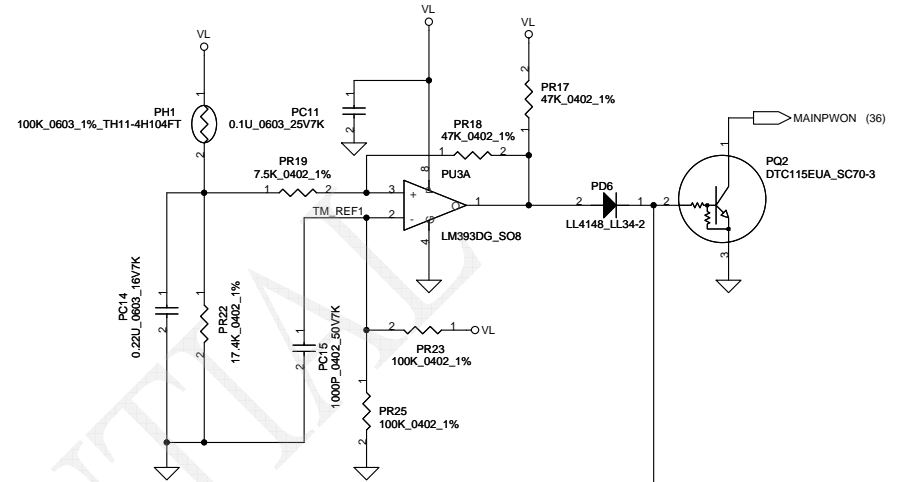
Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



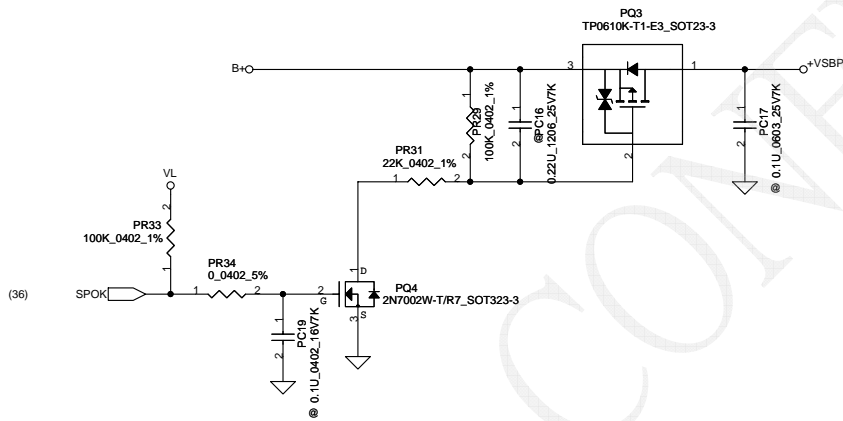
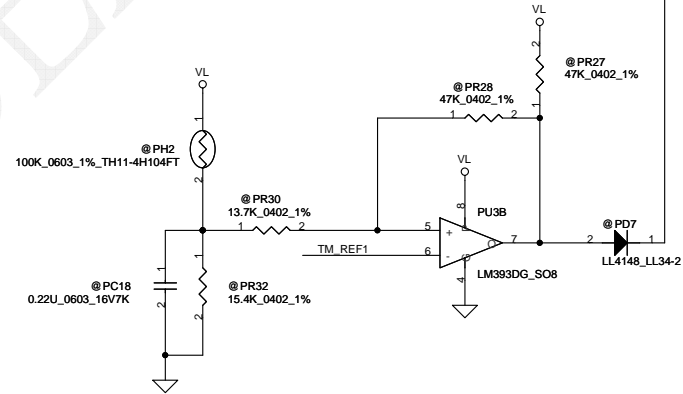
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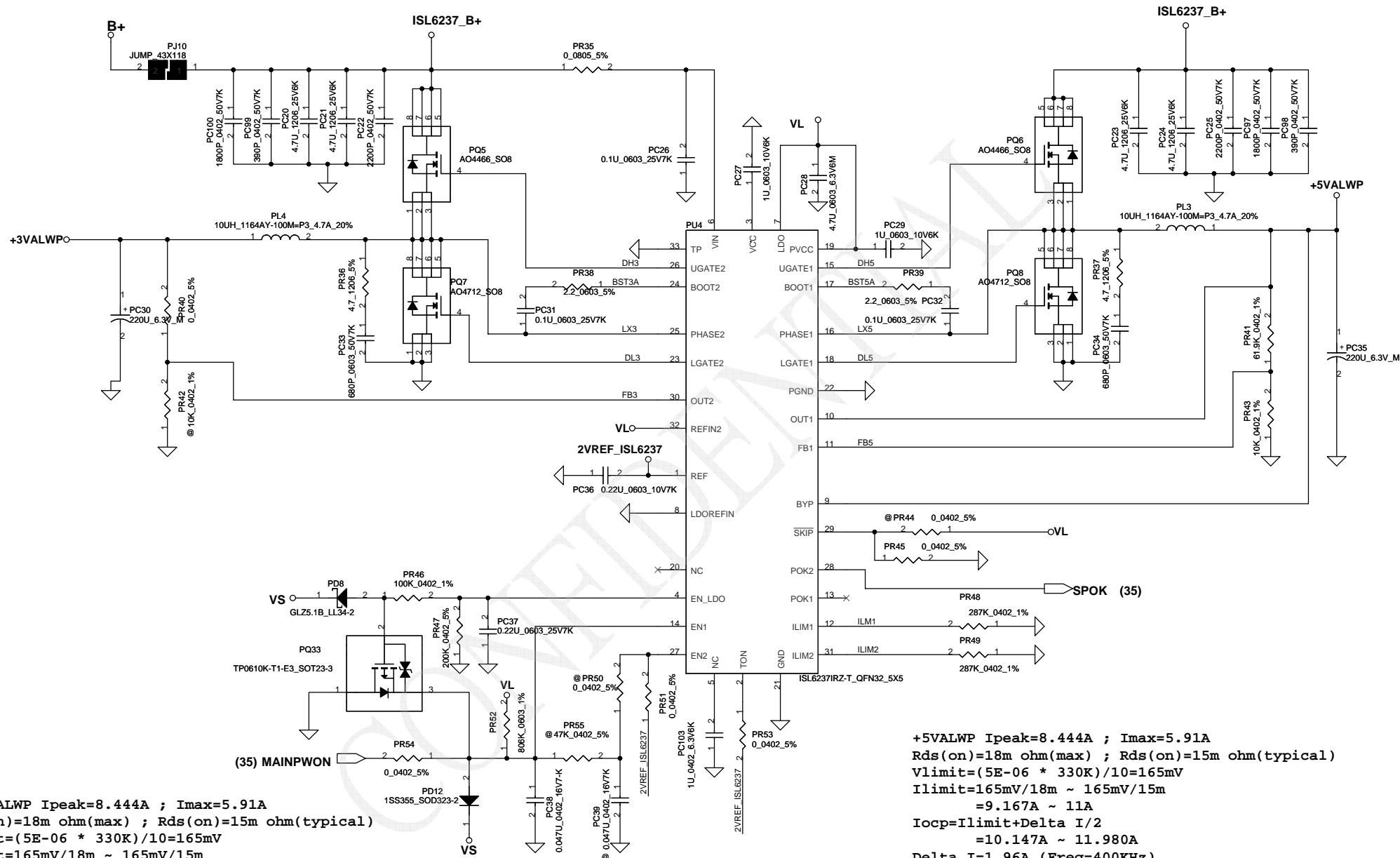
PH1 under CPU botten side :
 CPU thermal protection at 82 degree C
 Recovery at 56 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 92 degree C
 Recovery at 56 degree C



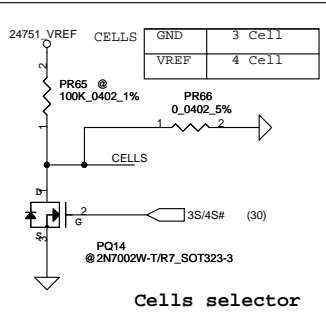
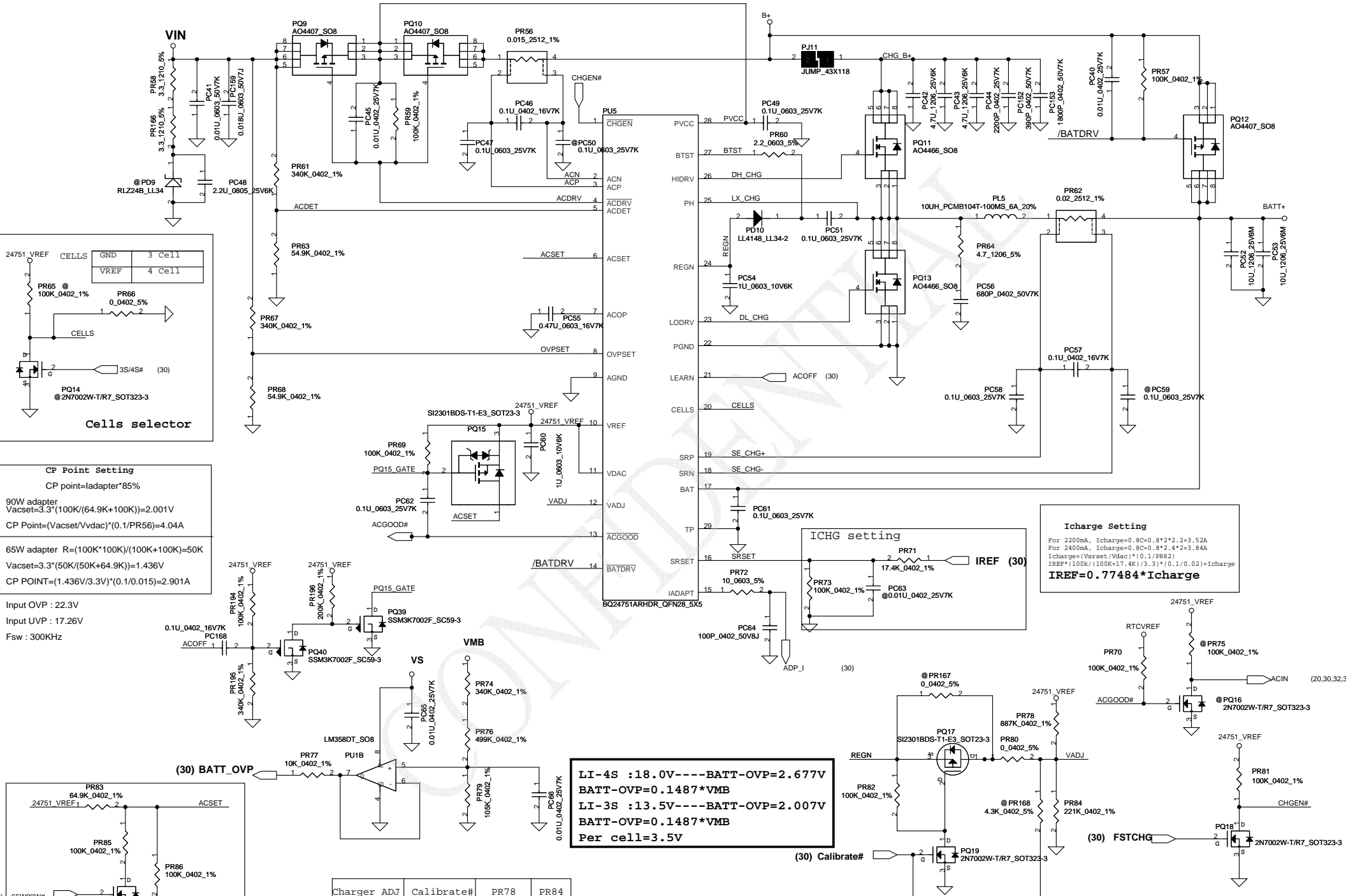
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+3.3VALWP Ipeak=8.444A ; Imax=5.91A
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 330K)/10=165mV
 Ilimit=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A
 Iocp=Ilimit+Delta I/2
 =10.134A ~ 11.967A
 Delta I=1.934A (Freq=300KHz)

+5VALWP Ipeak=8.444A ; Imax=5.91A
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 330K)/10=165mV
 Ilimit=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A
 Iocp=Ilimit+Delta I/2
 =10.147A ~ 11.980A
 Delta I=1.96A (Freq=400KHz)

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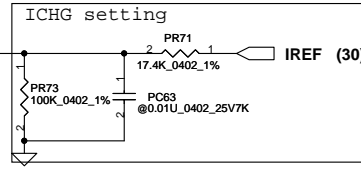
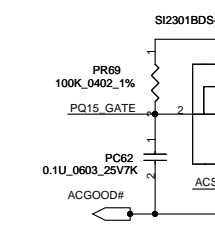
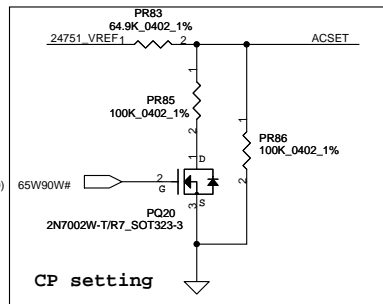


CP Point Setting
 CP point=ladapter*85%

90W adapter
 $V_{acset}=3.3 \cdot (100K/(64.9K+100K))=2.001V$
 $CP\ Point=(V_{acset}/V_{vdac}) \cdot (0.1/PR56)=4.04A$

65W adapter $R=(100K \cdot 100K)/(100K+100K)=50K$
 $V_{acset}=3.3 \cdot (50K/(50K+64.9K))=1.436V$
 $CP\ POINT=(1.436V/3.3V) \cdot (0.1/0.015)=2.901A$

Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz



Icharge Setting

For 2200mA, $I_{charge}=0.8C \cdot 0.8 \cdot 2.2=3.52A$
 For 2400mA, $I_{charge}=0.8C \cdot 0.8 \cdot 2.4=3.84A$
 $I_{charge}=(V_{acset}/V_{dac}) \cdot (0.1/PR62)$
 $IREF \cdot (100K/(100K+17.4K)/3.3) \cdot (0.1/0.02)=I_{charge}$
 $IREF=0.77484 \cdot I_{charge}$

LI-4S : 18.0V---BATT-OVP=2.677V
BATT-OVP=0.1487*VMB
LI-3S : 13.5V---BATT-OVP=2.007V
BATT-OVP=0.1487*VMB
Per cell=3.5V

Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	0
4.1V	L	887K	221K
4.2V	H	@	@

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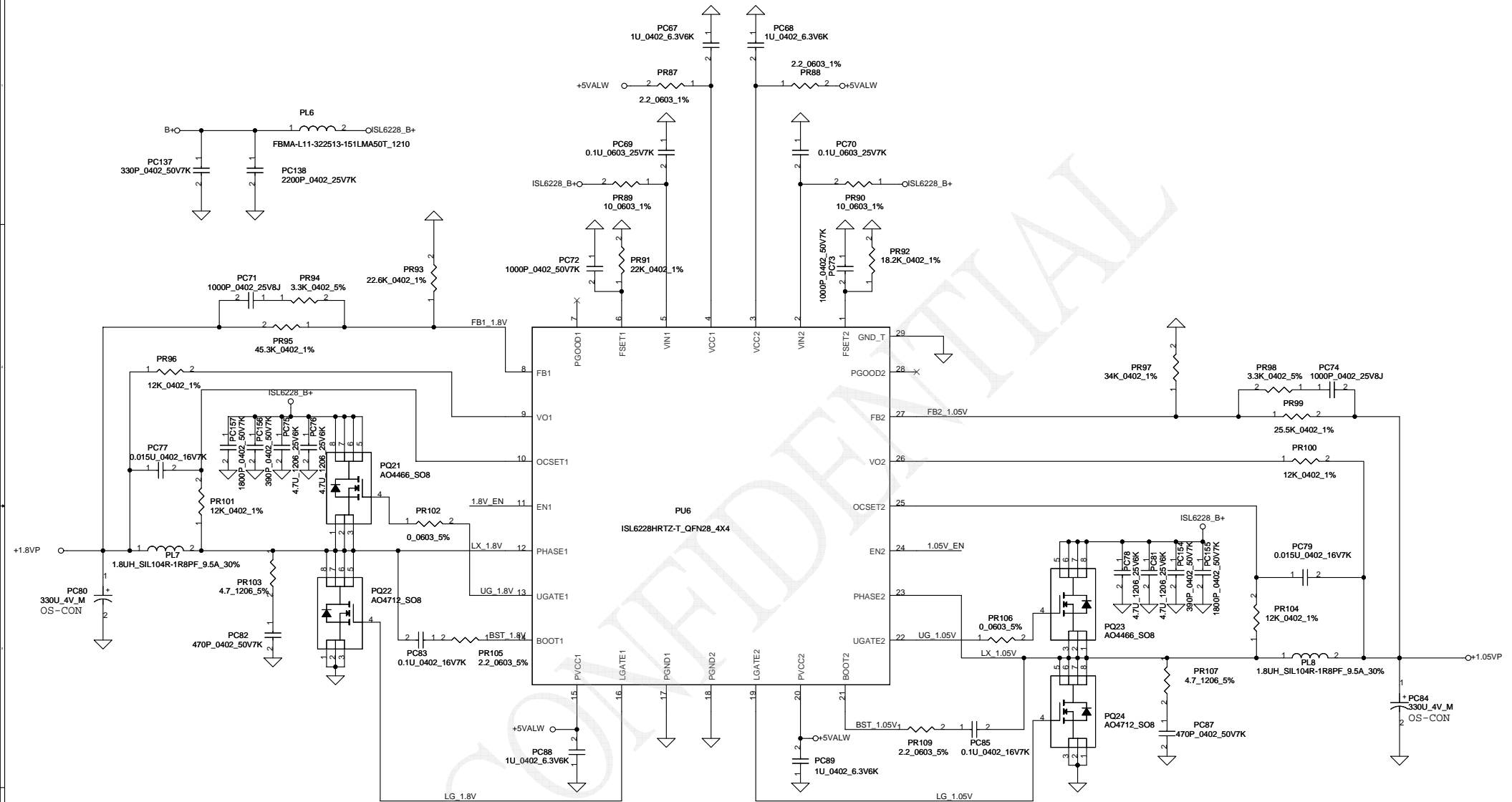
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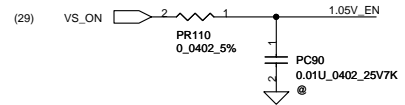
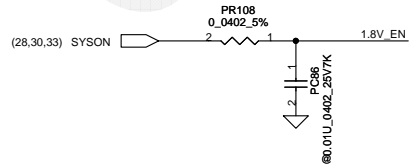
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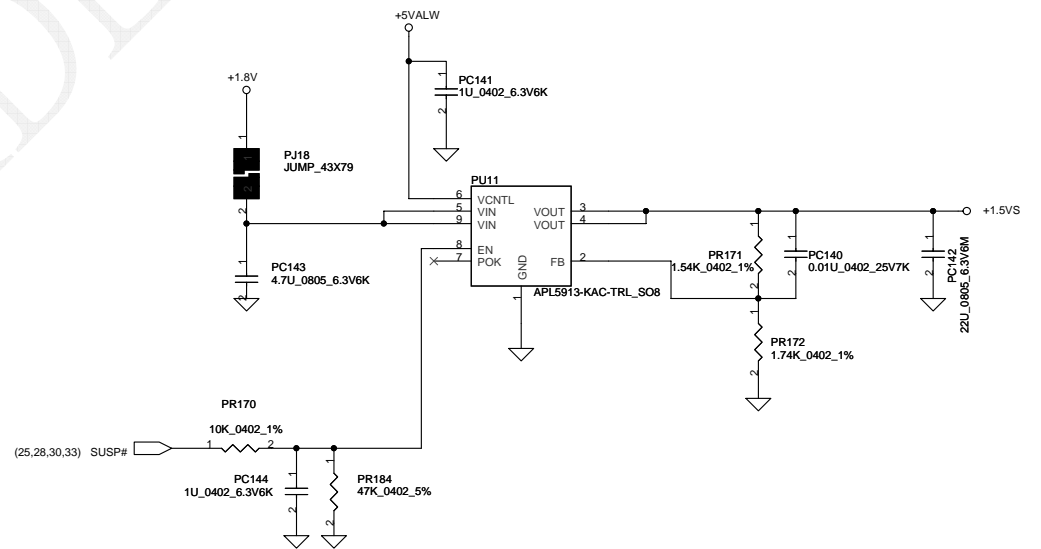
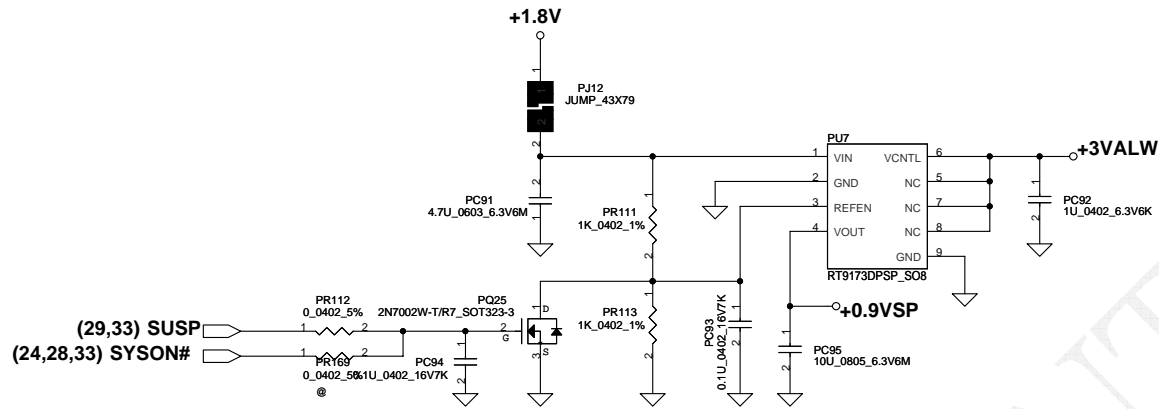


1.8VP Ipeak=9.45A ; Imax=6.615A
 DCR=10m ohm (max)
 $Rocset=(Iocp*DCR)/10E-06=12K$ ohm
 Iocp=12A
 $Csen=L/(Rocset*DCR)=0.015uF$
 Freq=303KHz
 $Rfset=1/(1.5E-10 * Freq)=22K$

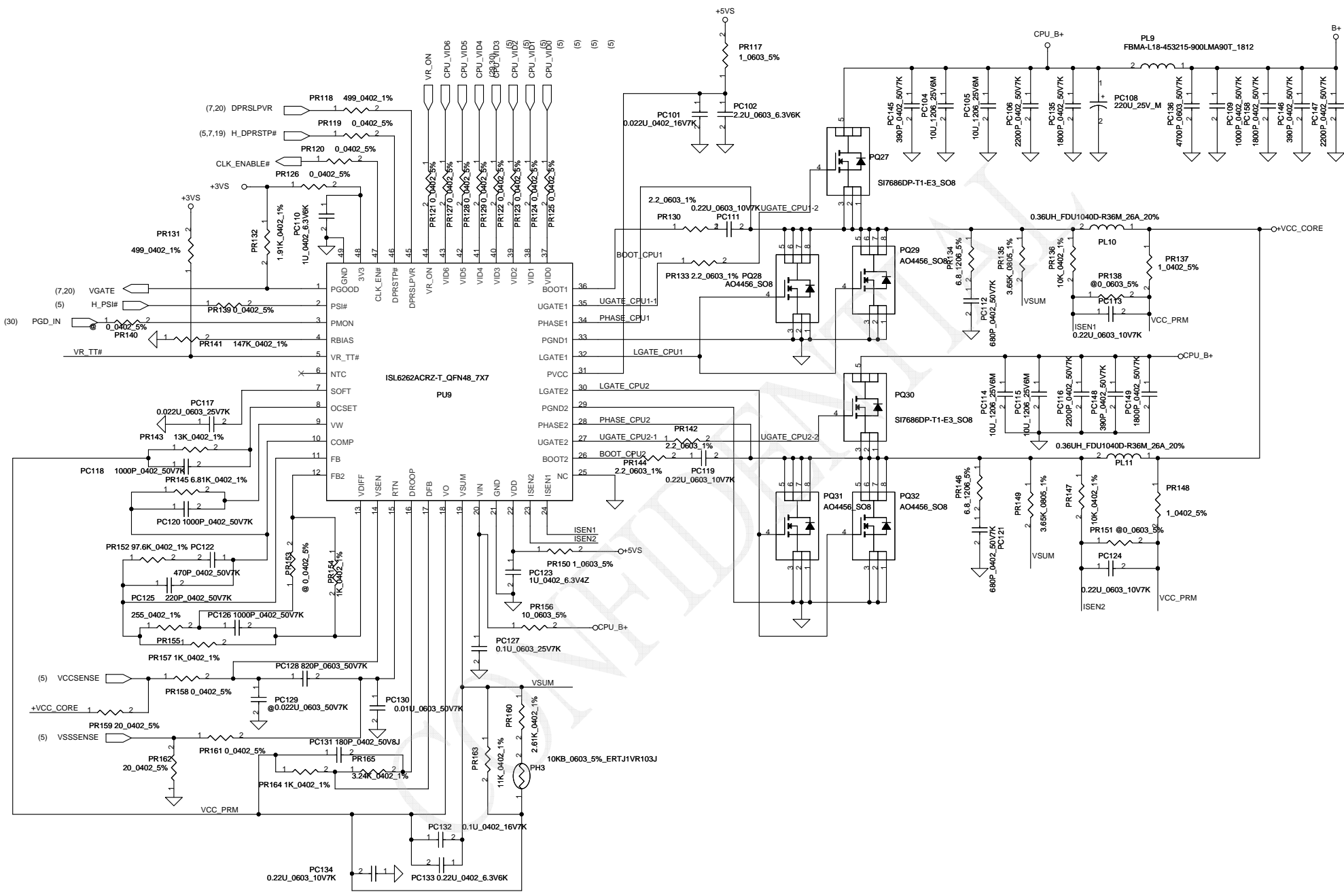
1.05VP Ipeak=8.8A ; Imax=6.16A
 DCR=10m ohm (max)
 $Rocset=(Iocp*DCR)/10E-06=12K$ ohm
 Iocp=12A
 $Csen=L/(Rocset*DCR)=0.015uF$
 Freq=366KHz
 $Rfset=1/(1.5E-10 * Freq)=18.2K$



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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Exchange battery connector pin	Use wrong model		35	Swap pin definition of PJP2	2007 12/12	EVT
2		For 2nd source of ISL6237		36	Add PC103 SE107105M80(S CER CAP 1U 6.3V M X5R 0603) on pin 5 of PU4	2007 12/12	EVT
3		Some risk in heavy load		37	Change PL5 to SH000005Z80(S COIL 10UH +-20% PCMB104T-100MS 6A)	2007 12/12	EVT
4		For EN function of PU4		36	Add PD12 SC100001K00(S DIO 1SS355 SOD323 T/R-5K) on pin 3 of PQ33 to VS	2007 12/12	EVT
5		Down size		36	Change PC38 from 0603 to 0402(SE076473K80)	2007 12/12	EVT
6		Down size		34	Change PC7 from 1206 to 0603(SE000005Z80)	2007 12/12	EVT
7		Down size		37	Change PC49 from 0805 to 0603(SE042104K80)	2007 12/12	EVT
8		Down size		36	Change PC28 from 0805 to 0603(SE107475M80)	2007 12/12	EVT
9		Down size		39	Change PC91 from 0805 to 0603(SE107475M80)	2007 12/12	EVT
10		Down size		39	Change PC96 from 0805 to 0603(SE107475M80)	2007 12/12	EVT
11		Down size		39	Change PC92 from 0603 to 0402(SE000000K80)	2007 12/12	EVT
12		Down size		39	Change PC97 from 0603 to 0402(SE000000K80)	2007 12/12	EVT
13		Down size		40	Change PC110 from 0603 to 0402(SE000000K80)	2007 12/12	EVT
14		Down size		35	Change PC14 from 0805 to 0603(SE026224K80)	2007 12/12	EVT
15		Down size		35	Change PC18 from 0805 to 0603(SE026224K80)	2007 12/12	EVT
16		For EMI		34	Add PC107 SE075472K80(S CER CAP 4700P 25V K X7R 0402) from VIN to GND	2007 12/12	EVT
17		For EMI		34	Add PC139 SE074331K80(S CER CAP 330P 50V K X7R 0402) from VIN to GND	2007 12/12	EVT
18		For EMI		40	Add PC135 SE074182K80(S CER CAP 1800P 50V K X7R 0402) from CPU_B+ to GND	2007 12/12	EVT
19		For EMI		40	Add PC136 SE025472K80(S CER CAP 4700P 50V K X7R 0603) from B+ to GND	2007 12/12	EVT
20		For EMI		38	Add PR103 SD001470B80(S RES 1/4W 4.7 +-5% 1206) from pin 12 of PU6 to PC82	2007 12/12	EVT
21		For EMI		38	Add PC82 SE074471K80(S CER CAP 470P 50V K X7R 0402) from PR103 to GND	2007 12/12	EVT
22		For EMI		38	Add PR107 SD001470B80(S RES 1/4W 4.7 +-5% 1206) from pin 23 of PU6 to PC82	2007 12/12	EVT
23		For EMI		38	Add PC87 SE074471K80(S CER CAP 470P 50V K X7R 0402) from PR107 to GND	2007 12/12	EVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24		For more current		34	Change PD11 in SCS00002F00(S SCH DIO PDS1040-13 POWERDI5)	2007 12/12	EVT
25		Space is not enough		34	Delete PD1	2007 12/18	EVT
26				37	Change PR70 Pin 1 to RTCVREF	2007 12/18	EVT
27		Down size		37	Change PC56 from 0603 to 0402(SE074681K80)	2007 12/18	EVT
28		Down size		40	Change PC112 from 0603 to 0402(SE074681K80)	2007 12/18	EVT
29		Down size		40	Change PC121 from 0603 to 0402(SE074681K80)	2007 12/18	EVT
30		Down size		36	Change PC103 from 0603 to 0402(SE000000K80)	2007 12/18	EVT
31		Down size		40	Change PC128 from 0603 to 0402(SE000003W00)	2007 12/20	EVT
32	APL5913 EN pin impedance must keep under 20K	For APL5913 EN risk		39	Change PR184 from 47K to 20K(SD028200280)	2007 12/31	EVT
33		Improve 3V/5V OCP		36	Change PR48v PR49 from 330K to 287K(SD000005D80) Change PL3V PL4 from 4.7uH to 10uH(SH000008R80)	2008 02/25	DVT
34		Improve Load line		40	Change PR165 from 4.42K to 3.24K(SD034324180)	2008 02/25	DVT
35		For EMI		34	Add PC96 1000pF(SE074102K80)	2008 02/25	DVT
36		For EMI			Add PC97v PC98v PC99v PC100v PC145v PC146v PC147v PC148v PC149v PC150v PC151v PC152v PC153v PC154v PC155v PC156v PC157 Delete PR64v PC56 "@"-mark Change PR38v PR39v PR60v PR105v PR109v PR130v PR144 from 0 to 2.2	2008 02/27	DVT
37							
38		Prevent ACOP issue		37	Add PC168v PQ39v PQ40v PR194v PR195v PR196	2008 02/27	DVT
39		HW request		39	Change PC144 to luF , delete PR184 "@" mark	2008 02/27	DVT
40		For EMI			Add PC158v PC159	2008 03/03	DVT
41		Thermal request		35	Change PR19 from 13.7K to 7.5K (SD034750180) Change PR22 from 15.4K to 17.4K (SD034174280)	2008 03/14	PVT1
42							
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