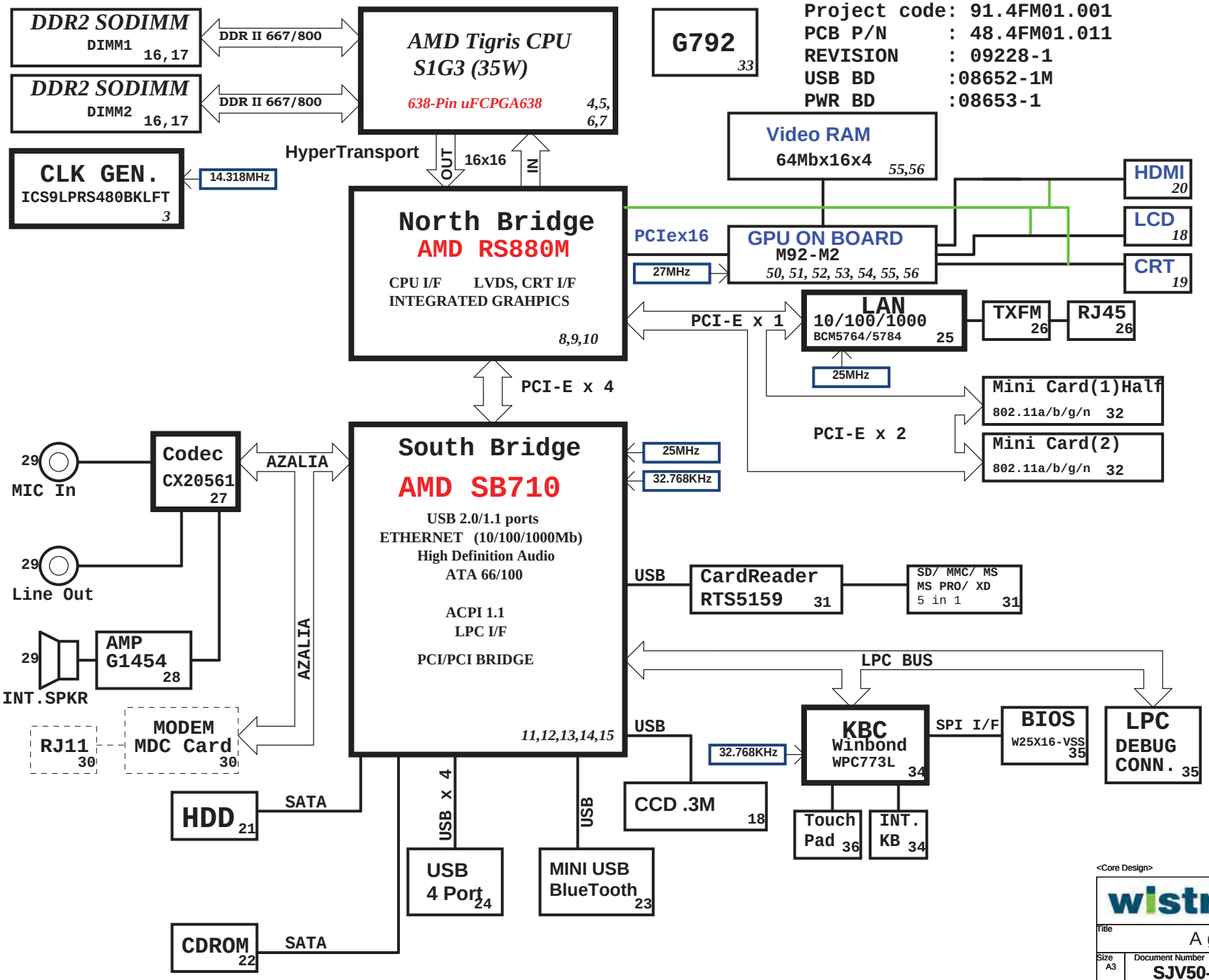
SJV50-TR Block Diagram



PCB Layer Stackup
L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D1V_S0 1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: A gift from Eko!

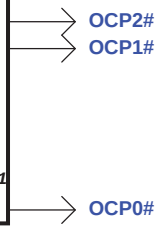
Size: A3 | Document Number: SJV50-TR | Rev: -1

Date: Monday, June 29, 2009 | Sheet 1 of 59

PCIE

PCIE0	LAN
PCIE1	MINICARD1
PCIE2	MINICARD2
PCIE3	

USB	
Pair	Device
11	CardReader
10	CCD
9	Mini Card2
8	USB4
7	USB1
6	USB2
5	BlueTooth
4	NC
3	NC
2	NC
1	Mini Card1
0	USB3



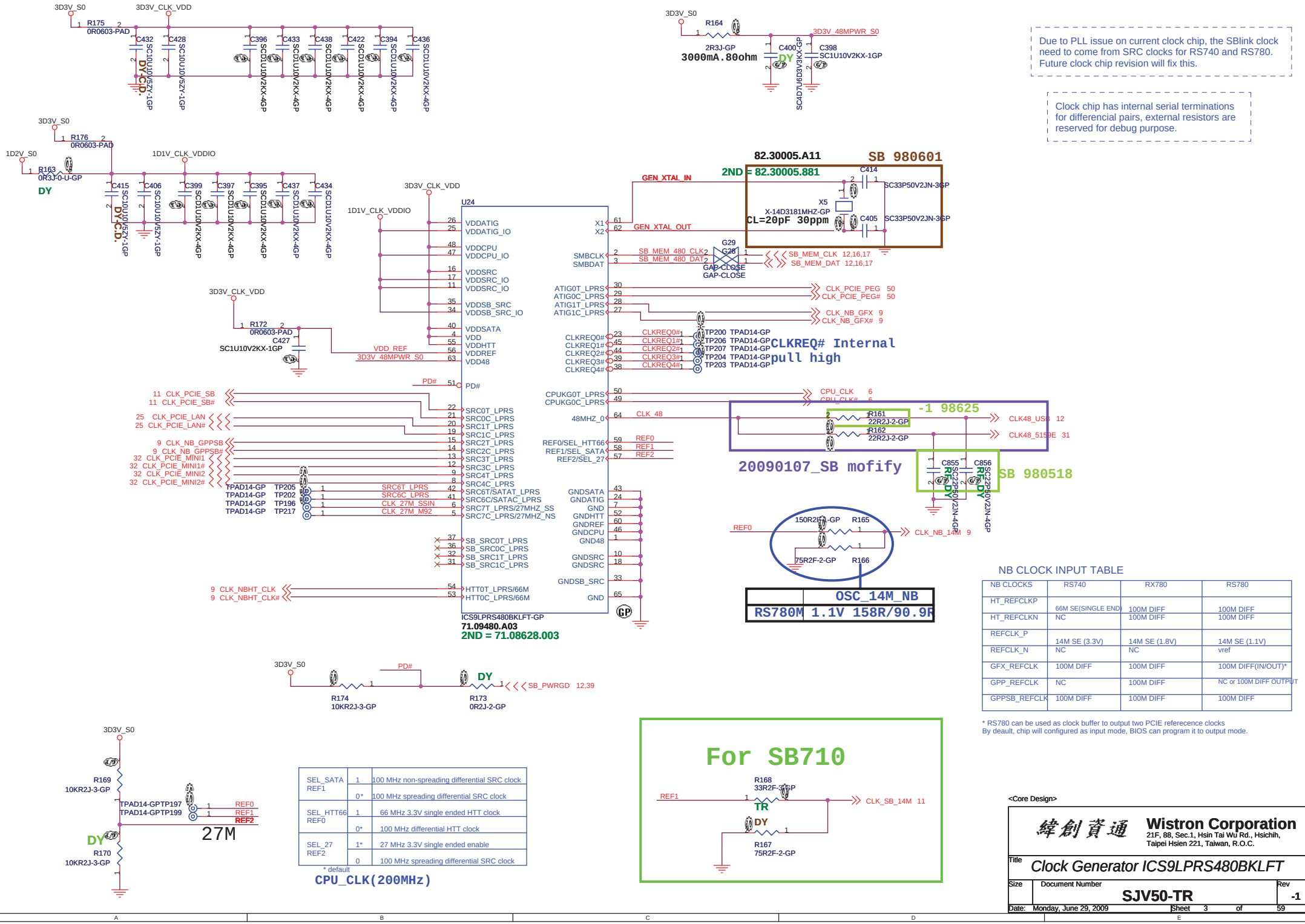
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

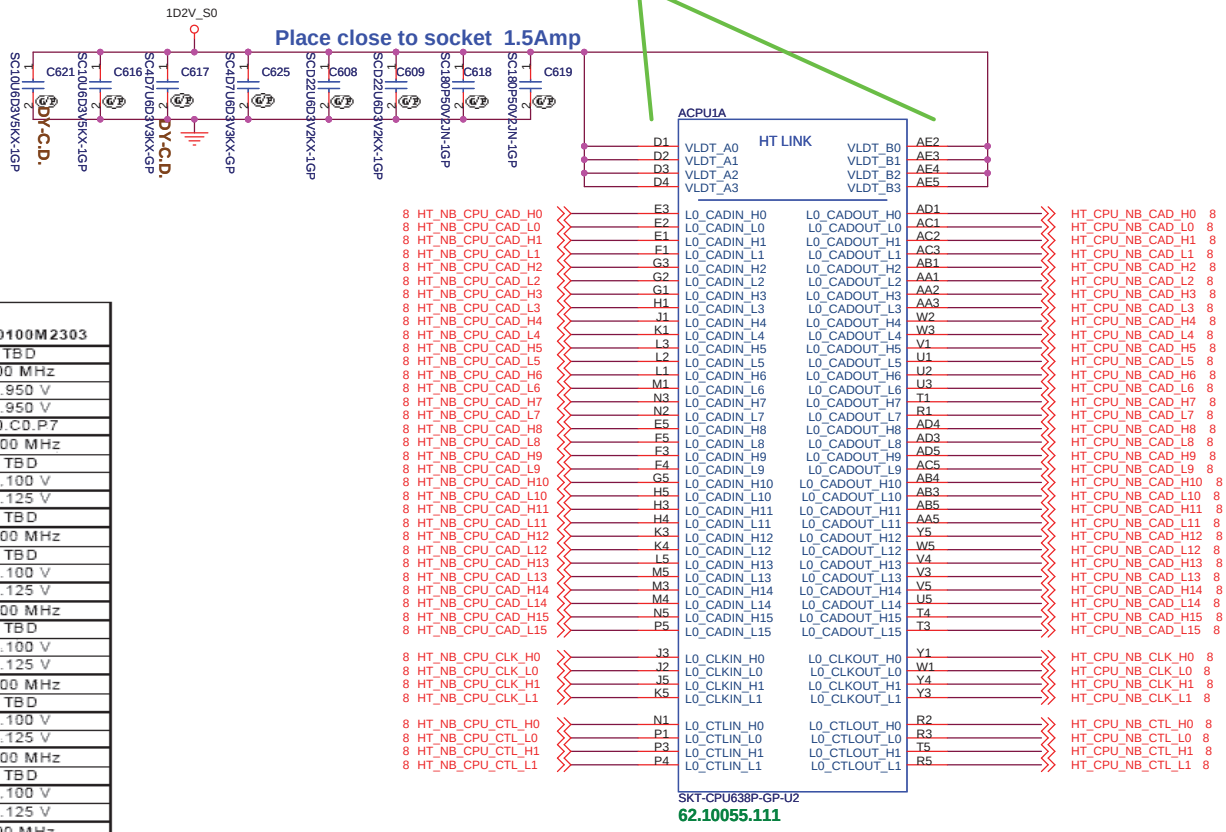
Title: USB&PCIE ROUTING

Size: A3 | Document Number: SJV50-TR | Rev: -1

Date: Monday, June 29, 2009 | Sheet 2 of 59


3D3V_S0
3D3V_CLK_VDD
R175 0R0603-PAD
C432 SC10U10V5ZY-1GP
C428 SC10U10V5ZY-1GP
C396 SC1U10V2KX-4GP
C433 SC1U10V2KX-4GP
C438 SC1U10V2KX-4GP
C422 SC1U10V2KX-4GP
C394 SC1U10V2KX-4GP
C436 SC1U10V2KX-4GP
DY C.D.
3D3V_S0
R164 2R3J-GP
3000mA.80ohm
C400 DY
3D3V_48MPWR_S0
C398 SC1U10V2KX-1GP
SC4D7U6D3V3KX-GP
Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.
Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.
3D3V_S0
R176 0R0603-PAD
1D2V_S0
R163 0R3J-0-U-GP
DY
1D1V_CLK_VDDIO
C415 SC10U10V5ZY-1GP
C406 SC10U10V5ZY-1GP
C399 SC1U10V2KX-4GP
C397 SC1U10V2KX-4GP
C395 SC1U10V2KX-4GP
C437 SC1U10V2KX-4GP
C434 SC1U10V2KX-4GP
DY C.D.
82.30005.A11
SB 980601
2ND = 82.30005.881
GEN_XTAL_IN
GEN_XTAL_OUT
X5
X-14D3181MHZ-GP
CL=20pF 30ppm
C414 SC33P50V2JN-3GP
C405 SC33P50V2JN-3GP
U24
VDDATIG
VDDATIG_IO
VDDCPU
VDDCPU_IO
VDDSRC
VDDSRC_IO
VDDSRC_IO
VDDSB_SRC
VDDSB_SRC_IO
VDDSATA
VDD
VDDHTT
VDDREF
VDD48
X1
X2
SMBCLK
SMBDAT
SB_MEM_480_CLK
SB_MEM_480_DAT
G29
G28
GAP-CLOSE
GAP-CLOSE
SB_MEM_CLK 12,16,17
SB_MEM_DAT 12,16,17
ATIG0T_LPRS
ATIG0C_LPRS
ATIG1T_LPRS
ATIG1C_LPRS
CLK_PCIE_PEG 50
CLK_PCIE_PEG# 50
CLK_NB_GFX 9
CLK_NB_GFX# 9
CLKREQ0#
CLKREQ1#
CLKREQ2#
CLKREQ3#
CLKREQ4#
TP200 TPAD14-GP
TP206 TPAD14-GP
TP207 TPAD14-GP
TP204 TPAD14-GP
TP203 TPAD14-GP
CLKREQ# Internal
pull high
3D3V_CLK_VDD
R172 0R0603-PAD
C427 SC1U10V2KX-1GP
VDD_REF
3D3V_48MPWR_S0
PD#
CPUKG0T_LPRS
CPUKG0C_LPRS
CPU_CLK 6
CPU_CLK# 6
48MHZ_0
CLK_48
-1 98625
R161 22R2J-2-GP
R162 22R2J-2-GP
CLK48_USB 12
CLK48_515E 31
20090107_SB mofify
C855 SC22P50V2JN-4GP
C856 SC22P50V2JN-4GP
DY
SB 980518
REF0
REF1
REF2
REF1/SEL_SATA
REF2/SEL_27
11 CLK_PCIE_SB
11 CLK_PCIE_SB#
25 CLK_PCIE_LAN
25 CLK_PCIE_LAN#
9 CLK_NB_GPPSB
9 CLK_NB_GPPSB#
32 CLK_PCIE_MINI1
32 CLK_PCIE_MINI1#
32 CLK_PCIE_MINI2
32 CLK_PCIE_MINI2#
SRC0T_LPRS
SRC0C_LPRS
SRC1T_LPRS
SRC1C_LPRS
SRC2T_LPRS
SRC2C_LPRS
SRC3T_LPRS
SRC3C_LPRS
SRC4T_LPRS
SRC4C_LPRS
SRC6T/SATAT_LPRS
SRC6C/SATAC_LPRS
SRC7T_LPRS/27MHZ_SS
SRC7C_LPRS/27MHZ_NS
TPAD14-GP TP205
TPAD14-GP TP202
TPAD14-GP TP196
TPAD14-GP TP217
SRC6T_LPRS
SRC6C_LPRS
CLK_27M_SSIN
CLK_27M_M92
SB_SRC0T_LPRS
SB_SRC0C_LPRS
SB_SRC1T_LPRS
SB_SRC1C_LPRS
9 CLK_NBHT_CLK
9 CLK_NBHT_CLK#
HTT0T_LPRS/66M
HTT0C_LPRS/66M
GNDSATA
GNDATIG
GND
GNDHTT
GNDREF
GNDCPU
GND48
GNDSRC
GNDSRC
GNDSB_SRC
GND
ICS9LPRS480BKLFT-GP
71.09480.A03
2ND = 71.08628.003
REF0
150R2F-GP R165
75R2F-2-GP R166
CLK_NB_14M 9
OSC_14M_NB
RS780M 1.1V 158R/90.9R
3D3V_S0
PD#
R174 10KR2J-3-GP
DY
R173 0R2J-2-GP
SB_PWRGD 12,39
NB CLOCK INPUT TABLE
NB CLOCKS | RS740 | RX780 | RS780
HT_REFCLKP | 66M SE(SINGLE END) | 100M DIFF | 100M DIFF
HT_REFCLKN | NC | 100M DIFF | 100M DIFF
REFCLK_P | 14M SE (3.3V) | 14M SE (1.8V) | 14M SE (1.1V)
REFCLK_N | NC | NC | vref
GFX_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF(IN/OUT)*
GPP_REFCLK | NC | 100M DIFF | NC or 100M DIFF OUTPUT
GPPSB_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF
* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.
3D3V_S0
R169 10KR2J-3-GP
TPAD14-GPTP197
TPAD14-GPTP199
REF0
REF1
REF2
27M
DY
R170 10KR2J-3-GP
SEL_SATA REF1
1 100 MHz non-spreading differential SRC clock
0* 100 MHz spreading differential SRC clock
SEL_HTT66 REF0
1 66 MHz 3.3V single ended HTT clock
0* 100 MHz differential HTT clock
SEL_27 REF2
1* 27 MHz 3.3V single ended enable
0 100 MHz spreading differential SRC clock
* default
CPU_CLK(200MHz)
For SB710
REF1
R168 33R2F-GP
TR
DY
R167 75R2F-2-GP
CLK_SB_14M 11
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator ICS9LPRS480BKLFT
Size
Document Number
SJV50-TR
Rev
-1
Date: Monday, June 29, 2009
Sheet 3 of 59

Placement note:
10ux1,4.7ux1,0.22ux1,180px1 for each group



SKT-BGA638H176

State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

<Core Design>

緯創資通 **Wistron Corporation**
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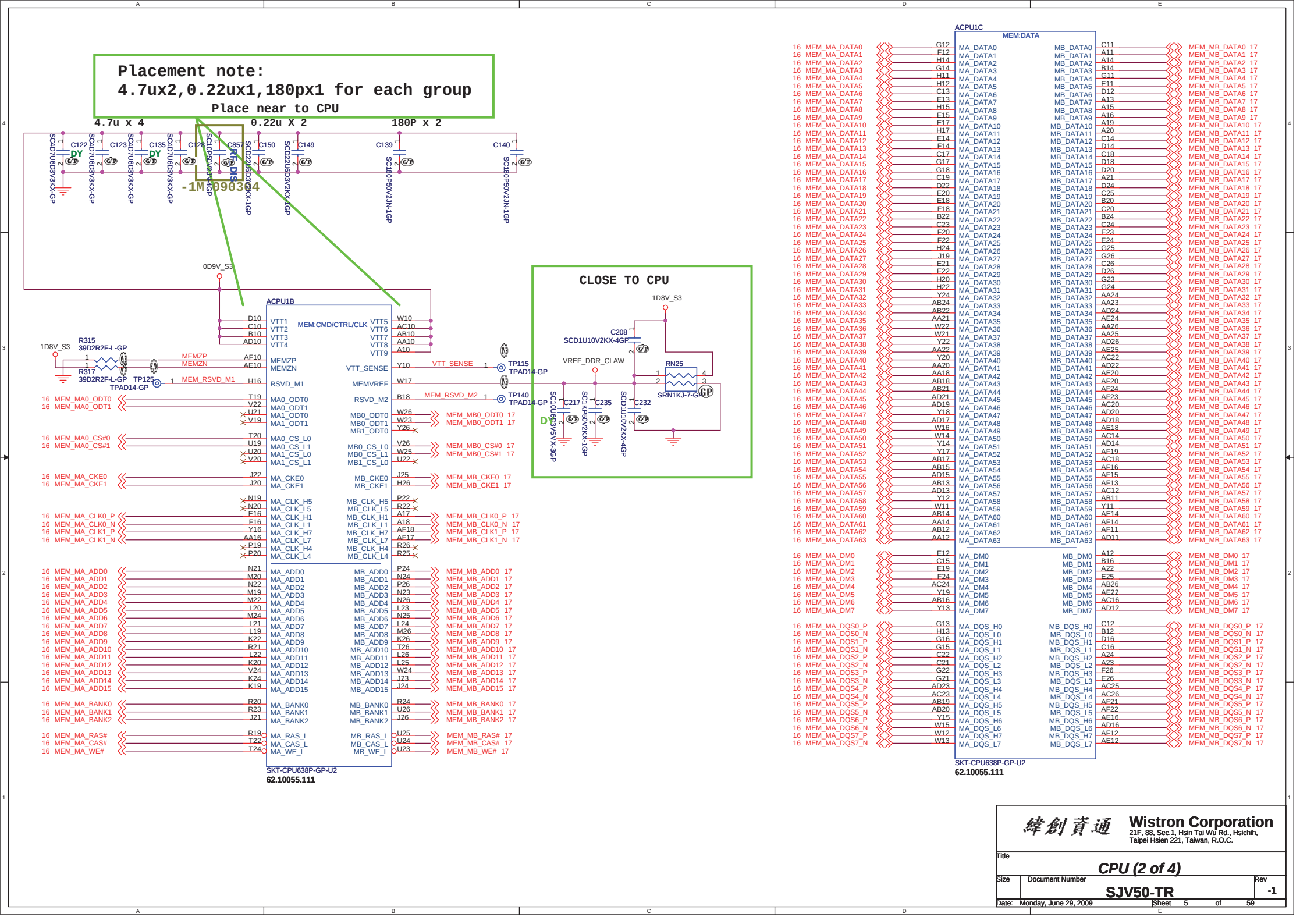
Title: ***CPU (1 of 4)***

Size | Document Number: **SJV50-TR** | Rev: -1

Date: Monday, June 29, 2009 | Sheet 4 of 59


Placement note:
4.7ux2,0.22ux1,180px1 for each group
Place near to CPU
4.7u x 4
0.22u X 2
180P x 2
-1M090334
CLOSE TO CPU
ACPU1B
ACPU1C
MEM:CMD/CTRL/CLK
MEM:DATA
SKT-CPU638P-GP-U2
62.10055.111
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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CPU (2 of 4)
SJV50-TR
-1
Monday, June 29, 2009
Sheet 5 of 59

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

SB_980430

Cloce To CPU

For HDT DBG

internal pull high 300 ohm

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

R614,R615
PU use 300R
TR use 510R

SA_980326

SB_980511

SA_20081030

CPU exceeds to 125℃

ACPU1D

SKT-CPU638P-GP-U2
62.10055.111

HDT Connectors

HDT1
SMC-CONN26A-FP

<Core Design>

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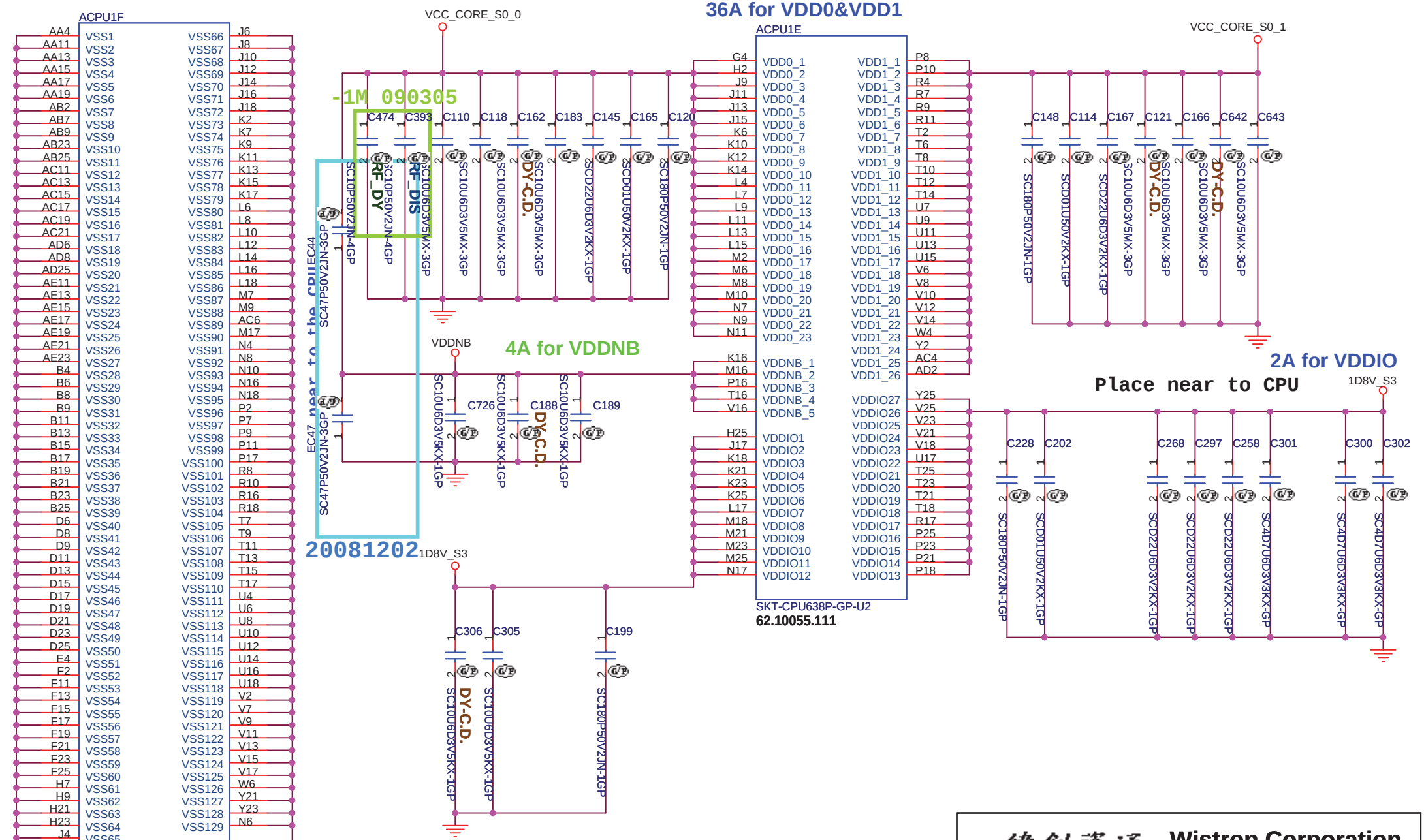
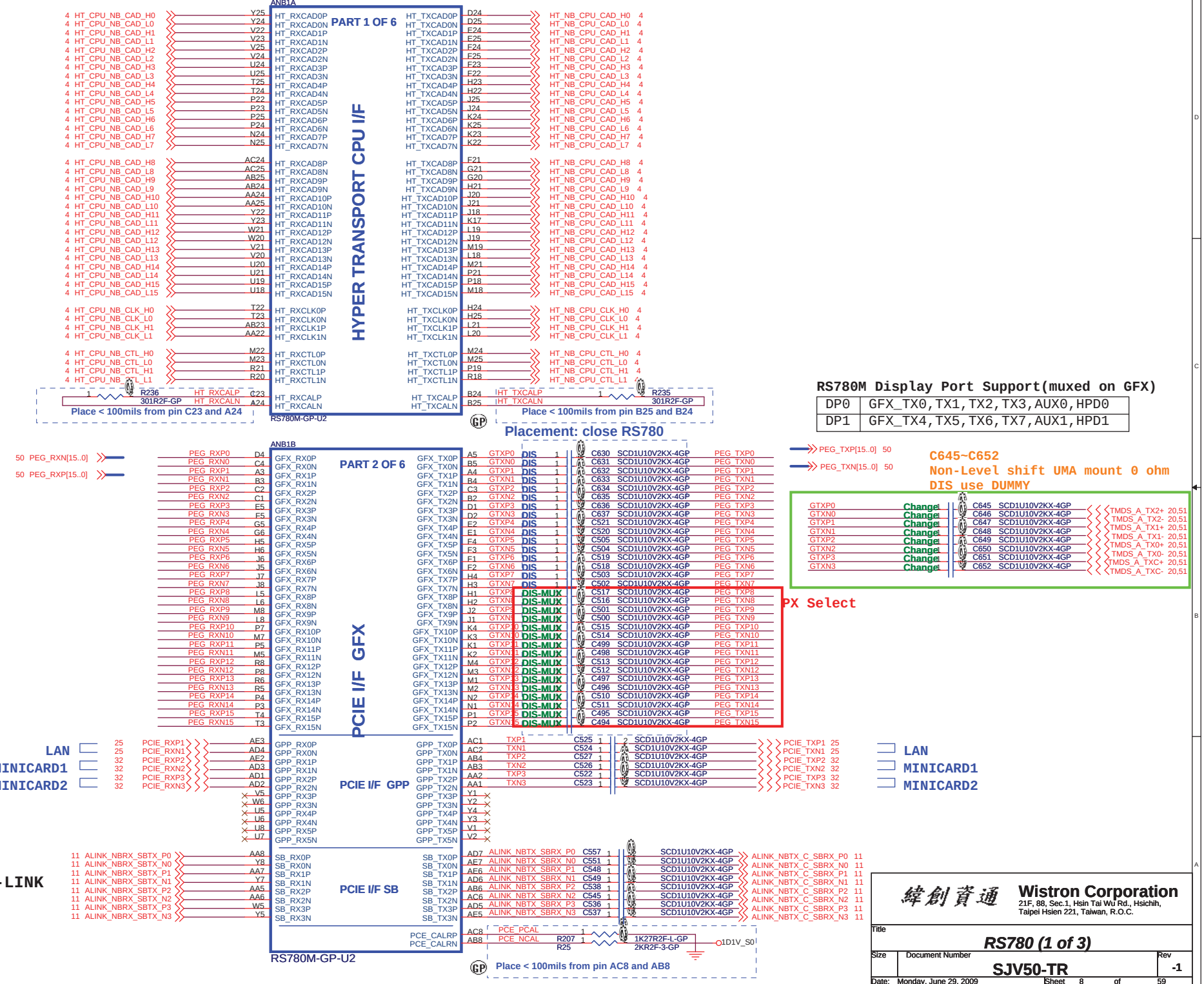
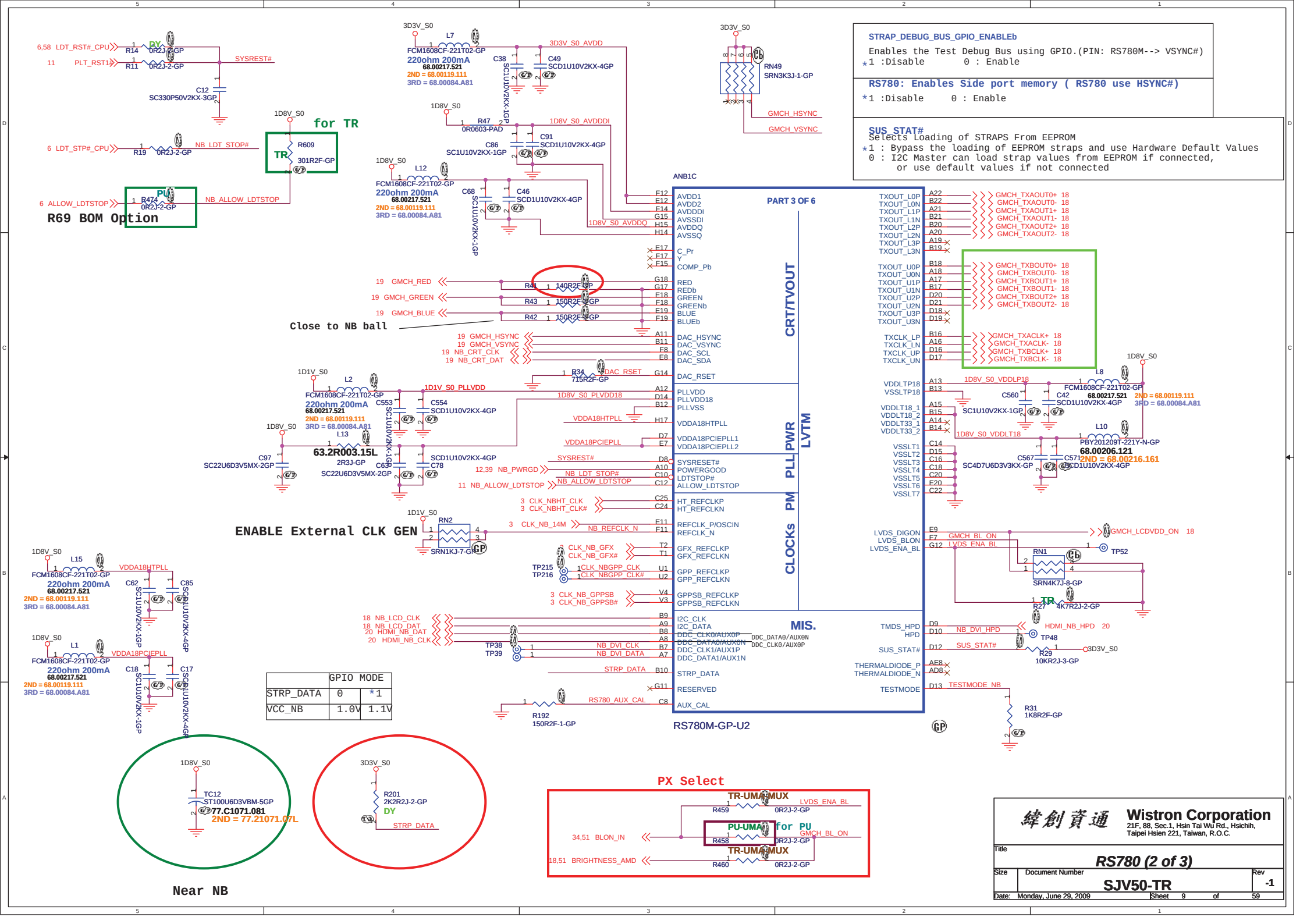
Title: CPU (3 of 4)		
Size	Document Number: SJV50-TR	Rev: -1
Date: Monday, June 29, 2009	Sheet 6 of 59	

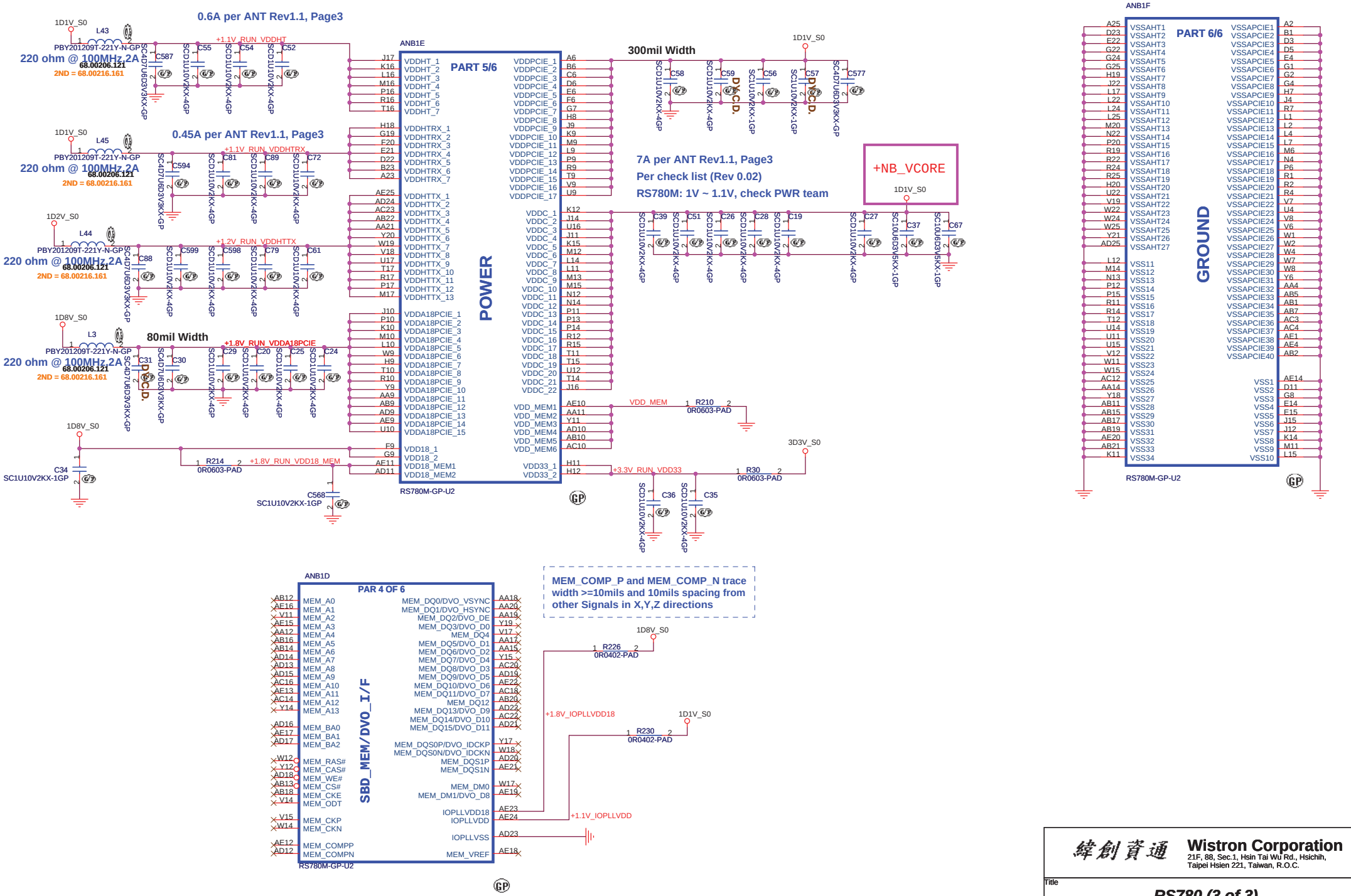

ACPU1F
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35 VSS36 VSS37 VSS38 VSS39 VSS40 VSS41 VSS42 VSS43 VSS44 VSS45 VSS46 VSS47 VSS48 VSS49 VSS50 VSS51 VSS52 VSS53 VSS54 VSS55 VSS56 VSS57 VSS58 VSS59 VSS60 VSS61 VSS62 VSS63 VSS64 VSS65
VSS66 VSS67 VSS68 VSS69 VSS70 VSS71 VSS72 VSS73 VSS74 VSS75 VSS76 VSS77 VSS78 VSS79 VSS80 VSS81 VSS82 VSS83 VSS84 VSS85 VSS86 VSS87 VSS88 VSS89 VSS90 VSS91 VSS92 VSS93 VSS94 VSS95 VSS96 VSS97 VSS98 VSS99 VSS100 VSS101 VSS102 VSS103 VSS104 VSS105 VSS106 VSS107 VSS108 VSS109 VSS110 VSS111 VSS112 VSS113 VSS114 VSS115 VSS116 VSS117 VSS118 VSS119 VSS120 VSS121 VSS122 VSS123 VSS124 VSS125 VSS126 VSS127 VSS128 VSS129
SKT-CPU638P-GP-U2
62.10055.111
VCC_CORE_S0_0
-1M 090305
C474 C393 C110 C118 C162 C183 C145 C165 C120
SC10P50V2JN-4GP
RF_DY
RF_DIS
SC10U6D3V5MX-3GP
DY-C.D.
SCD22U6D3V2KX-1GP
SCD01U50V2KX-1GP
SC180P50V2JN-1GP
EC44
SC47P50V2JN-3GP
near to the CPU
EC47
SC47P50V2JN-3GP
20081202
VDDNB
4A for VDDNB
C726 C188 C189
SC10U6D3V5KX-1GP
1D8V_S3
C306 C305 C199
SC10U6D3V5KX-1GP
SC180P50V2JN-1GP
36A for VDD0&VDD1
ACPU1E
VDD0_1 VDD0_2 VDD0_3 VDD0_4 VDD0_5 VDD0_6 VDD0_7 VDD0_8 VDD0_9 VDD0_10 VDD0_11 VDD0_12 VDD0_13 VDD0_14 VDD0_15 VDD0_16 VDD0_17 VDD0_18 VDD0_19 VDD0_20 VDD0_21 VDD0_22 VDD0_23
VDD1_1 VDD1_2 VDD1_3 VDD1_4 VDD1_5 VDD1_6 VDD1_7 VDD1_8 VDD1_9 VDD1_10 VDD1_11 VDD1_12 VDD1_13 VDD1_14 VDD1_15 VDD1_16 VDD1_17 VDD1_18 VDD1_19 VDD1_20 VDD1_21 VDD1_22 VDD1_23 VDD1_24 VDD1_25 VDD1_26
VDDNB_1 VDDNB_2 VDDNB_3 VDDNB_4 VDDNB_5
VDDIO1 VDDIO2 VDDIO3 VDDIO4 VDDIO5 VDDIO6 VDDIO7 VDDIO8 VDDIO9 VDDIO10 VDDIO11 VDDIO12
VDDIO27 VDDIO26 VDDIO25 VDDIO24 VDDIO23 VDDIO22 VDDIO21 VDDIO20 VDDIO19 VDDIO18 VDDIO17 VDDIO16 VDDIO15 VDDIO14 VDDIO13
SKT-CPU638P-GP-U2
62.10055.111
VCC_CORE_S0_1
C148 C114 C167 C121 C166 C642 C643
SC180P50V2JN-1GP
SCD01U50V2KX-1GP
SCD22U6D3V2KX-1GP
SC10U6D3V5MX-3GP
DY-C.D.
2A for VDDIO
Place near to CPU
1D8V_S3
C228 C202
C268 C297 C258 C301
C300 C302
SC4D7U6D3V3KX-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (4 of 4)
Size
Document Number
SJV50-TR
Rev
-1
Date: Monday, June 29, 2009
Sheet 7 of 59



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: RS780 (1 of 3)	
Size	Document Number: SJV50-TR
Rev: -1	
Date: Monday, June 29, 2009	Sheet 8 of 59



	GPIO MODE	
STRP_DATA	0	*1
VCC_NB	1.0V	1.1V


0.6A per ANT Rev1.1, Page3
0.45A per ANT Rev1.1, Page3
80mil Width
300mil Width
7A per ANT Rev1.1, Page3
Per check list (Rev 0.02)
RS780M: 1V ~ 1.1V, check PWR team
+NB_VCORE
ANB1E
PART 5/6
POWER
RS780M-GP-U2
ANB1F
PART 6/6
GROUND
RS780M-GP-U2
ANB1D
PAR 4 OF 6
SBD_MEM/DVO_I/F
RS780M-GP-U2
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions
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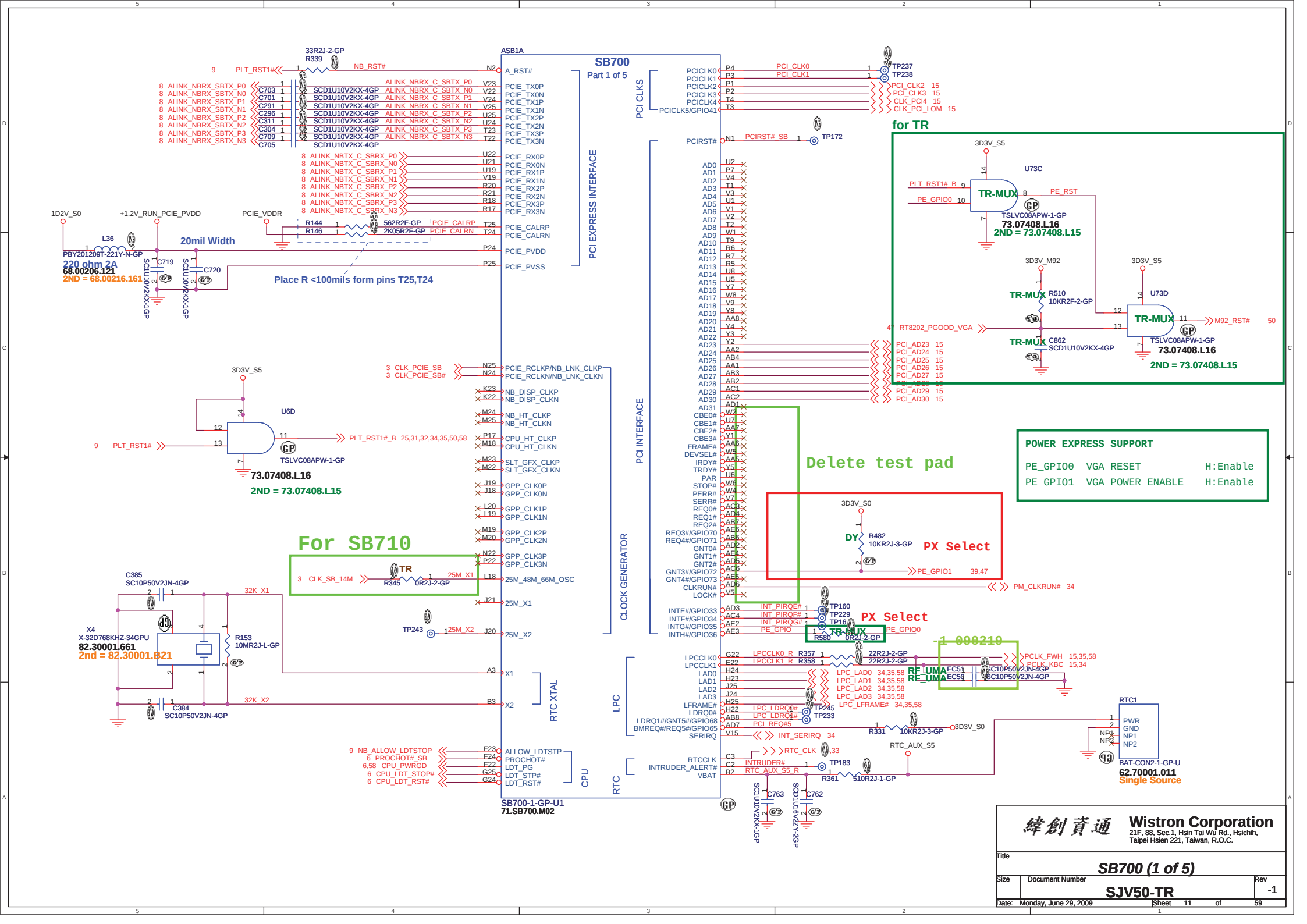
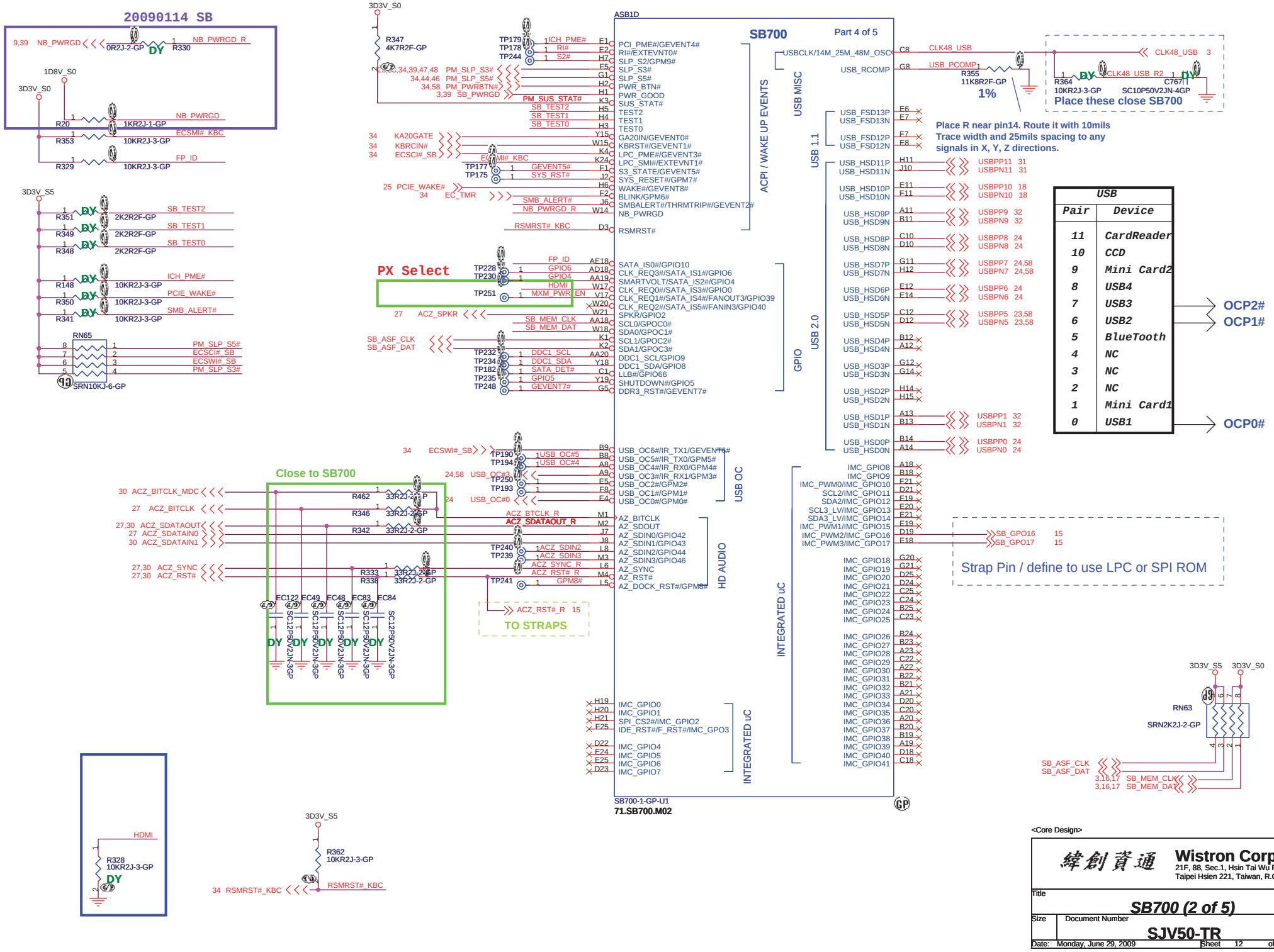
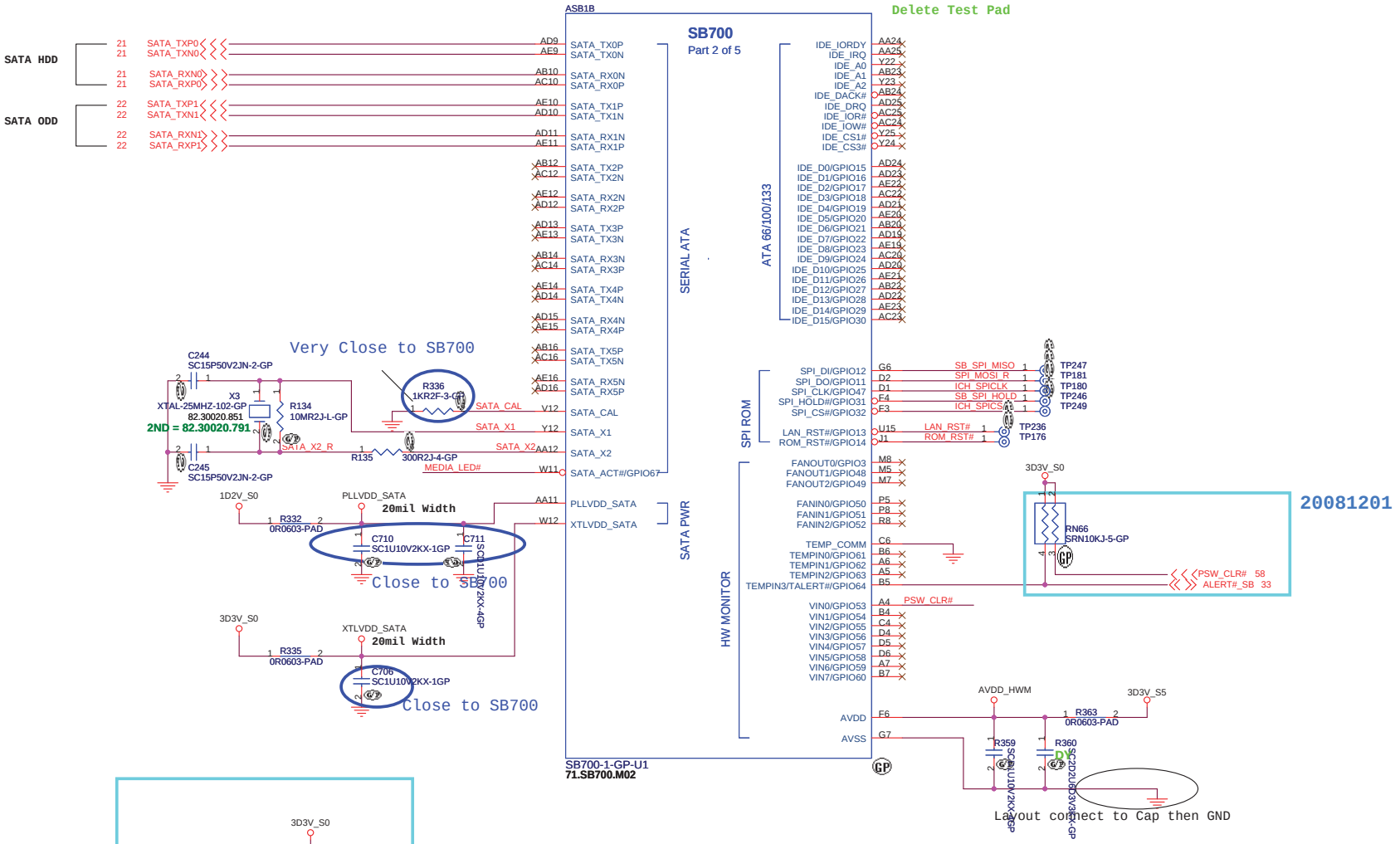
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
RS780 (3 of 3)
SJV50-TR
-1
Monday, June 29, 2009
10
59


SB700
Part 1 of 5
ASB1A
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTRAL
CPU
RTC
for TR
TR-MUX
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
Delete test pad
PX Select
For SB710
POWER EXPRESS SUPPORT
PE_GPIO0 VGA RESET H:Enable
PE_GPIO1 VGA POWER ENABLE H:Enable
20mil Width
Place R <100mils form pins T25,T24
220 ohm 2A
68.00206.121
2ND = 68.00216.161
X4
X-32D768KHZ-34GPU
82.30001.661
2nd = 82.30001.821
SB700-1-GP-U1
71.SB700.M02
BAT-CON2-1-GP-U
62.70001.011
Single Source
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
SB700 (1 of 5)
SJV50-TR
Rev -1
Monday, June 29, 2009
Sheet 11 of 59


20090114 SB
SB700
Part 4 of 5
ASB1D
PX Select
Close to SB700
TO STRAPS
Strap Pin / define to use LPC or SPI ROM
Place these close SB700
Place R near pin14. Route it with 10mils
Trace width and 25mils spacing to any
signals in X, Y, Z directions.
USB
Pair Device
11 CardReader
10 CCD
9 Mini Card2
8 USB4
7 USB3
6 USB2
5 BlueTooth
4 NC
3 NC
2 NC
1 Mini Card1
0 USB1
OCP2#
OCP1#
OCP0#
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
INTEGRATED uC
SB700-1-GP-U1
71.SB700.M02
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
SB700 (2 of 5)
Size
Document Number
SJV50-TR
Rev
-1
Date: Monday, June 29, 2009
Sheet 12 of 59



<Core Design>

Wistron Corporation
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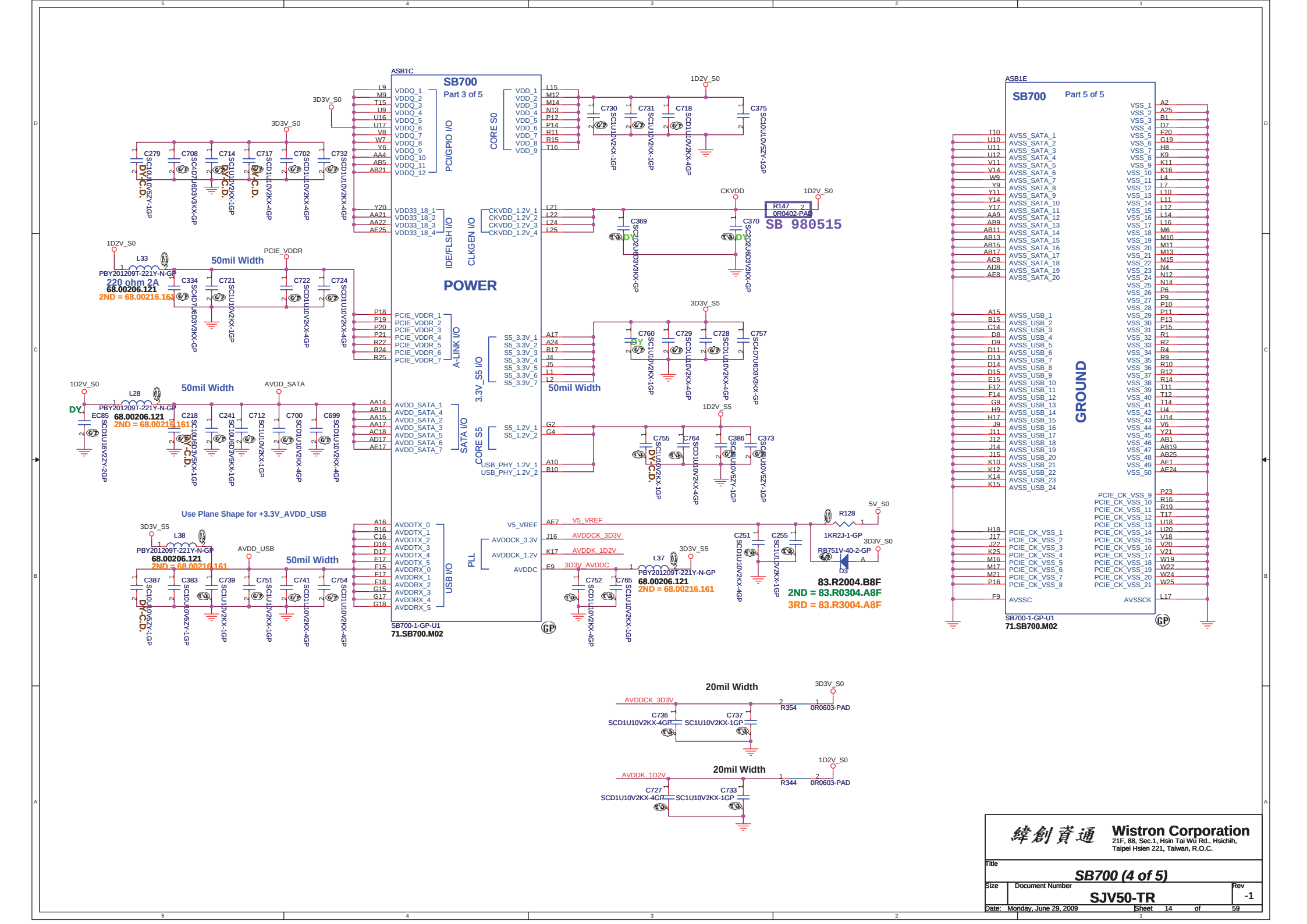
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB700 (3 of 5)

Size | Document Number: SJV50-TR | Rev: -1

Date: Monday, June 29, 2009 | Sheet 13 of 59


ASB1C
SB700
Part 3 of 5
POWER
PCI/GPIO I/O
CORE S0
IDE/FLSH I/O
CLKGEN I/O
A-LINK I/O
3.3V_S5 I/O
SATA I/O
CORE S5
USB I/O
PLL
VDDQ_1
VDDQ_2
VDDQ_3
VDDQ_4
VDDQ_5
VDDQ_6
VDDQ_7
VDDQ_8
VDDQ_9
VDDQ_10
VDDQ_11
VDDQ_12
VDD_1
VDD_2
VDD_3
VDD_4
VDD_5
VDD_6
VDD_7
VDD_8
VDD_9
VDD33_18_1
VDD33_18_2
VDD33_18_3
VDD33_18_4
CKVDD_1.2V_1
CKVDD_1.2V_2
CKVDD_1.2V_3
CKVDD_1.2V_4
PCIE_VDDR_1
PCIE_VDDR_2
PCIE_VDDR_3
PCIE_VDDR_4
PCIE_VDDR_5
PCIE_VDDR_6
PCIE_VDDR_7
S5_3.3V_1
S5_3.3V_2
S5_3.3V_3
S5_3.3V_4
S5_3.3V_5
S5_3.3V_6
S5_3.3V_7
S5_1.2V_1
S5_1.2V_2
USB_PHY_1.2V_1
USB_PHY_1.2V_2
AVDD_SATA_1
AVDD_SATA_4
AVDD_SATA_2
AVDD_SATA_3
AVDD_SATA_5
AVDD_SATA_6
AVDD_SATA_7
AVDDTX_0
AVDDTX_1
AVDDTX_2
AVDDTX_3
AVDDTX_4
AVDDTX_5
AVDDRX_0
AVDDRX_1
AVDDRX_2
AVDDRX_3
AVDDRX_4
AVDDRX_5
V5_VREF
AVDDCK_3D3V
AVDDCK_1.2V
AVDDC
SB700-1-GP-U1
71.SB700.M02
ASB1E
SB700
Part 5 of 5
GROUND
VSS_1
VSS_2
VSS_3
VSS_4
VSS_5
VSS_6
VSS_7
VSS_8
VSS_9
VSS_10
VSS_11
VSS_12
VSS_13
VSS_14
VSS_15
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VSS_48
VSS_49
VSS_50
AVSS_SATA_1
AVSS_SATA_2
AVSS_SATA_3
AVSS_SATA_4
AVSS_SATA_5
AVSS_SATA_6
AVSS_SATA_7
AVSS_SATA_8
AVSS_SATA_9
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AVSS_SATA_12
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AVSS_SATA_14
AVSS_SATA_15
AVSS_SATA_16
AVSS_SATA_17
AVSS_SATA_18
AVSS_SATA_19
AVSS_SATA_20
AVSS_USB_1
AVSS_USB_2
AVSS_USB_3
AVSS_USB_4
AVSS_USB_5
AVSS_USB_6
AVSS_USB_7
AVSS_USB_8
AVSS_USB_9
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AVSS_USB_20
AVSS_USB_21
AVSS_USB_22
AVSS_USB_23
AVSS_USB_24
PCIE_CK_VSS_1
PCIE_CK_VSS_2
PCIE_CK_VSS_3
PCIE_CK_VSS_4
PCIE_CK_VSS_5
PCIE_CK_VSS_6
PCIE_CK_VSS_7
PCIE_CK_VSS_8
PCIE_CK_VSS_9
PCIE_CK_VSS_10
PCIE_CK_VSS_11
PCIE_CK_VSS_12
PCIE_CK_VSS_13
PCIE_CK_VSS_14
PCIE_CK_VSS_15
PCIE_CK_VSS_16
PCIE_CK_VSS_17
PCIE_CK_VSS_18
PCIE_CK_VSS_19
PCIE_CK_VSS_20
PCIE_CK_VSS_21
AVSSC
AVSSCK
SB700-1-GP-U1
71.SB700.M02
3D3V_S0
1D2V_S0
3D3V_S5
1D2V_S5
CKVDD
5V_S0
PCIE_VDDR
AVDD_SATA
AVDD_USB
L33
L28
L38
L37
PBY201209T-221Y-N-GP
220 ohm 2A
68.00206.121
2ND = 68.00216.161
50mil Width
Use Plane Shape for +3.3V_AVDD_USB
20mil Width
R147
0R0402-PAD
SB 980515
R128
1KR2J-1-GP
RB751V-40-2-GP
D3
83.R2004.B8F
2ND = 83.R0304.A8F
3RD = 83.R3004.A8F
R354
R344
0R0603-PAD
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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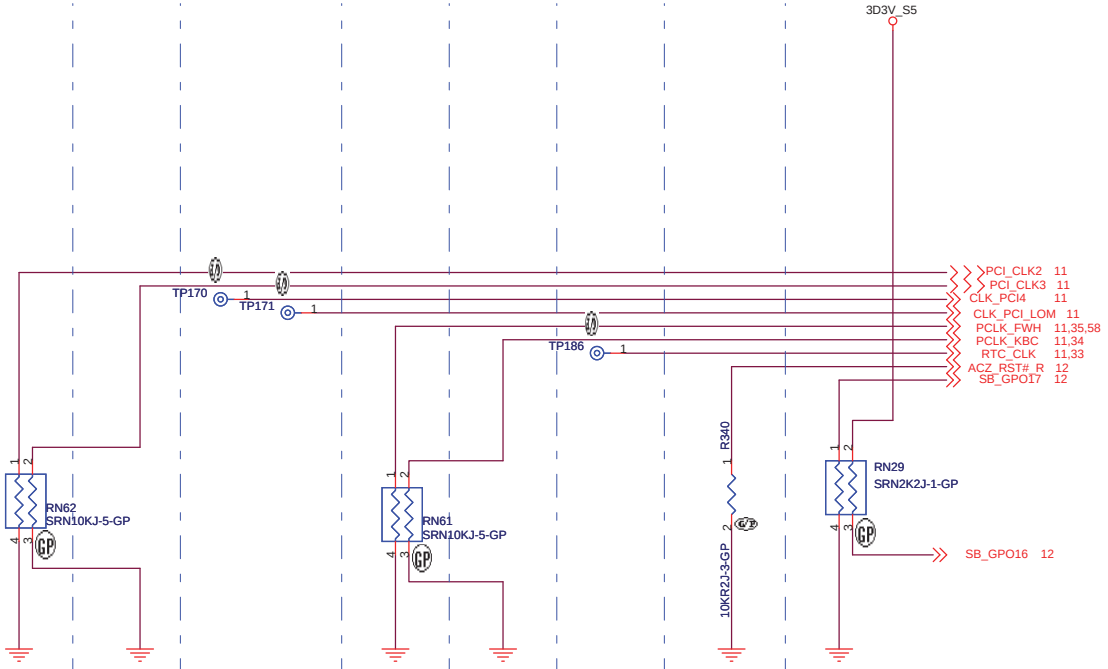
Title
SB700 (4 of 5)
Size
Document Number
SJV50-TR
Rev
-1
Date: Monday, June 29, 2009
Sheet 14 of 59

Delete DY Parts

REQUIRED STRAPS

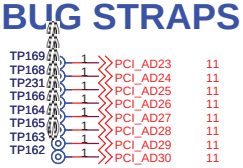
REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

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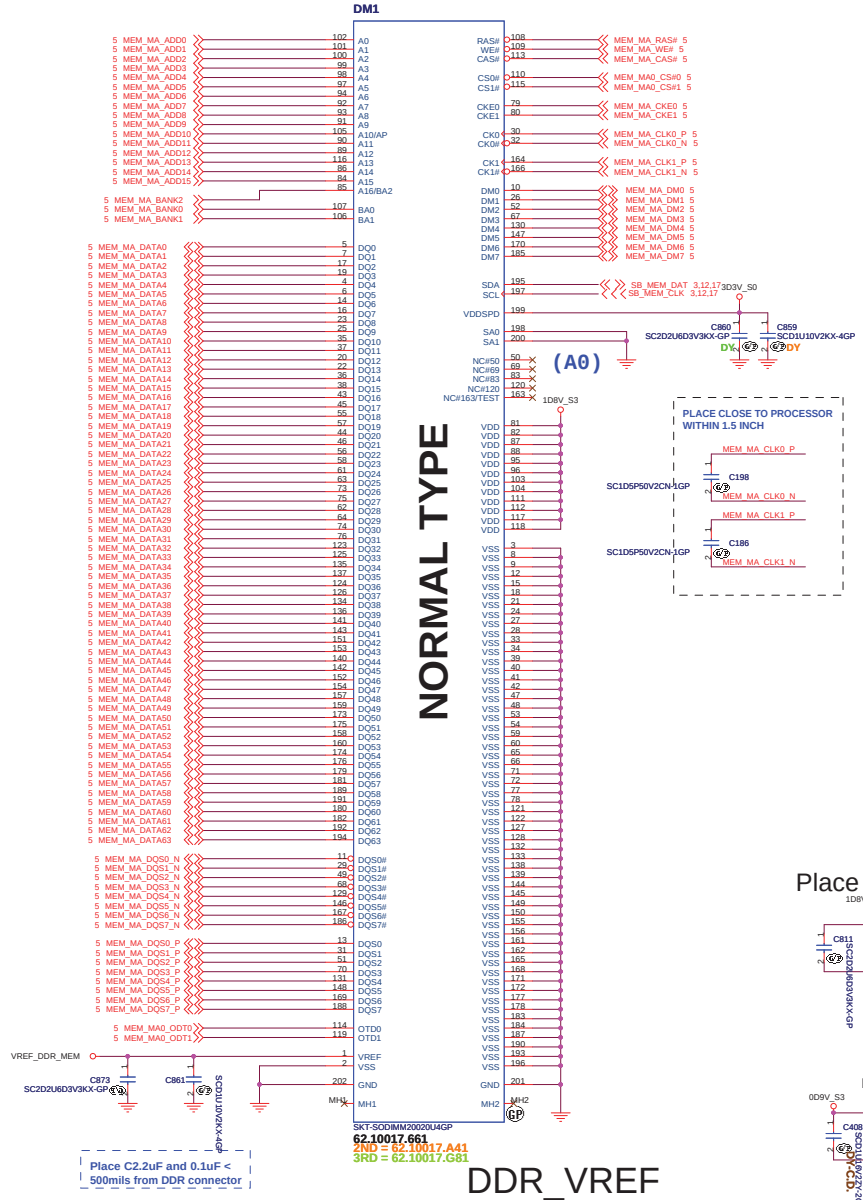
Title: SB700 (5 of 5)

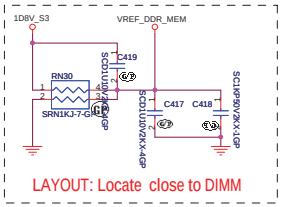
Size | Document Number: SJV50-TR | Rev: -1

Date: Monday, June 29, 2009 | Sheet 15 of 59

DDR2 SOCKET_1 (5.2mm)

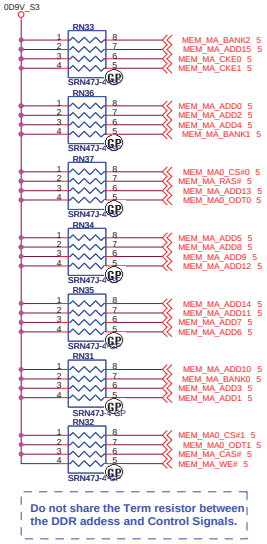


DDR_VREF



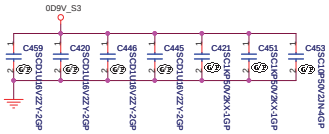
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

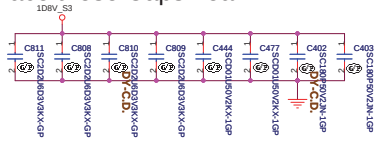


Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

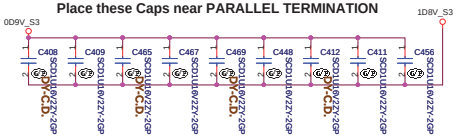


Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



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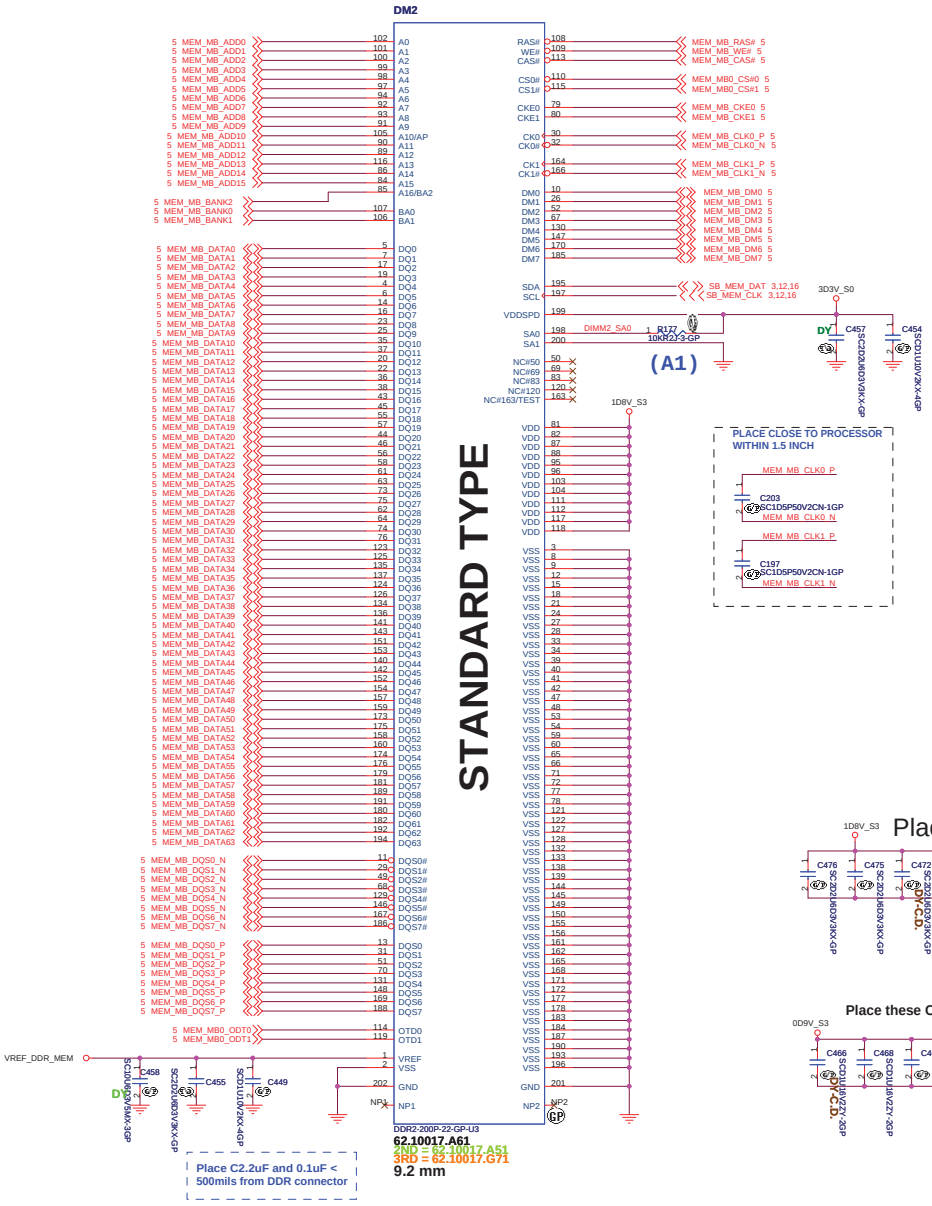
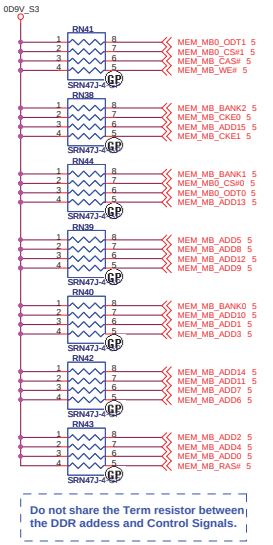
Title	DDR2 Socket_1	
Size	Document Number	Rev
	SJV50-TR	-1
Date: Monday, June 29, 2009	Sheet 16 of 59	

DDR2 SOCKET_2 (9.2mm)



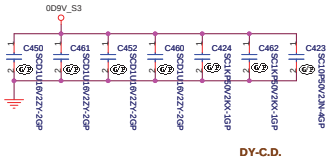
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

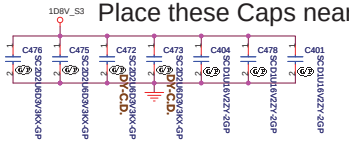


Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

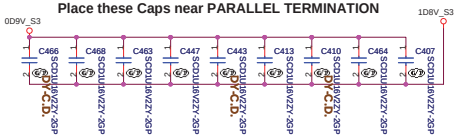


Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



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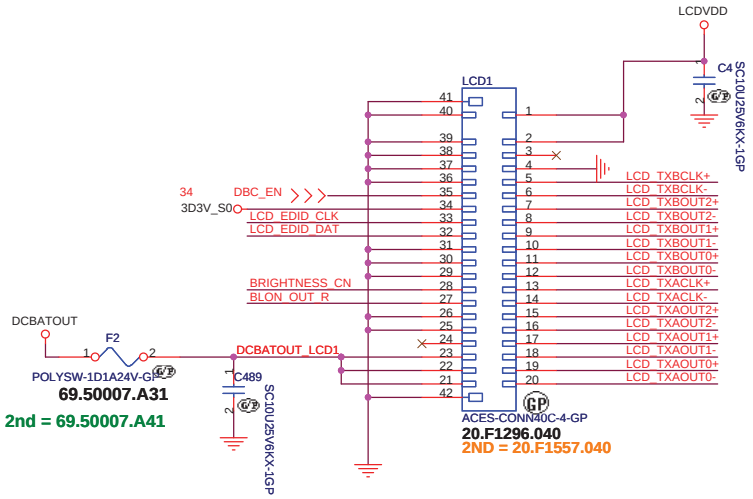
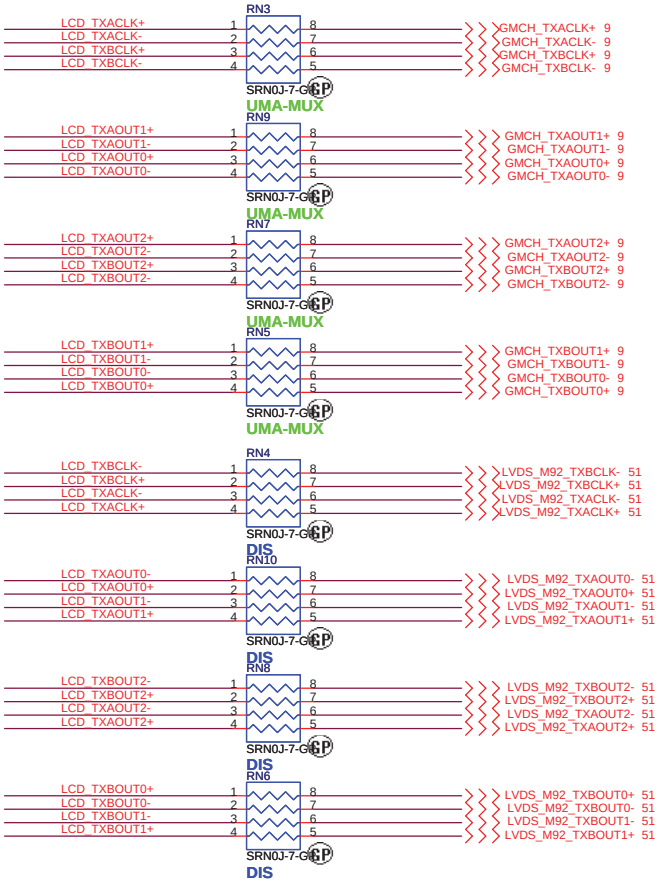
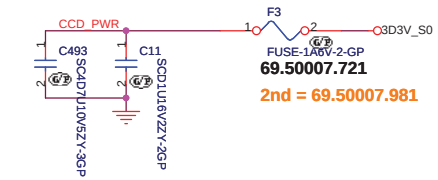
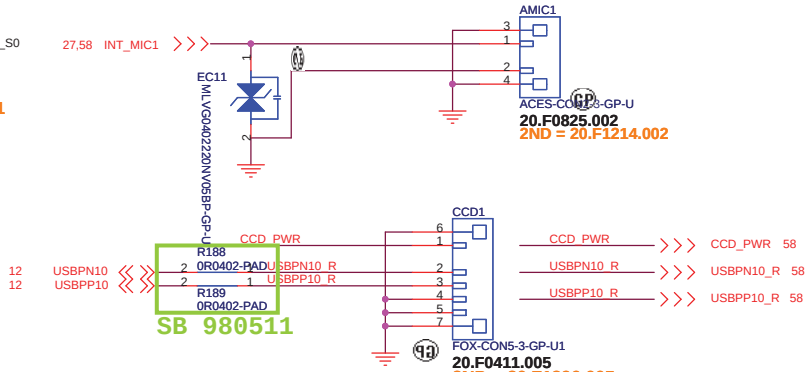
Title: *DDR2 Socket_2*		
Size	Document Number: SJV50-TR	Rev: -1
Date: Monday, June 29, 2009	Sheet 17 of 59	

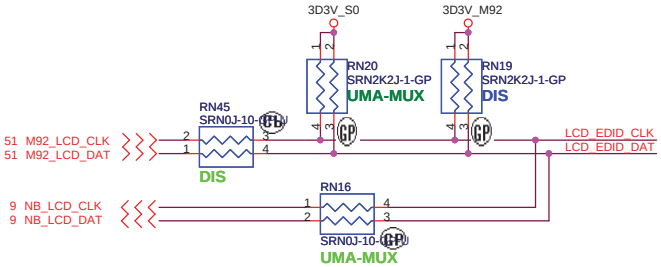
LCD/CCD CONN



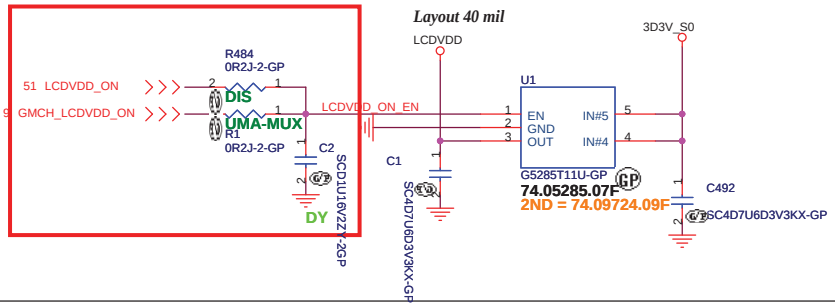


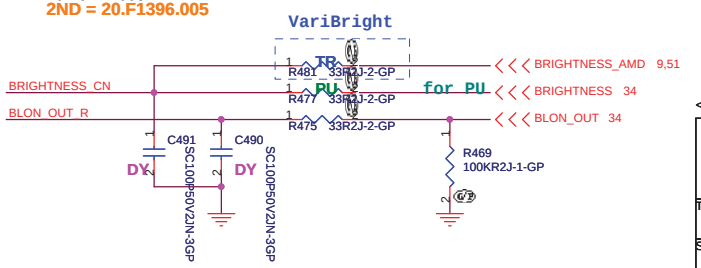






PX Select





<Core Design>

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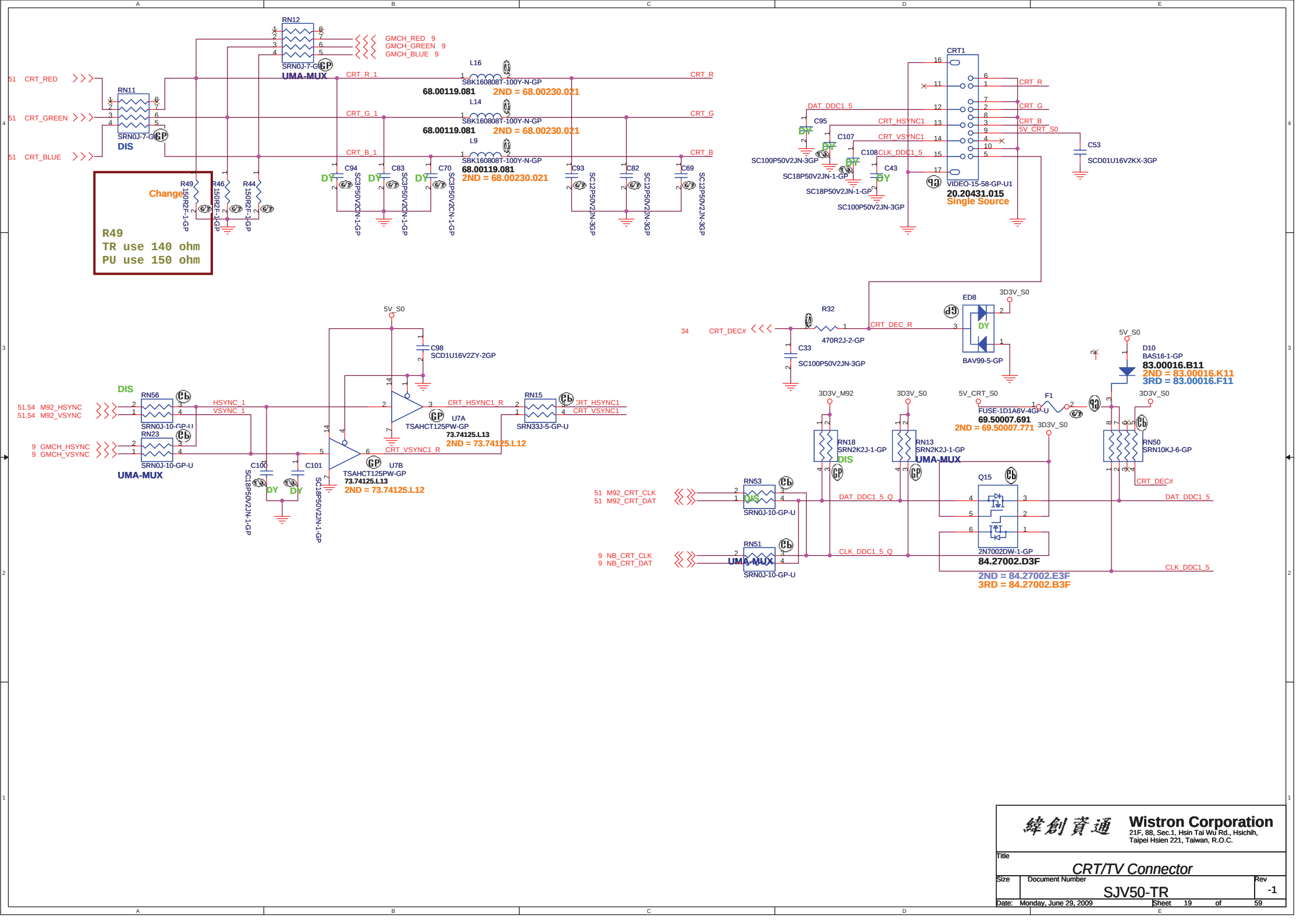
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED & LCD CONN / CCD

Size | Document Number: SJV50-TR | Rev: -1

Date: Monday, June 29, 2009 Sheet 18 of 59



緯創資通	**Wistron Corporation**
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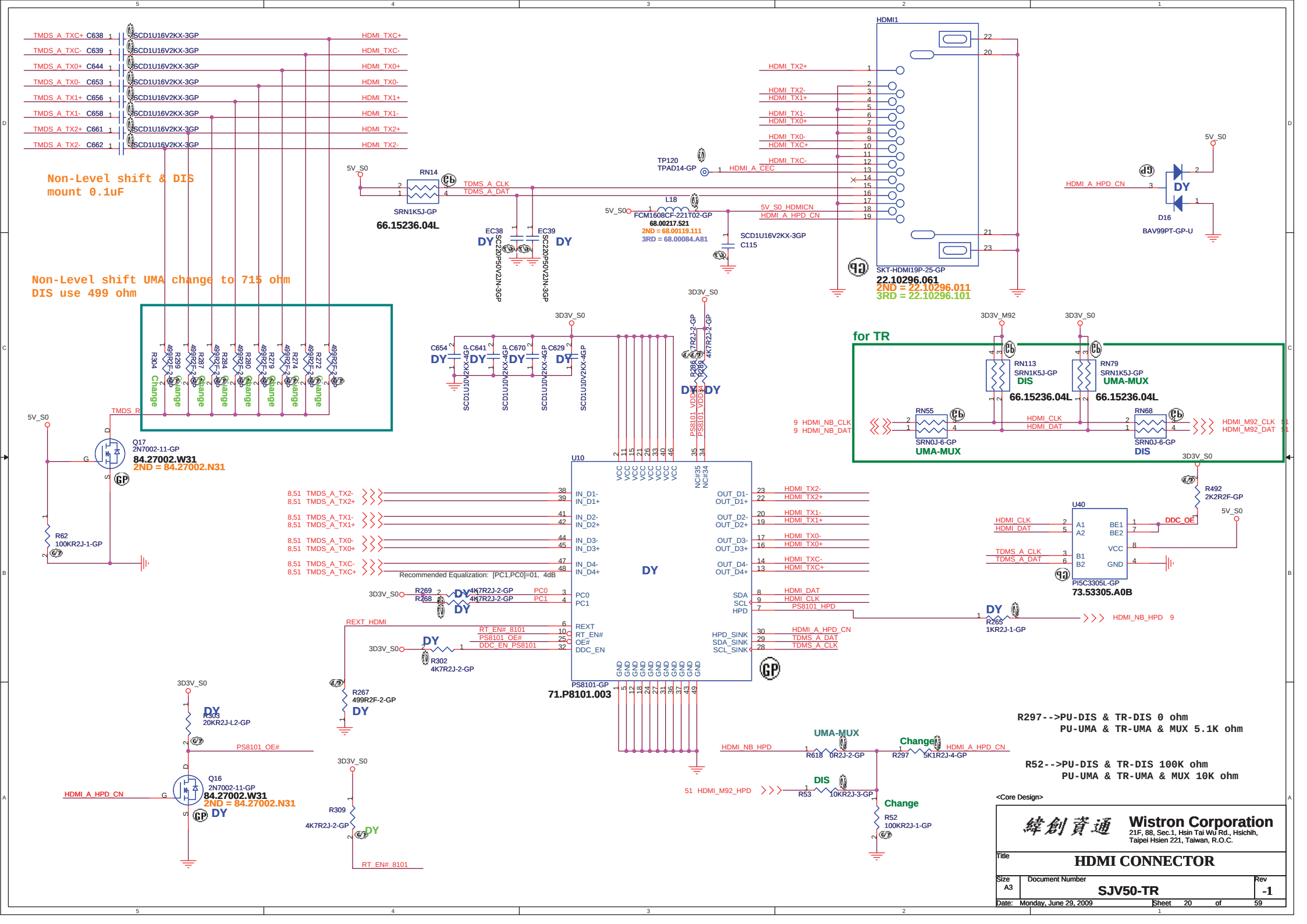
Title	*CRT/TV Connector*
Size	Document Number: SJV50-TR
Rev	-1
Date: Monday, June 29, 2009	Sheet 19 of 59


Non-Level shift & DIS mount 0.1uF
Non-Level shift UMA change to 715 ohm
DIS use 499 ohm
for TR
HDMI1
SKT-HDMI19P-25-GP
22.10296.061
2ND = 22.10296.011
3RD = 22.10296.101
RN14
SRN1K5J-GP
66.15236.04L
TP120
TPAD14-GP
L18
FCM1608CF-221T02-GP
68.00217.521
2ND = 68.00119.111
3RD = 68.00084.A81
SCD1U16V2KX-3GP
C115
EC38
EC39
SC220P50V2JN-3GP
D16
BAV99PT-GP-U
RN113
RN79
UMA-MUX
RN55
RN68
SRN0J-6-GP
U10
PS8101-GP
71.P8101.003
U40
PI5C3305L-GP
73.53305.A0B
Q17
2N7002-11-GP
84.27002.W31
2ND = 84.27002.N31
Q16
R62
100KR2J-1-GP
R492
2K2R2F-GP
R265
1KR2J-1-GP
R267
499R2F-2-GP
R302
4K7R2J-2-GP
R303
20KR2J-L2-GP
R309
4K7R2J-2-GP
R618
0R2J-2-GP
R297
5K1R2J-4-GP
R53
10KR2J-3-GP
R52
100KR2J-1-GP
R297-->PU-DIS & TR-DIS 0 ohm
PU-UMA & TR-UMA & MUX 5.1K ohm
R52-->PU-DIS & TR-DIS 100K ohm
PU-UMA & TR-UMA & MUX 10K ohm
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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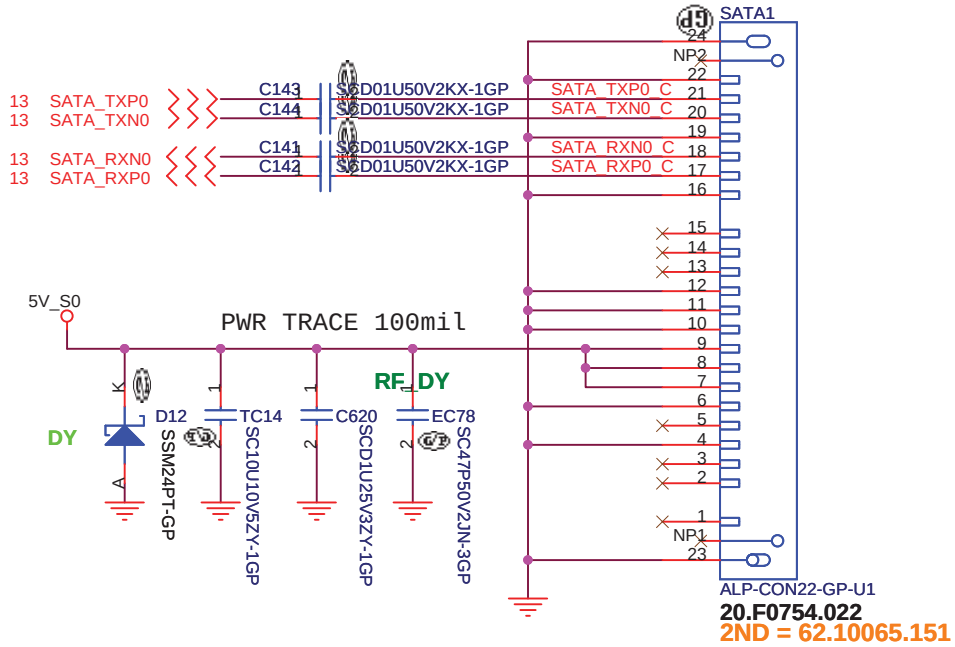
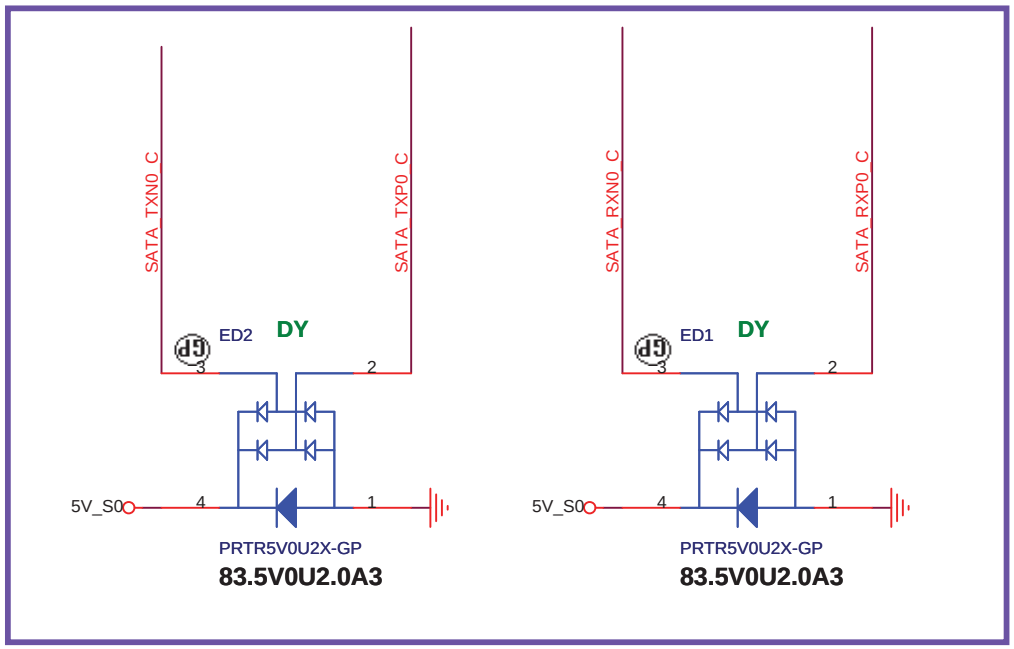
Title
HDMI CONNECTOR
Size A3
Document Number
SJV50-TR
Rev -1
Date: Monday, June 29, 2009
Sheet 20 of 59

SATA HDD Connector





SA_20081112

<Core Design>

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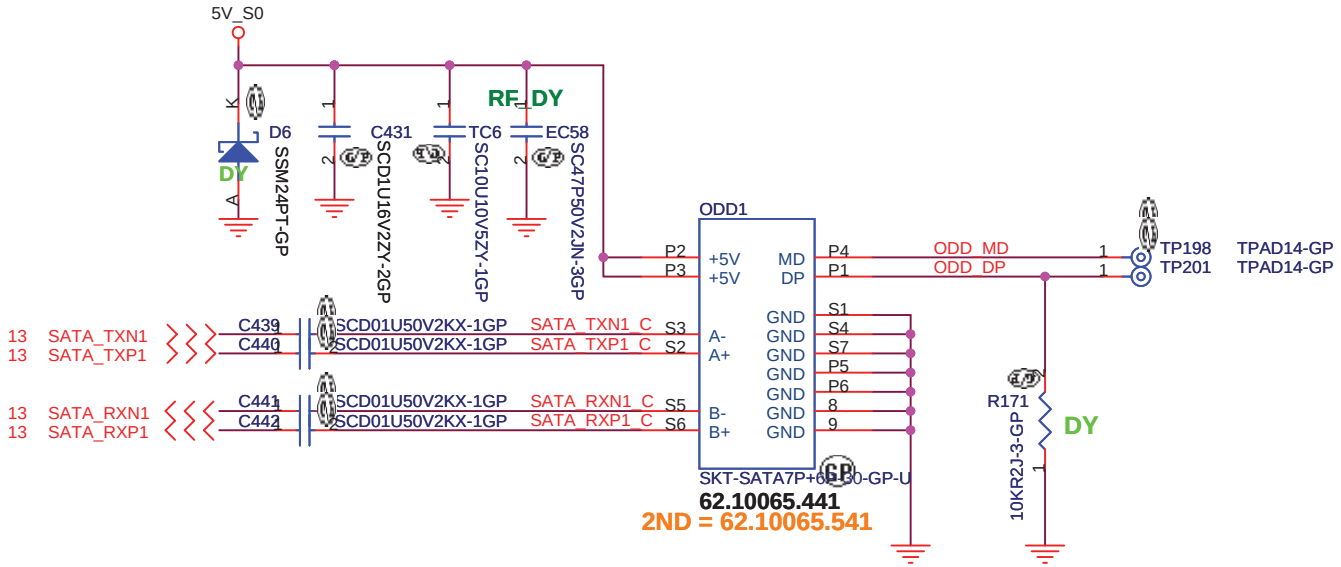
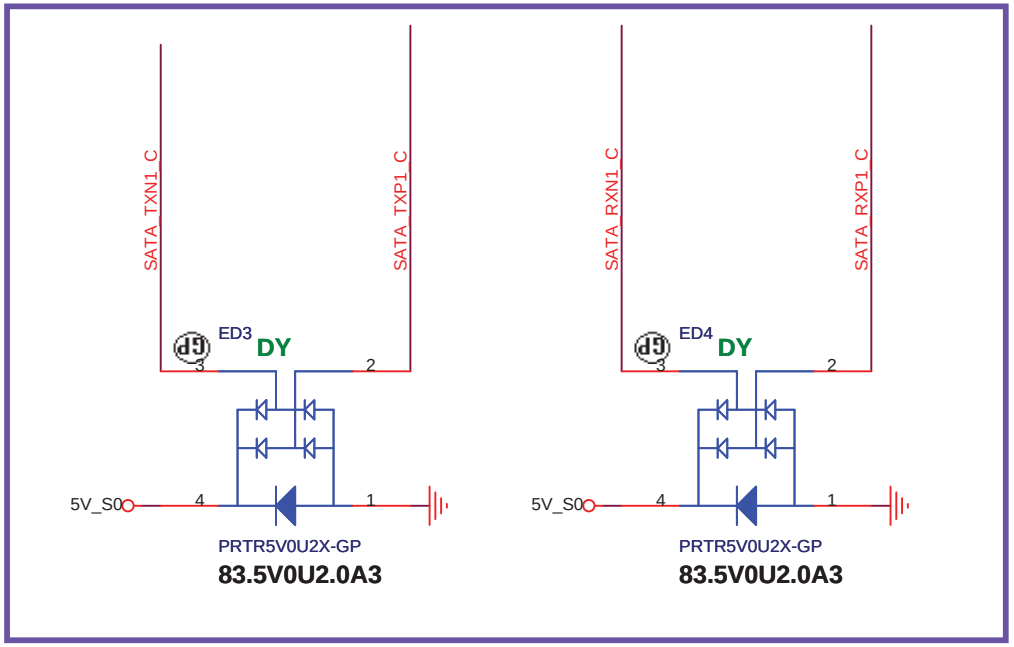
Title	***HDD***	
Size	Document Number **SJV50-TR**	Rev -1
Date: Monday, June 29, 2009	Sheet 21 of 59	

SATA ODD Connector





SA_20081112

<Core Design>

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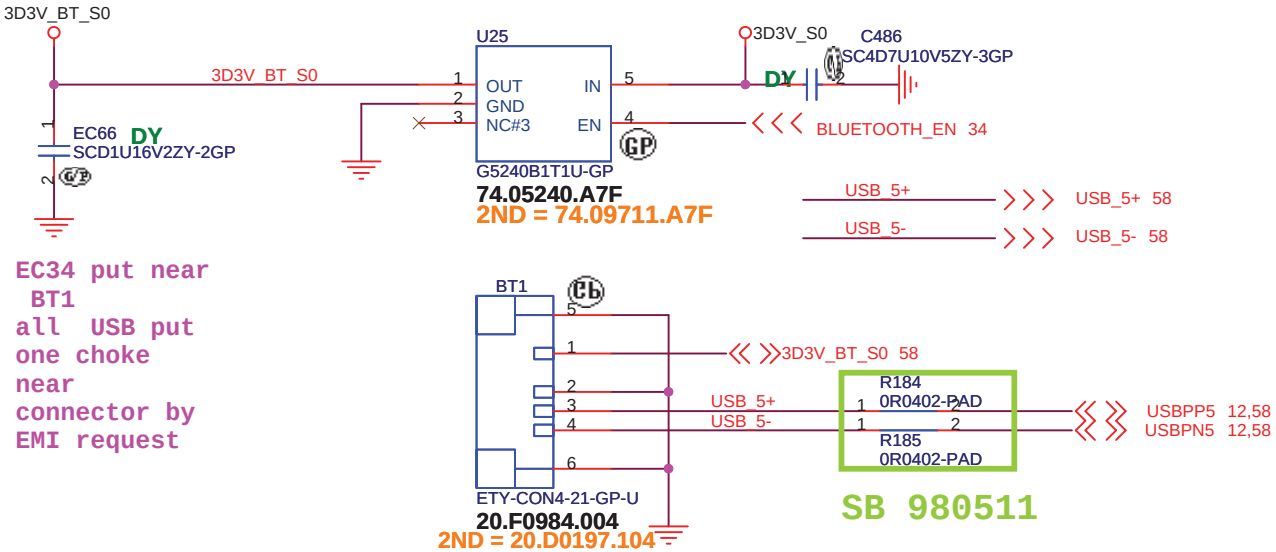
Taipei Hsien 221, Taiwan, R.O.C.

Title: ODD		
Size	Document Number: SJV50-TR	Rev: -1
Date: Monday, June 29, 2009	Sheet 22 of 59	

BLUETOOTH MODULE



<Core Design>

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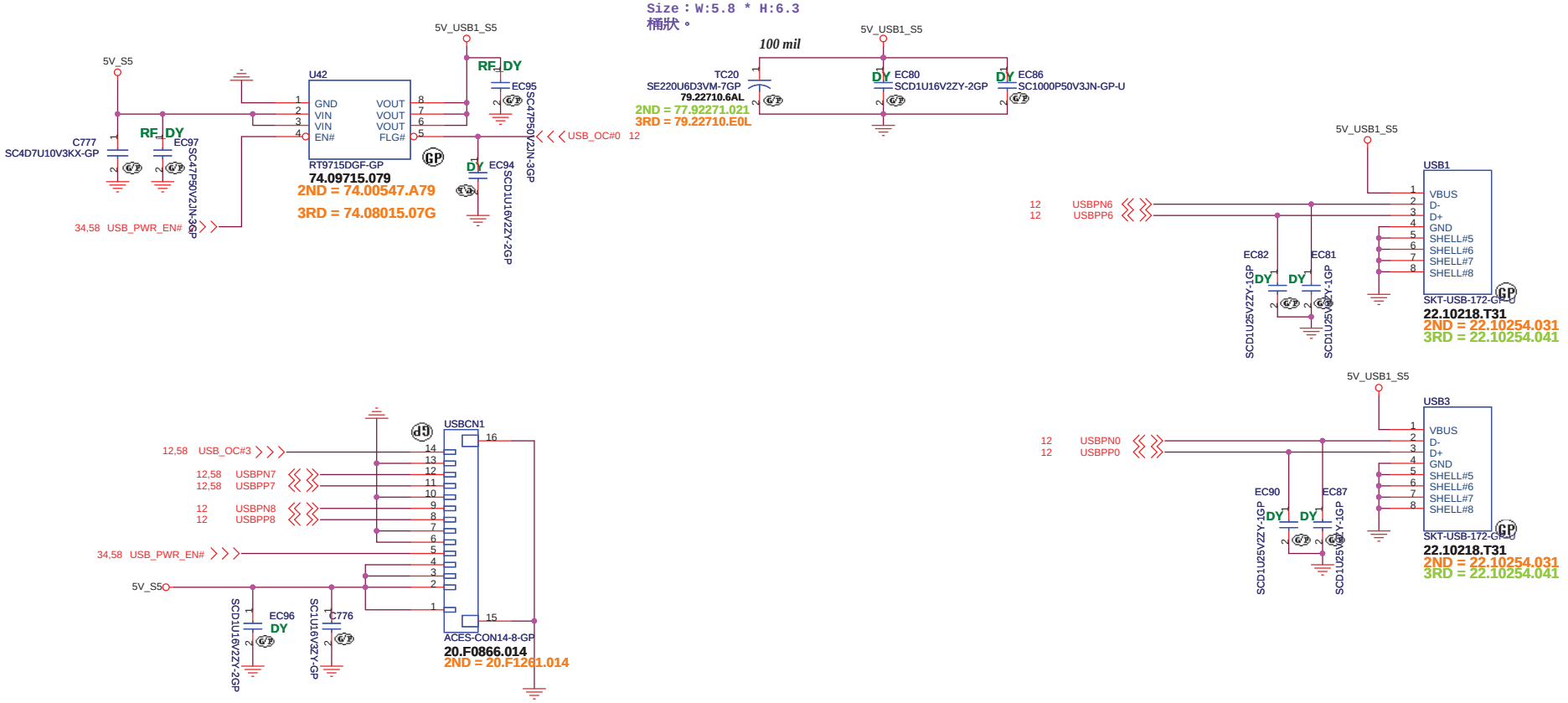
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BLUETOOTH***		
Size	Document Number: **SJV50-TR**	Rev: -1
Date: Monday, June 29, 2009	Sheet 23 of 59	



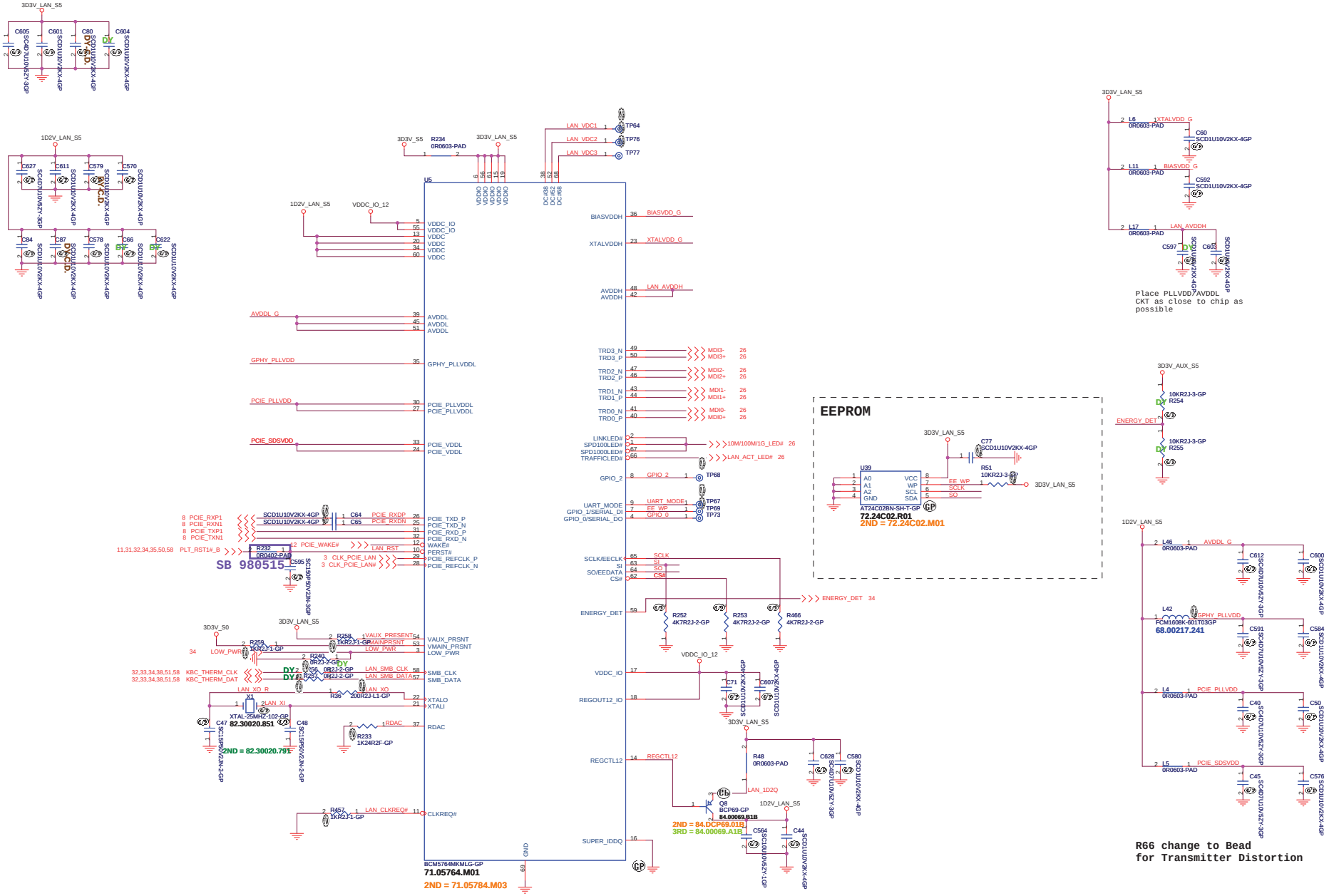
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Connector***

Size	Document Number	Rev
	SJV50-TR	-1

Date: Monday, June 29, 2009 Sheet 24 of 59



<Core Design>

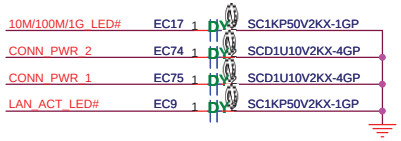
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

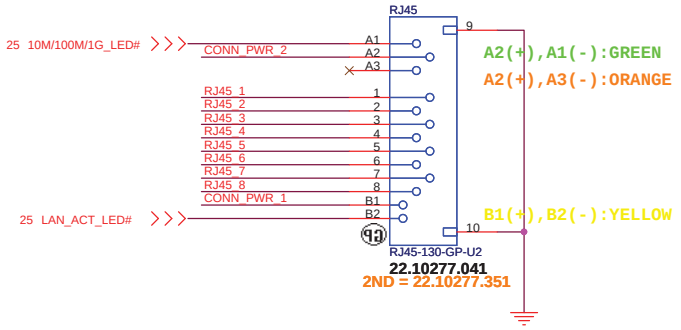
Title: BCM 5764

Size: A2 | Document Number: SJV50-TR | Rev: -1

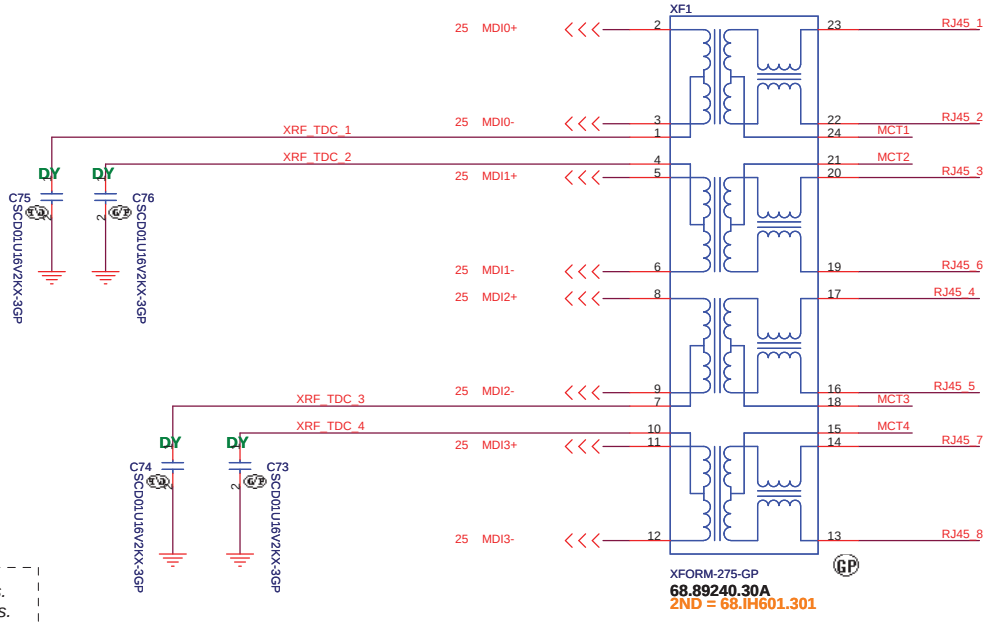
Date: Monday, June 29, 2009 | Sheet 25 of 59

LAN Connector

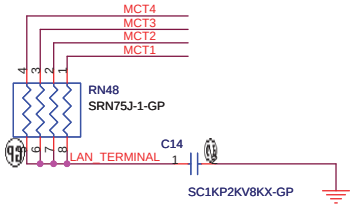




GIGA Lan Transformer



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

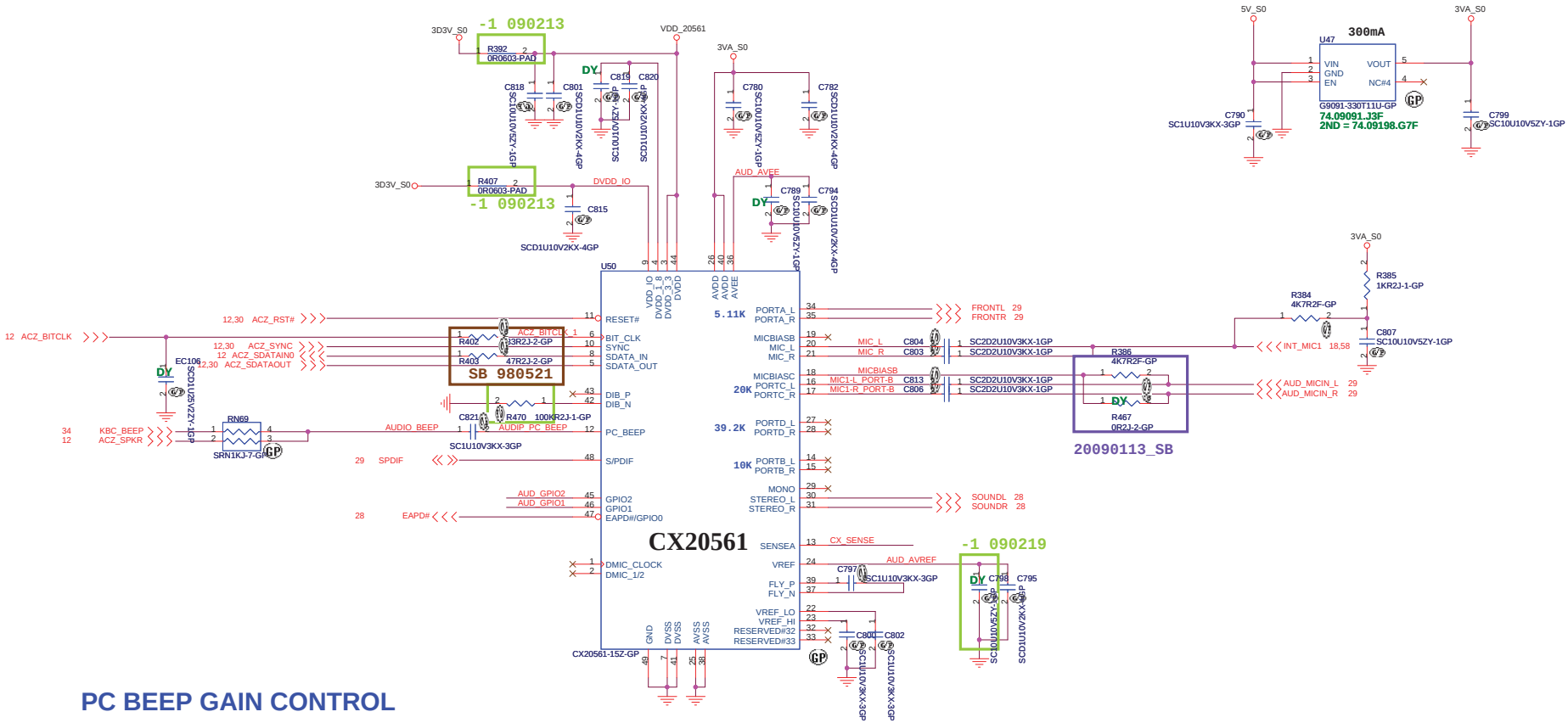
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

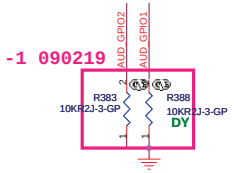
Title: **LAN Connector**

Size	Document Number	Rev
A3	SJV50-TR	-1

Date: Monday, June 29, 2009 Sheet 26 of 59



PC BEEP GAIN CONTROL



GAIN	10K GPIO RESISTORS	
	R388	R383
0dB	Populate	Populate
-6dB	Omit	Omit
-12dB	Populate	Omit
-18dB	Omit	Populate

Default gain is -6dB without populating the 10K-ohms pull-down resistors going to GPIO1 and GPIO2.

<Core Design>

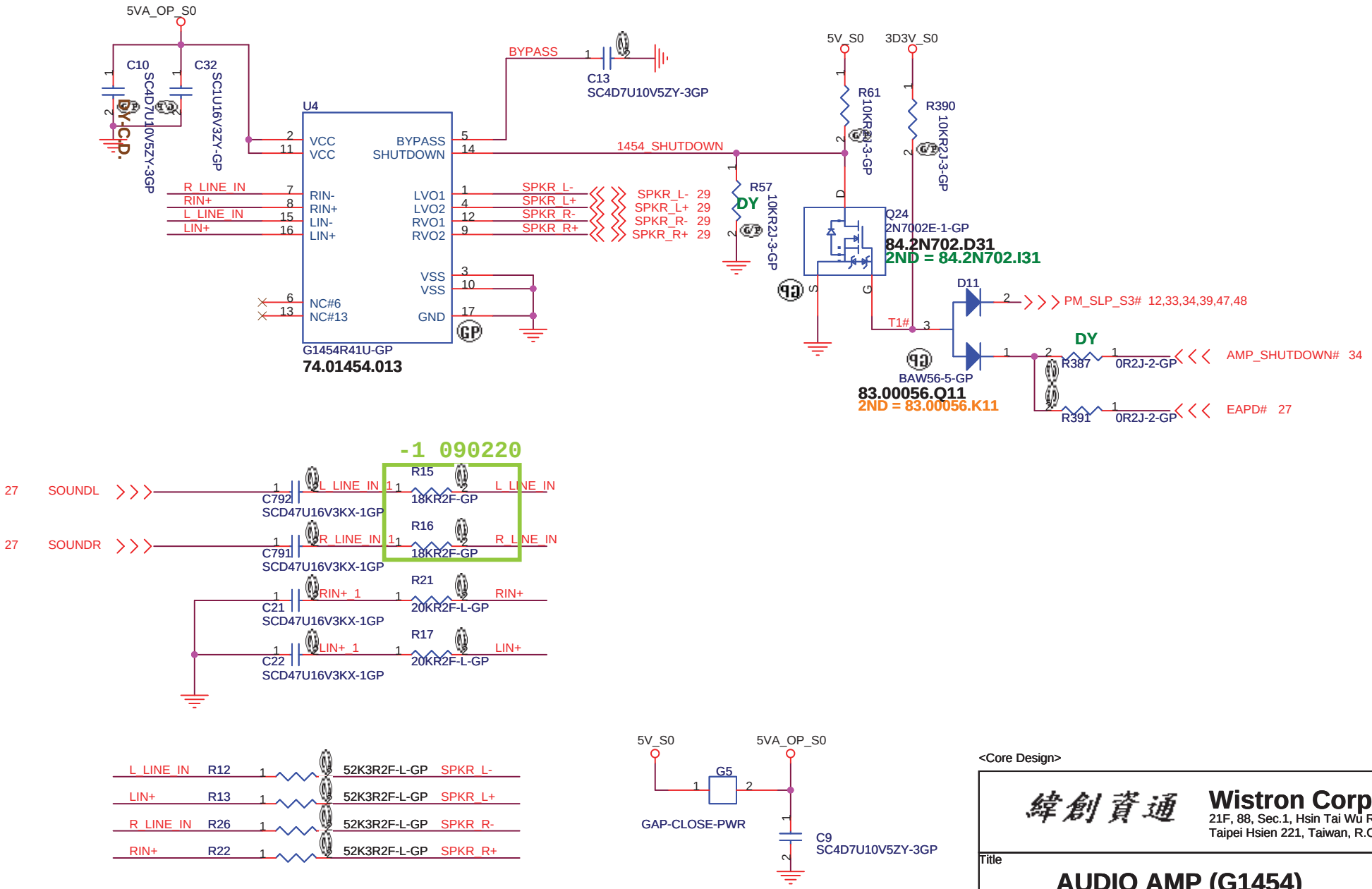
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AZALIA CODEC - CX20561

Size	Document Number	Rev
	SJV50-TR	-1

Date: Monday, June 29, 2009 Sheet 27 of 59

AUDIO OP AMPLIFIER



<Core Design>

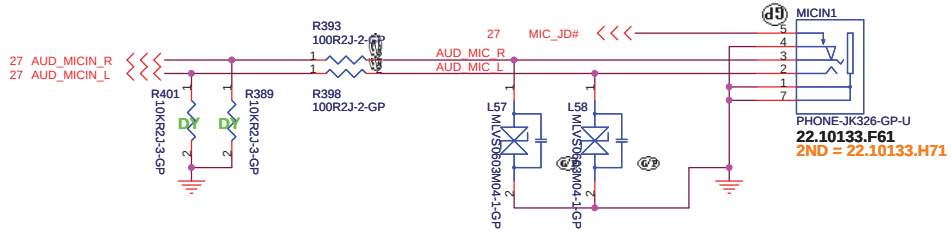
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO AMP (G1454)**

Size	Document Number	Rev
	SJV50-TR	-1

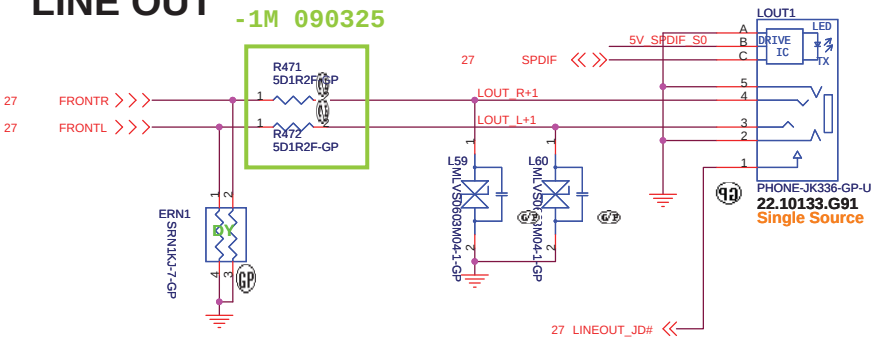
Date: Monday, June 29, 2009 Sheet 28 of 59

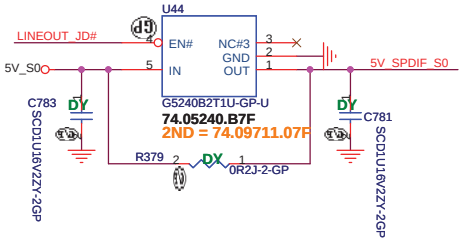
MIC IN



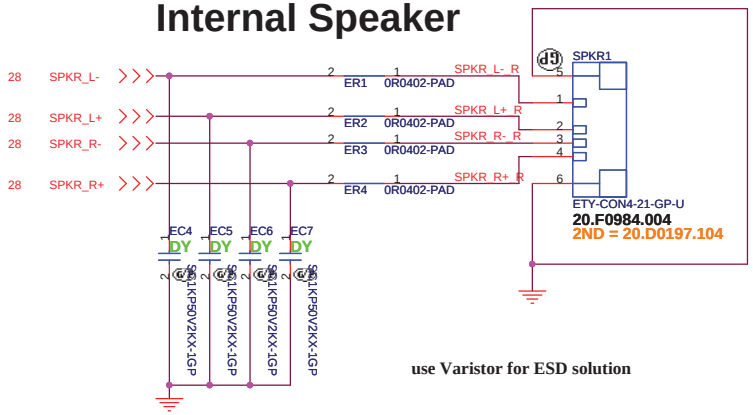
LINE OUT

-1M 090325





Internal Speaker



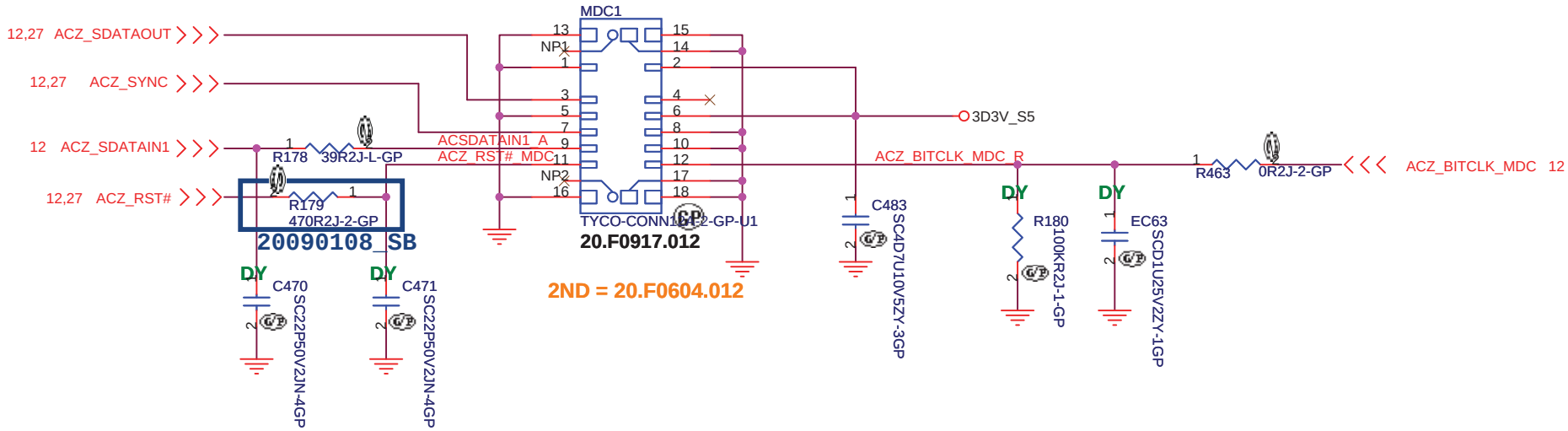
use Varistor for ESD solution

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Audio Jack	
Size	Document Number SJV50-TR	Rev -1
Date: Monday, June 29, 2009	Sheet 29 of 59	

MDC 1.5 CONN



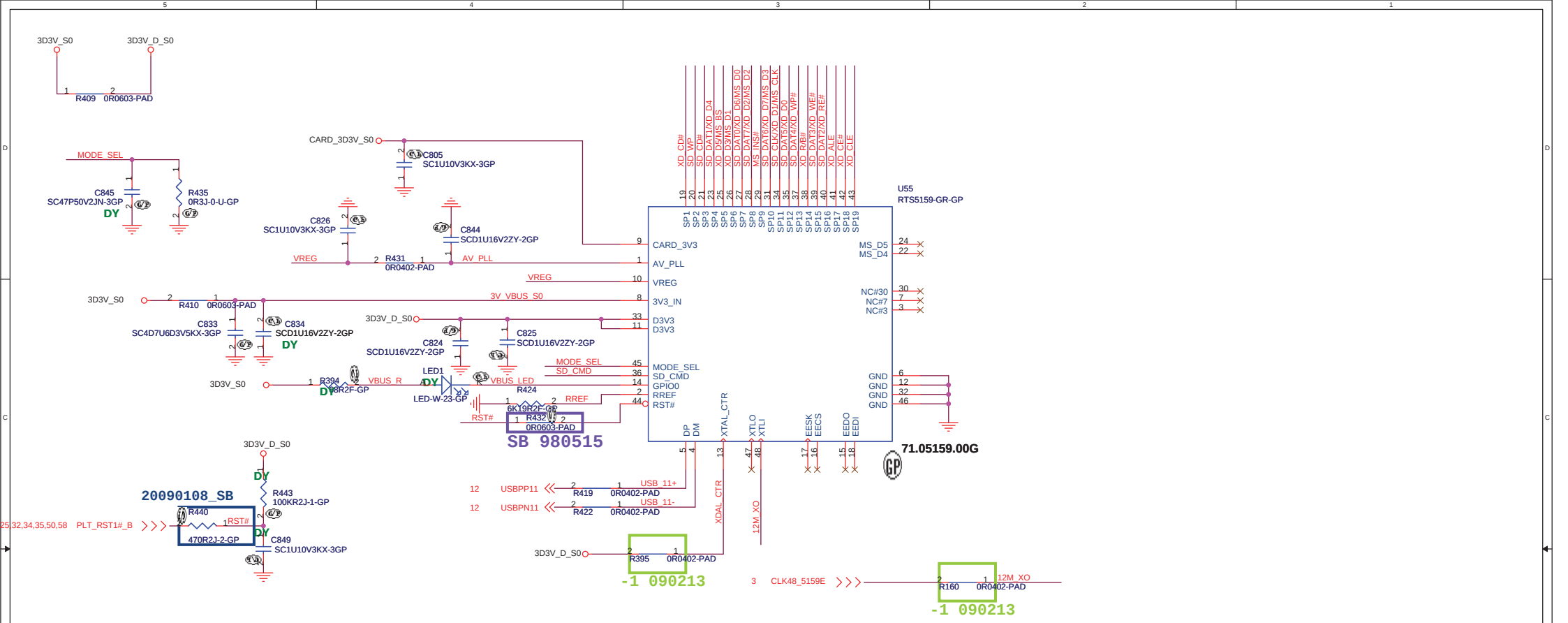
<Core Design>

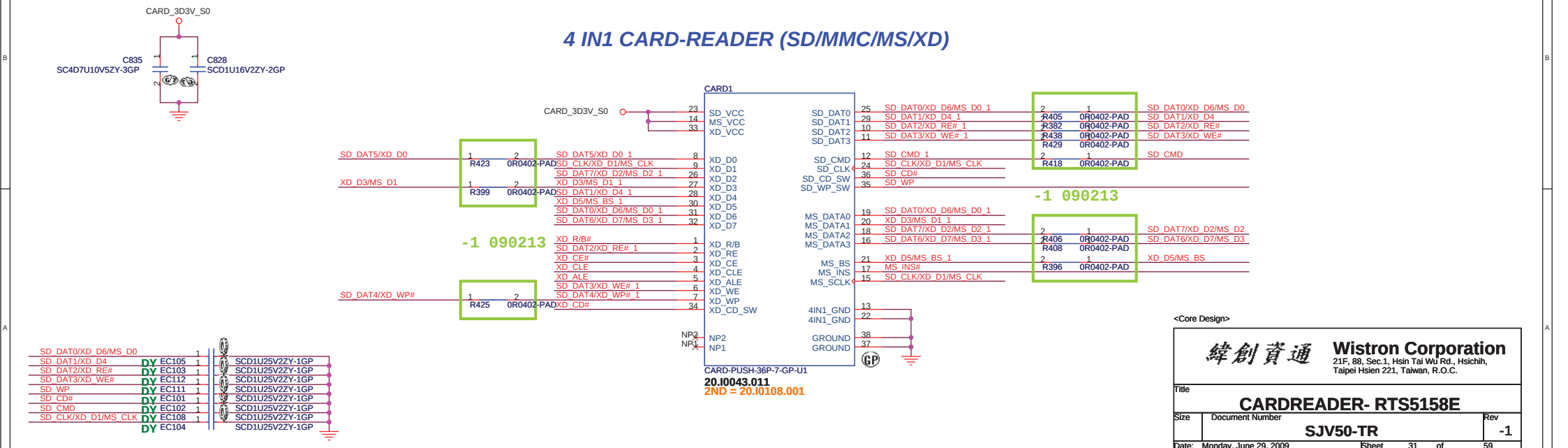
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Connector***

Size	Document Number	Rev
	SJV50-TR	-1

Date: Monday, June 29, 2009 Sheet 30 of 59





<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

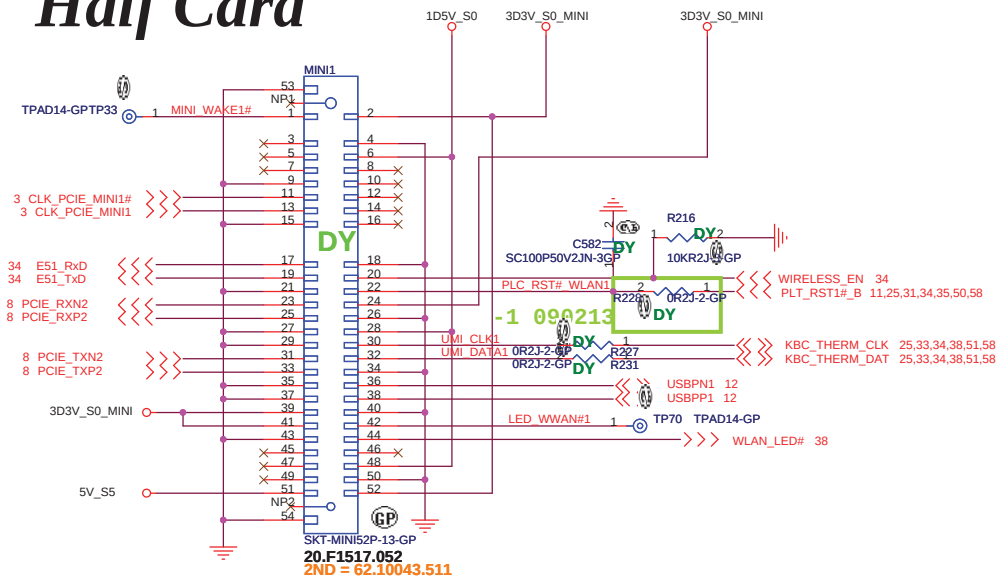
Title: **CARDREADER- RTS5158E**

Size	Document Number	Rev
	SJV50-TR	-1

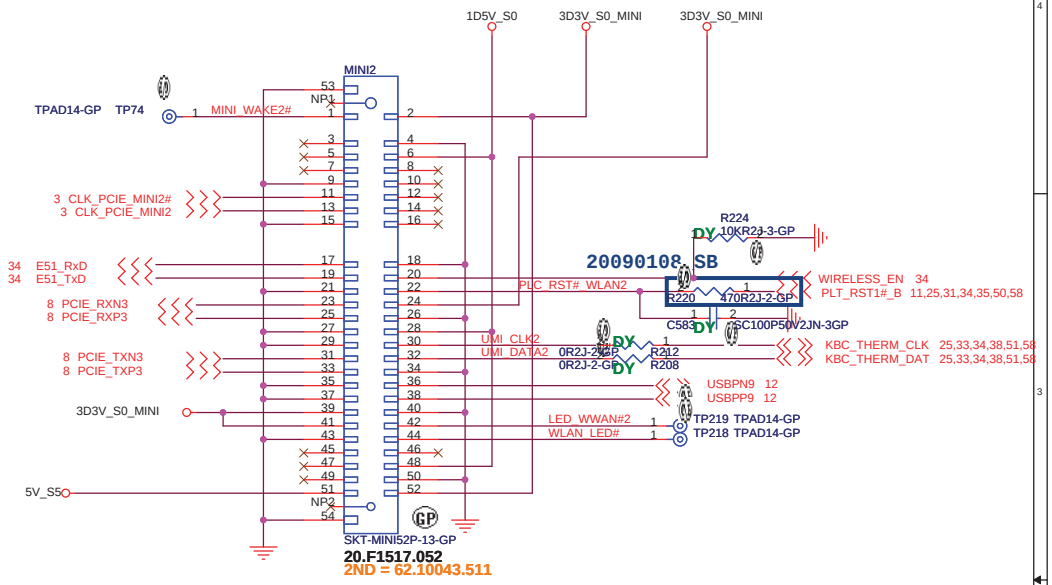
Date: Monday, June 29, 2009 Sheet 31 of 59

Mini Card Connector

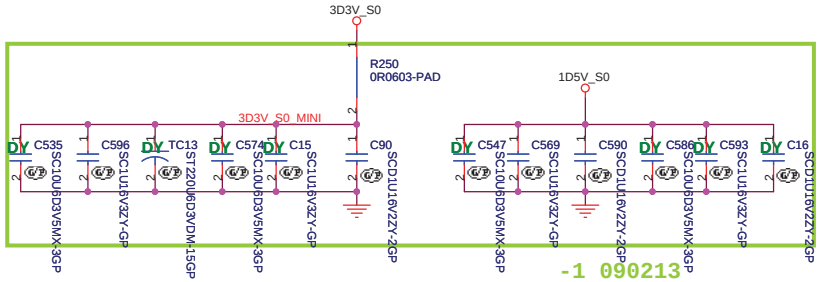
Half Card



Symbol use 62.10043.461

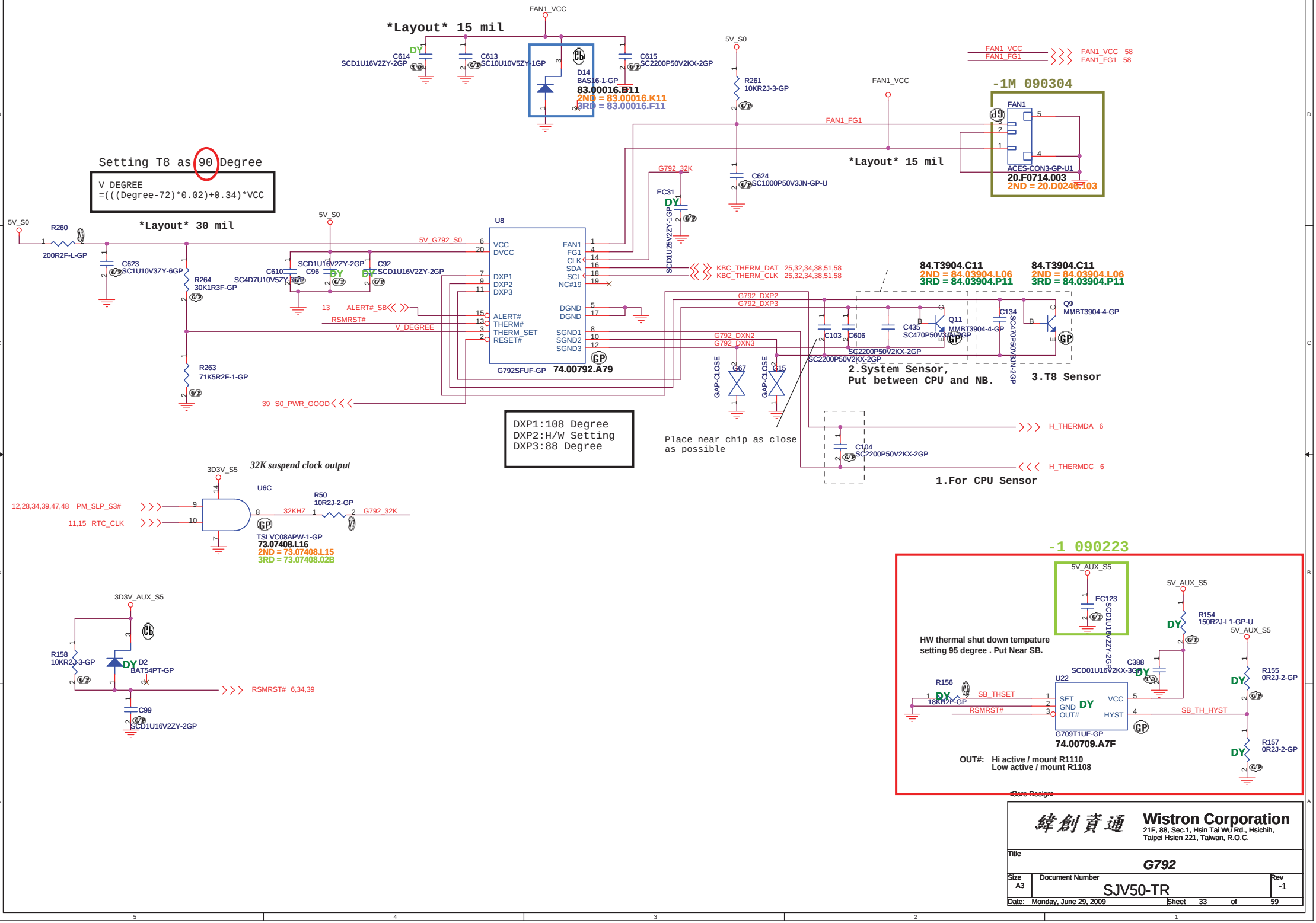


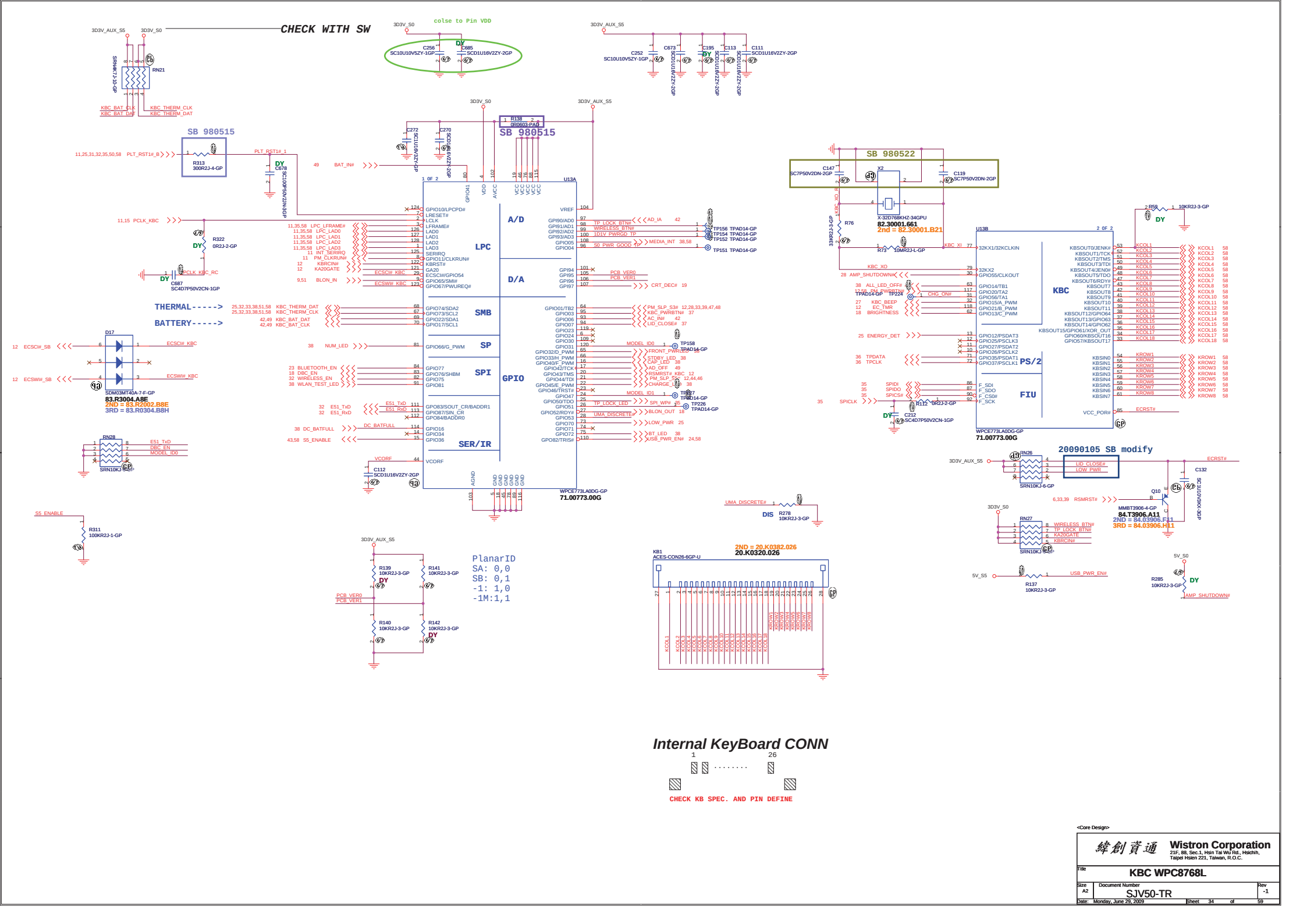
Symbol use 62.10043.461



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***MINI CARD***
Size / Document Number	**SJV50-TR**
Rev	-1
Date: Monday, June 29, 2009	Sheet 32 of 59


Layout 15 mil
FAN1_VCC
C614 SCD1U16V2ZY-2GP
C613 SC10U10V5ZY-1GP
C615 SC2200P50V2KX-2GP
D14 BAS16-1-GP
83.00016.B11
2ND = 83.00016.K11
3RD = 83.00016.F11
5V_S0
R261 10KR2J-3-GP
FAN1_VCC 58
FAN1_FG1 58
-1M 090304
FAN1
ACES-CON3-GP-U1
20.F0714.003
2ND = 20.D0246.003
FAN1_FG1
Layout 15 mil
C624 SC1000P50V3JN-GP-U
G792_32K
EC31 SCD1U25V2ZY-1GP
Setting T8 as 90 Degree
V_DEGREE
=(((Degree-72)*0.02)+0.34)*VCC
Layout 30 mil
5V_S0
R260 200R2F-L-GP
C623 SC1U10V3ZY-6GP
R264 30K1R3F-GP
R263 71K5R2F-1-GP
C610 SCD1U16V2ZY-2GP
C96 SC4D7U10V5ZY-1GP
C92 SCD1U16V2ZY-2GP
5V_G792_S0
U8
VCC
DVCC
DXP1
DXP2
DXP3
ALERT#
THERM#
THERM_SET
RESET#
FAN1
FG1
CLK
SDA
SCL
NC#19
DGND
DGND
SGND1
SGND2
SGND3
G792SFUF-GP
74.00792.A79
13 ALERT#_SB
RSMRST#
V_DEGREE
39 S0_PWR_GOOD
KBC_THERM_DAT 25,32,34,38,51,58
KBC_THERM_CLK 25,32,34,38,51,58
84.T3904.C11
2ND = 84.03904.L06
3RD = 84.03904.P11
84.T3904.C11
2ND = 84.03904.L06
3RD = 84.03904.P11
G792_DXP2
G792_DXP3
G792_DXN2
G792_DXN3
C103 SC2200P50V2KX-2GP
C606 SC2200P50V2KX-2GP
C435 SC470P50V3JN-2GP
Q11 MMBT3904-4-GP
C134 SC470P50V3JN-2GP
Q9 MMBT3904-4-GP
GAP-CLOSE
G67
GAP-CLOSE
C15
2.System Sensor,
Put between CPU and NB.
3.T8 Sensor
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
Place near chip as close as possible
H_THERMDA 6
C104 SC2200P50V2KX-2GP
H_THERMDC 6
1.For CPU Sensor
3D3V_S5
32K suspend clock output
U6C
12,28,34,39,47,48 PM_SLP_S3#
11,15 RTC_CLK
R50 10R2J-2-GP
32KHZ
G792_32K
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
3D3V_AUX_S5
R158 10KR2J-3-GP
D2 BAT54PT-GP
RSMRST# 6,34,39
C99 SCD1U16V2ZY-2GP
-1 090223
5V_AUX_S5
EC123 SCD1U16V2ZY-2GP
HW thermal shut down tempature setting 95 degree . Put Near SB.
R156 18KR2F-GP
SB_THSET
RSMRST#
U22
SET
GND
OUT#
VCC
HYST
G709T1UF-GP
74.00709.A7F
C388 SCD01U16V2KX-3GP
R154 150R2J-L1-GP-U
R155 0R2J-2-GP
R157 0R2J-2-GP
SB_TH_HYST
OUT#: Hi active / mount R1110
Low active / mount R1108
Core Design
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
G792
Size A3
Document Number
SJV50-TR
Rev -1
Date: Monday, June 29, 2009
Sheet 33 of 59



<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

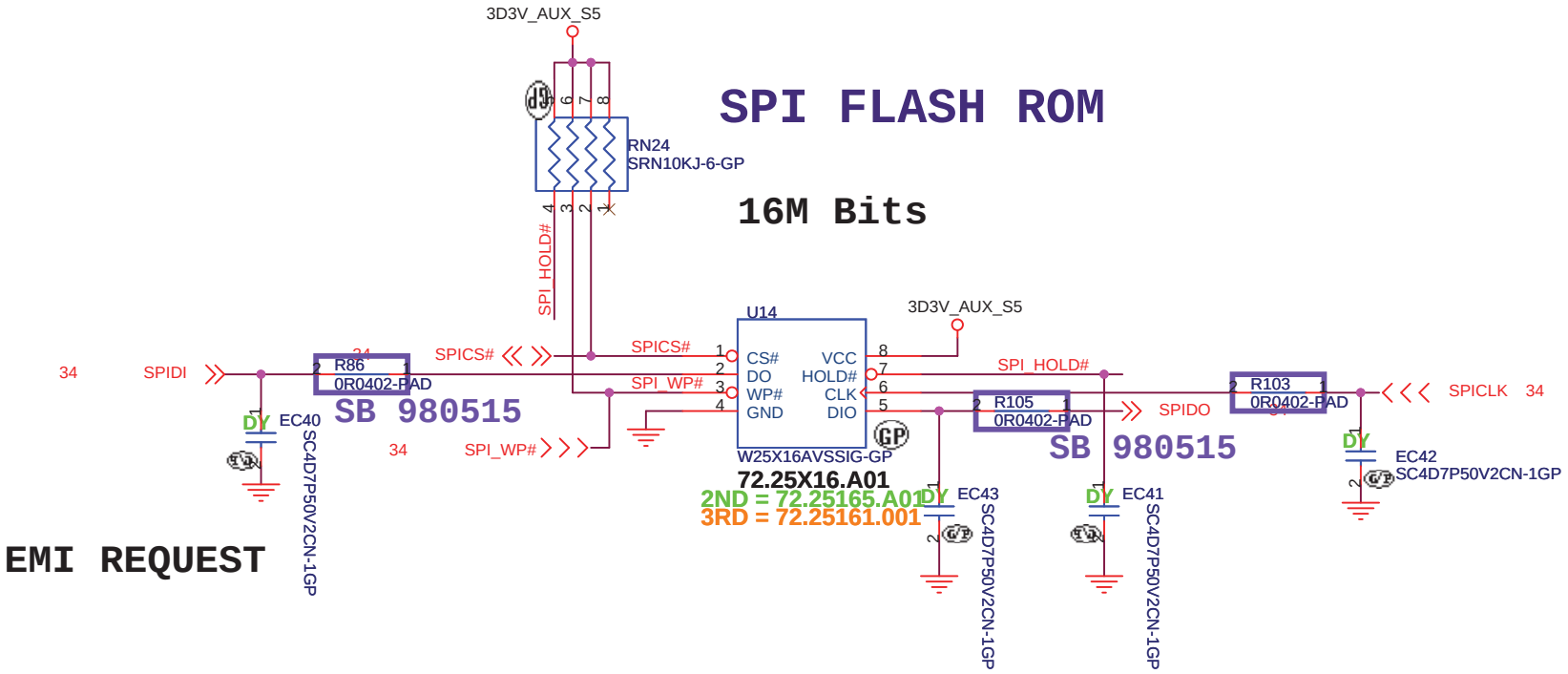
Title: KBC WPC8768L

Size	Document Number	Rev
A2	SJV50-TR	-1

Date: Monday, June 29, 2009 Sheet 34 of 59

SPI FLASH ROM

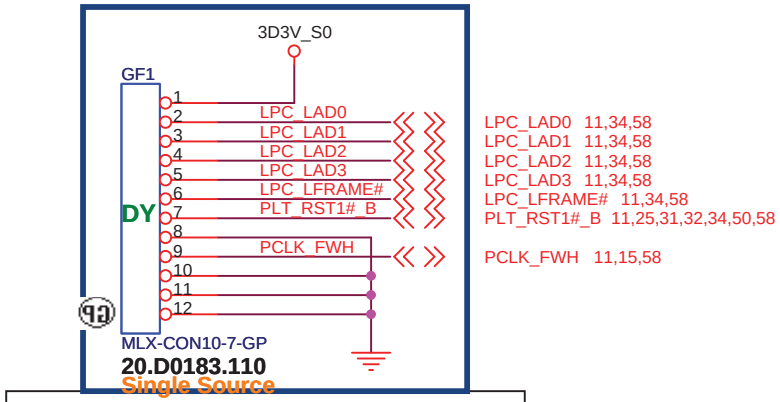
16M Bits



EMI REQUEST

Connector FOR DEBUG BOARD

20081219



LPC_LAD0 11,34,58
LPC_LAD1 11,34,58
LPC_LAD2 11,34,58
LPC_LAD3 11,34,58
LPC_LFRAME# 11,34,58
PLT_RST1#_B 11,25,31,32,34,50,58

PCLK_FWH 11,15,58

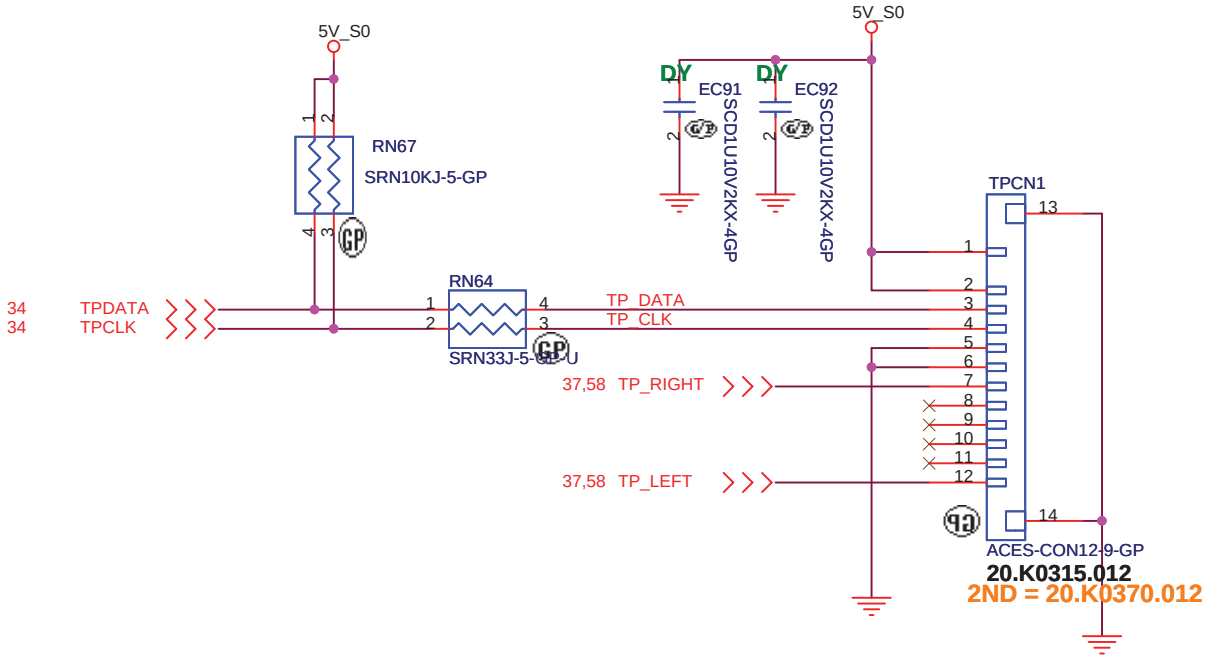
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

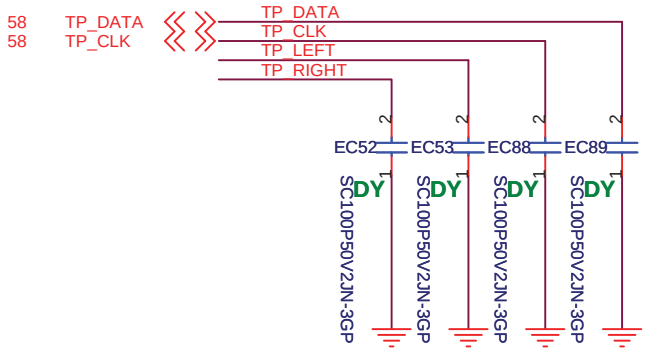
<Core Design>

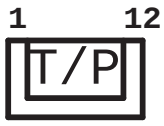
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
BIOS			
Size: A4	Document Number: SJV50-TR		Rev: -1
Date: Monday, June 29, 2009	Sheet 35 of 59		

TOUCH PAD





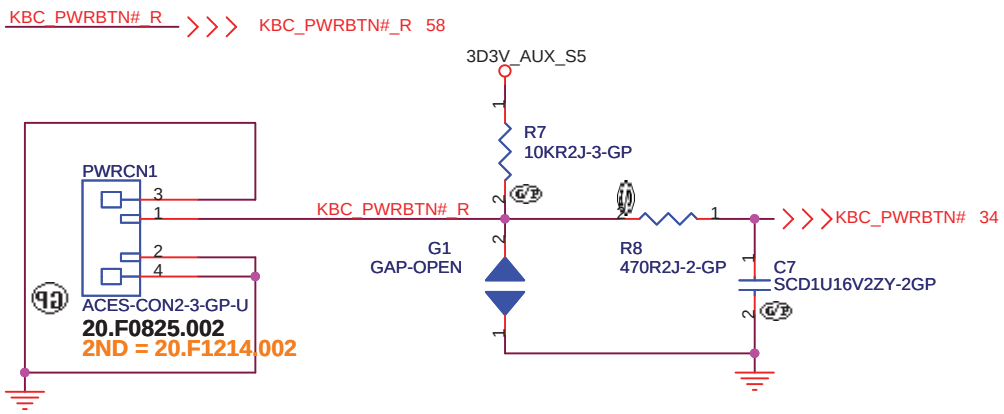


<Core Design>

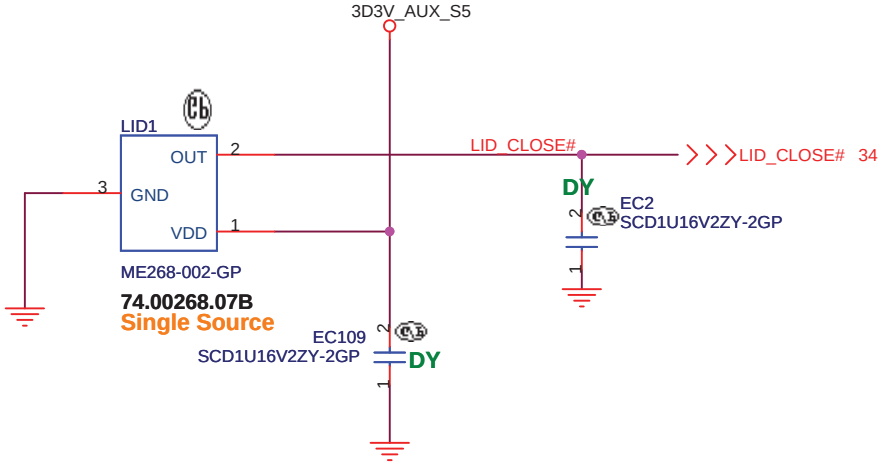
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *TouchPad*		
Size	Document Number: **SJV50-TR**	Rev: -1
Date: Monday, June 29, 2009	Sheet 36 of 59	

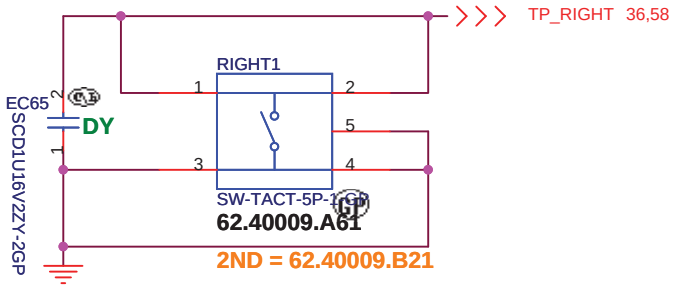
Power Button Board



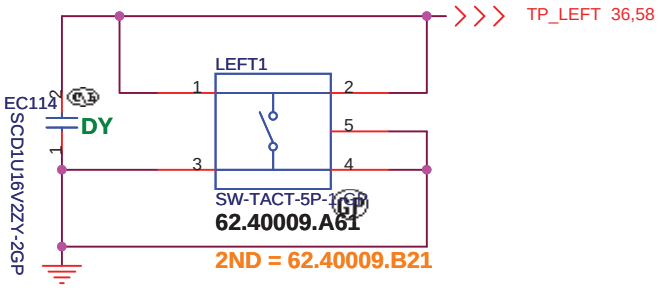
Cover Up Switch



RIGHT



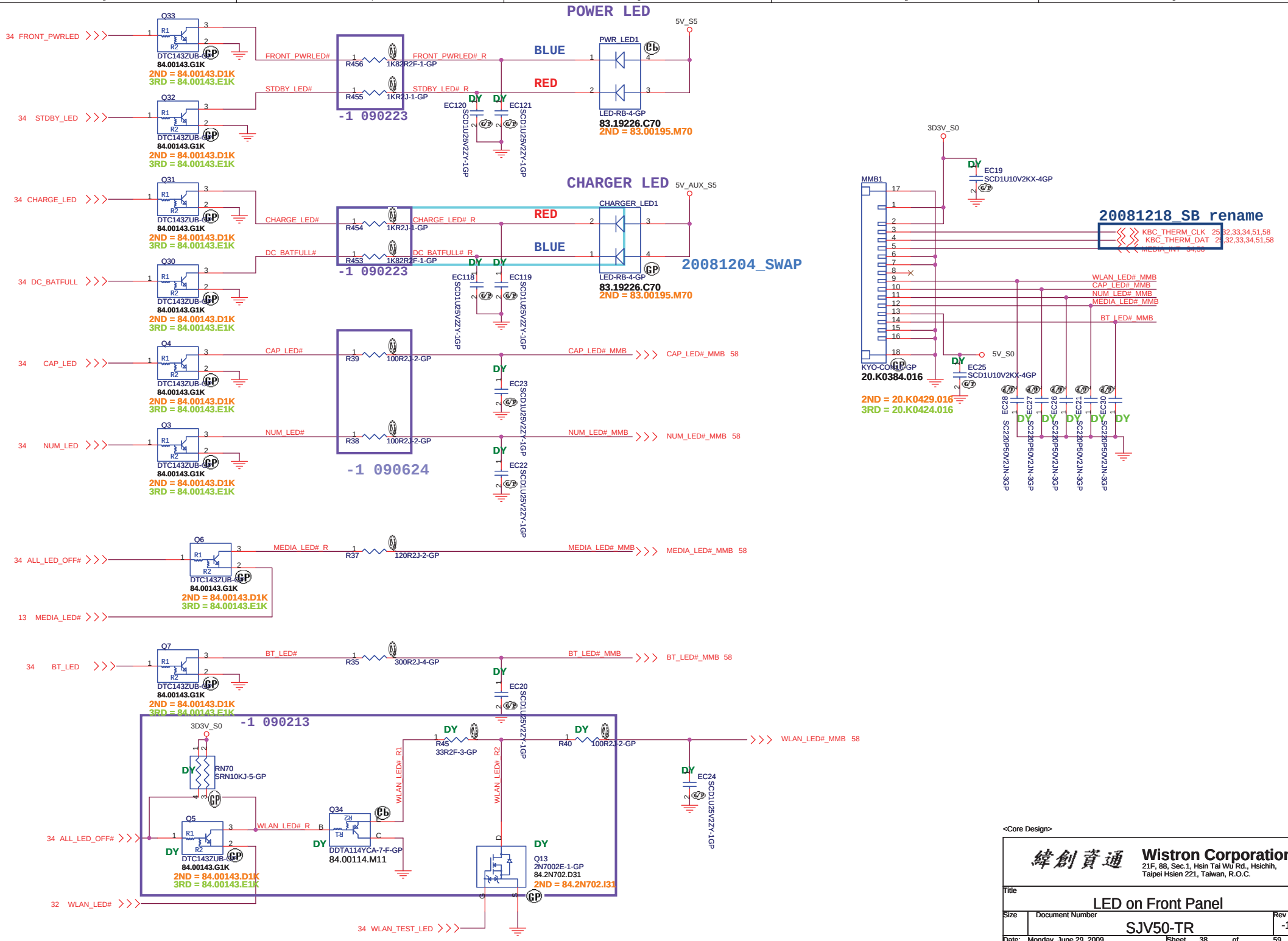
LEFT



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Switchs		
Size	Document Number: SJV50-TR	Rev: -1
Date: Monday, June 29, 2009	Sheet 37 of 59	



<Core Design>

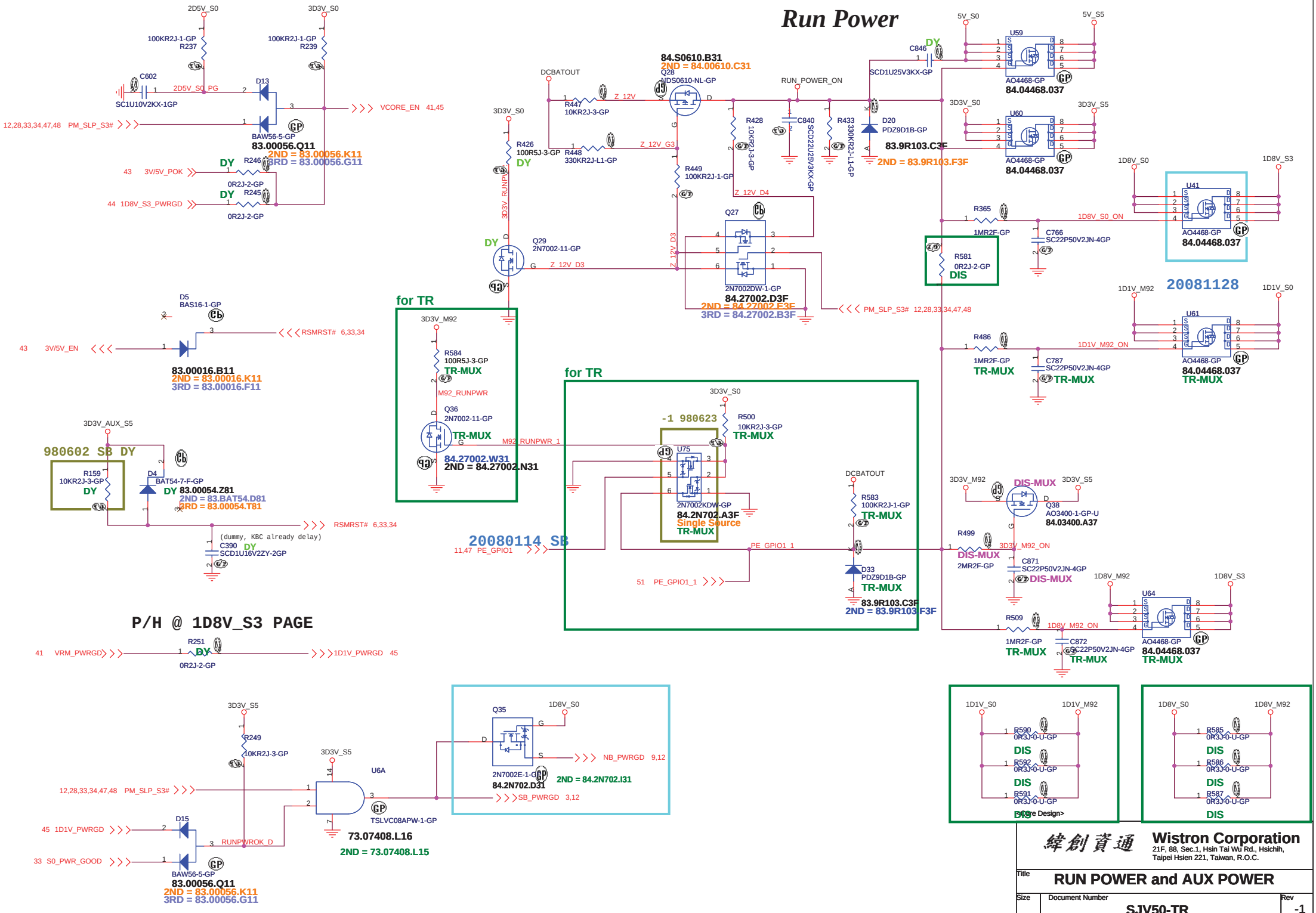
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED on Front Panel

Size | Document Number: SJV50-TR | Rev: -1

Date: Monday, June 29, 2009 | Sheet 38 of 59

Run Power



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUN POWER and AUX POWER**

Size	Document Number	Rev
	SJV50-TR	-1

Date: Monday, June 29, 2009 Sheet 39 of 59

CPU_CORE
ISL6264

VID0
VID1
VID2
VID3
VID4
VID5

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)

Output Signal
VROK()

MAX8760_VRM

Output Power
VCC_CORE_PWR(O)

VCC_CORE_S0(Imax=35A)

VCORE_EN

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

COREFB
COREFB#

Input Power
VCC(I)
VCC(I)
VCC(I)

DCBATOUT
5V_S0
3D3V_S0

TI TPS51125
3D3V/5V

Input Signal
51120_EN2 FOR 3.3V
51120_EN1 FOR 5.0V
VIN

Output Signal
PGOUT(OD / 5V)

Pull High (3D3V)

DCBATOUT_51120

Input Power
VIN
REG5V_IN(I / 5V)

DCBATOUT_51120

Output Power
5V(O)
3D3V(O)

5V_AUX_S5
3D3V_AUX_S5
5V_S5 (5.4A)
3D3V_S5 (4A)

1D5V_S0

3D3V_S0 → INPUT / OUT → 1D5V_S0

G957

1D2V_S5

3D3V_S5 → INPUT / OUT → 1D2V_S5

G9091

2D5V_S0

3D3V_S0 → INPUT / OUT → 2D5V_S0

G9091

0D9V_S3

5V_S5 → INPUT / OUT → 0D9V_S3

RT9026

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Output Signal
(O)

AD_IN

Input Power
VCC(I)
VCC(I)

Output Power
VCC(O)

AD+

Charger_MAX8731

CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN

Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0

Output Signal
LDO (O / 5.4V)
XTAL2/PB4 (O/5V)
XTAL1/PB3 (O/5V)

AD_IN
CHARGE_LED#
BL2#

Output Power
VCC (O)
VCC (O)

DCBATOUT
BT+

AD+

Input Power
DCIN (I)

TI TPS51124
1.8V / 1.2V

PM_SLP_S5#

Input Signal
S5
S3

Output Signal
PGOOD(OD / 3.3V)

1D8V_S3_PG

Input Power
VCC(I)
VCC(I)

DCBATOUT
5V_S5

Output Power
VCC(O)
VCC(O)

1.8V_S3
1.2V_S0

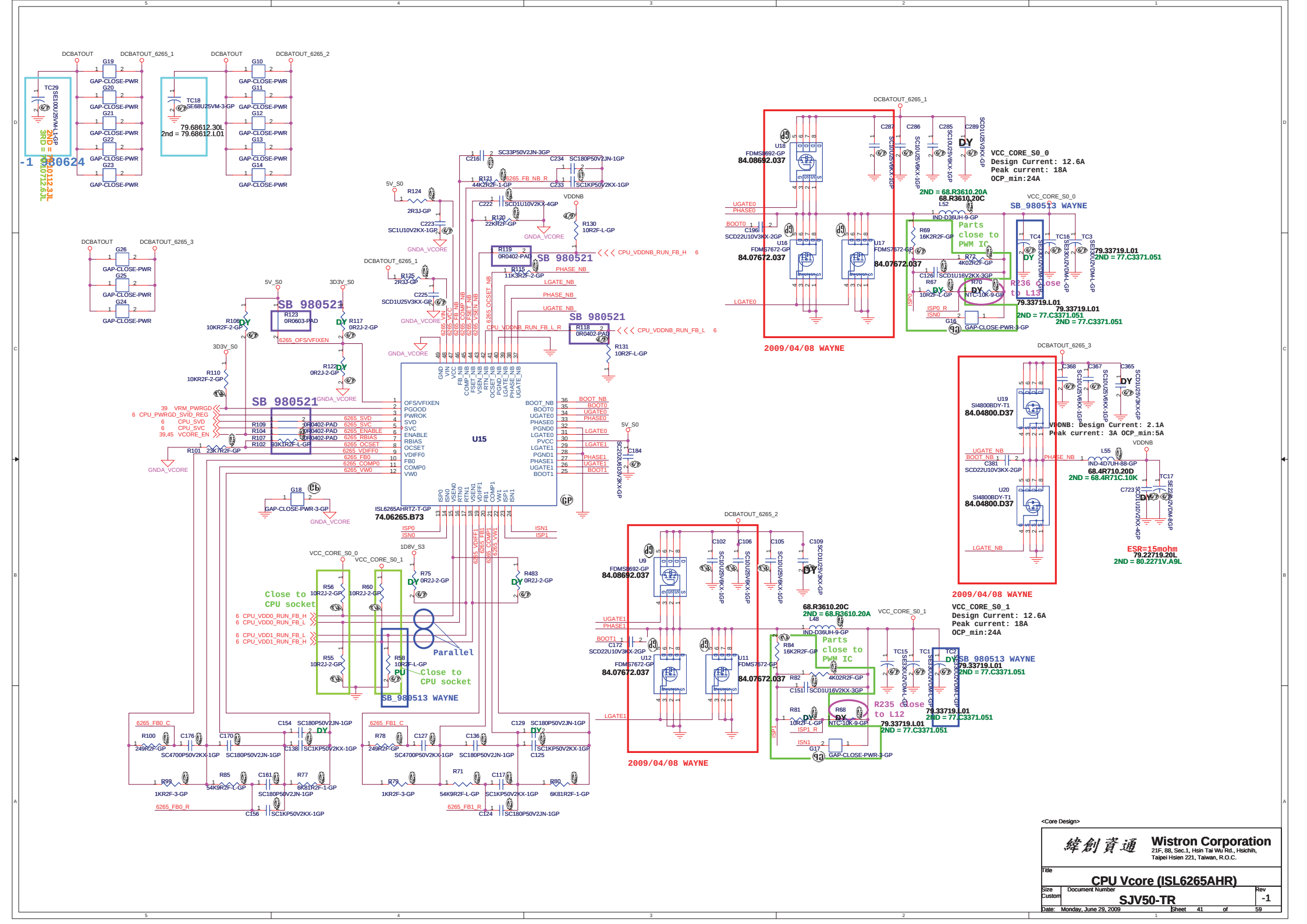
<Core Design>

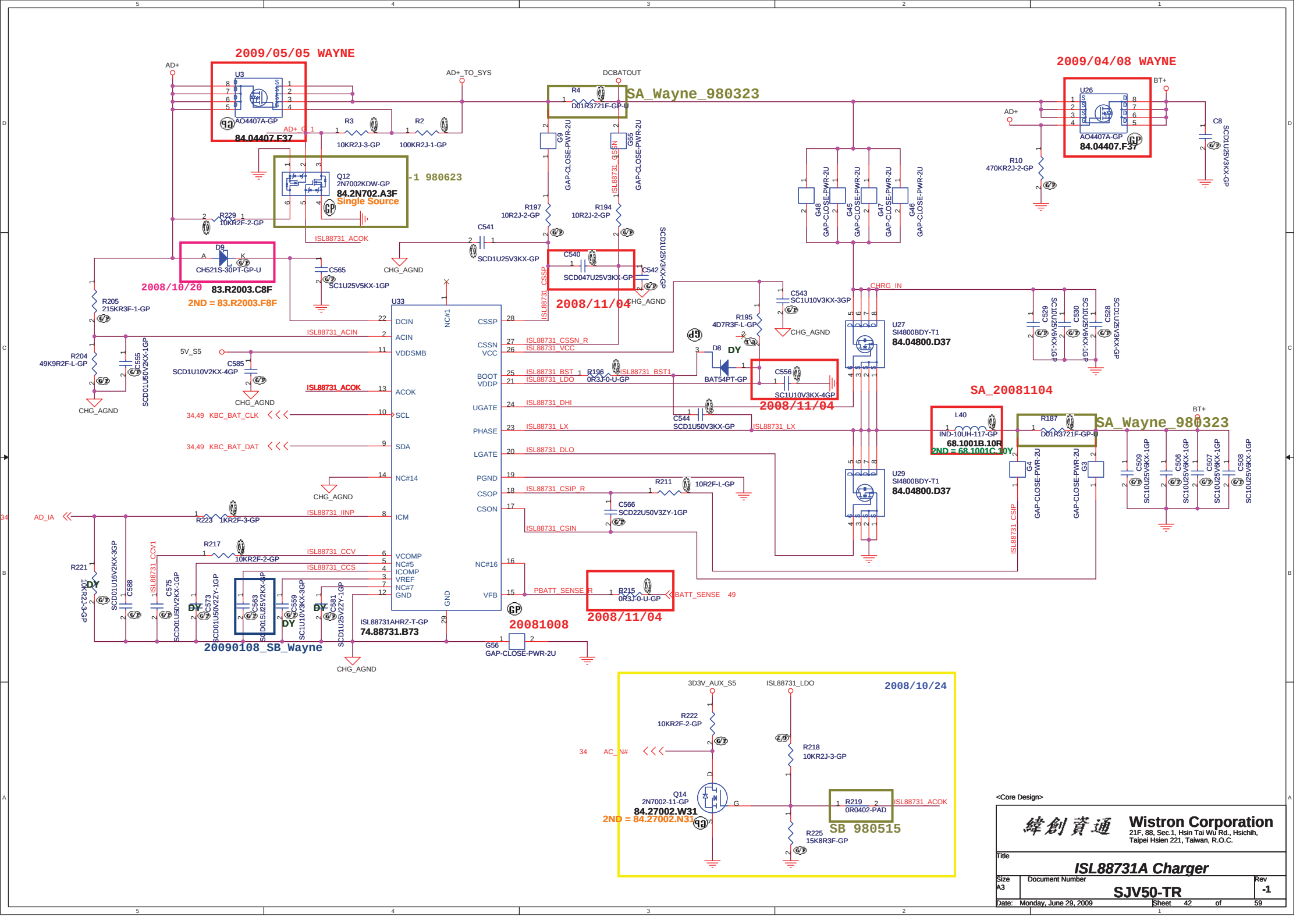
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

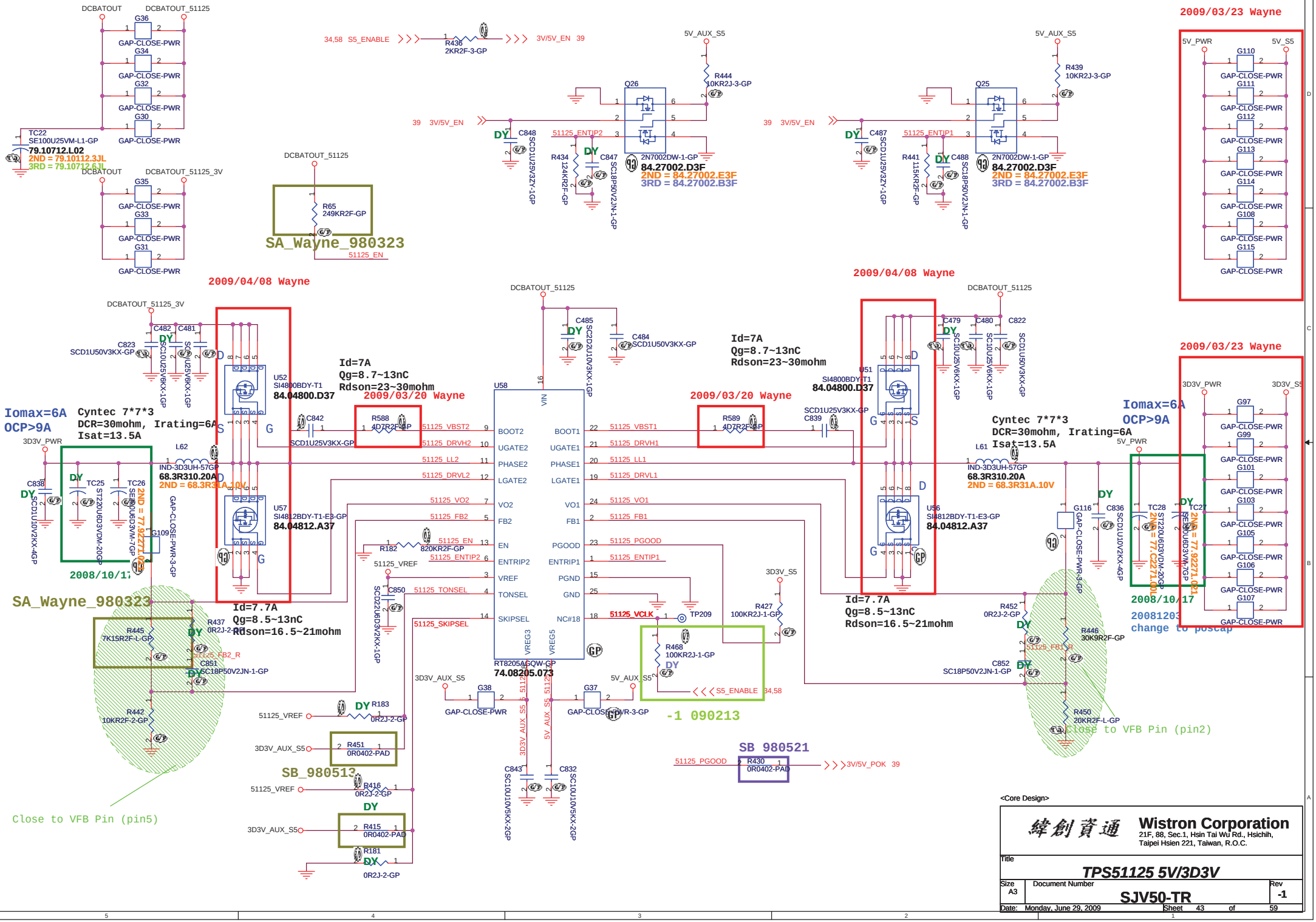
Title: **Power Block Diagram**

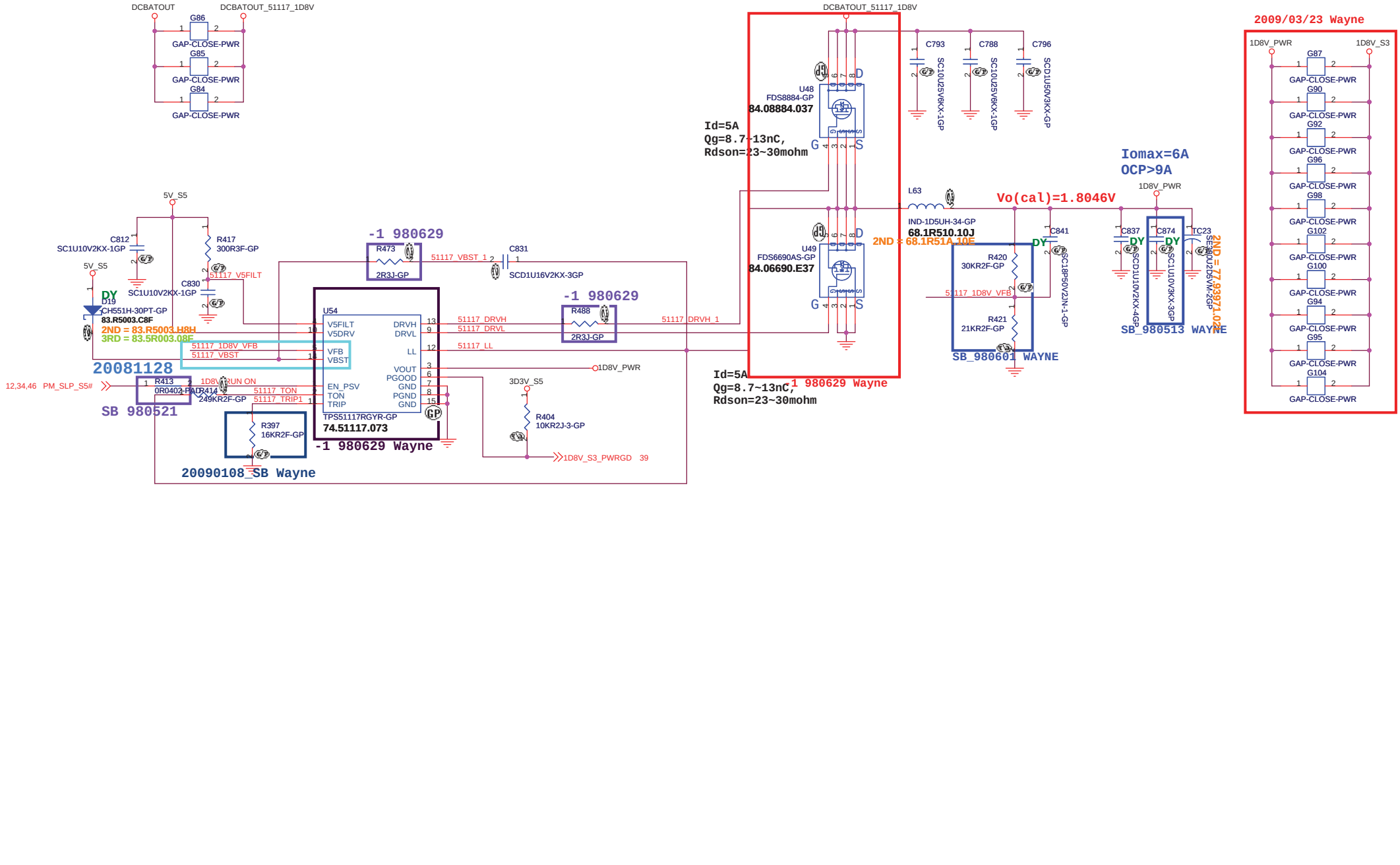
Size	Document Number	Rev
A3	SJV50-TR	-1

Date: Monday, June 29, 2009 Sheet 40 of 59


U15
ISL6265AHRTZ-T-GP
74.06265.B73
SB 980521
SB 980513 WAYNE
2009/04/08 WAYNE
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VCC_CORE_S0_1
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
Close to CPU socket
Parallel
Parts close to PWM IC
R235 Close to L12
R236 Close to L13
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore (ISL6265AHR)
SJV50-TR
Rev -1
Date: Monday, June 29, 2009
Sheet 41 of 59


2009/05/05 WAYNE
2009/04/08 WAYNE
SA_Wayne_980323
SA_Wayne_980323
SA_20081104
U3
AO4407A-GP
84.04407.F37
U26
AO4407A-GP
84.04407.F37
Q12
2N7002KDW-GP
84.2N702.A3F
Single Source
-1 980623
D9
CH521S-30PT-GP-U
2008/10/20
83.R2003.C8F
2ND = 83.R2003.F8F
U33
ISL88731AHRZ-T-GP
74.88731.B73
2008/11/04
2008/11/04
2008/11/04
20081008
20090108_SB_Wayne
U27
SI4800BDY-T1
84.04800.D37
U29
SI4800BDY-T1
84.04800.D37
L40
IND-10UH-117-GP
68.1001B.10R
2ND = 68.1001C.10Y
Q14
2N7002-11-GP
84.27002.W31
2ND = 84.27002.N31
SB 980515
2008/10/24
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A Charger
Size A3
Document Number SJV50-TR
Rev -1
Date: Monday, June 29, 2009
Sheet 42 of 59


2009/03/23 Wayne
2009/04/08 Wayne
2009/03/20 Wayne
SA_Wayne_980323
SA_Wayne_980513
SA_Wayne_980323
SB 980521
-1 090213
Iomax=6A
OCP>9A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
TPS51125 5V/3D3V
SJV50-TR
Monday, June 29, 2009



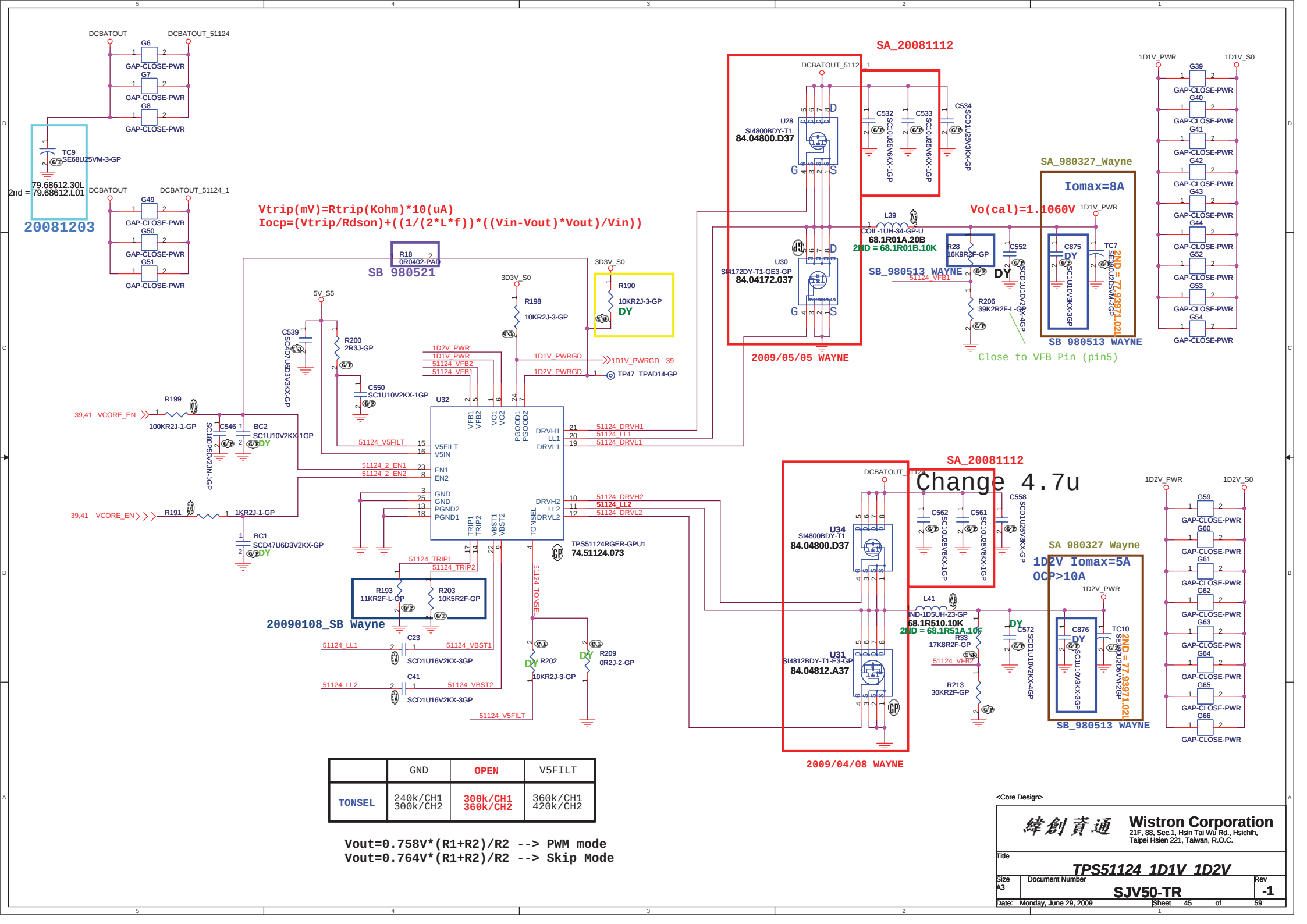
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPS51117_1D8V***

Size	Document Number	Rev
A3	SJV50-TR	-1

Date: Monday, June 29, 2009 Sheet 44 of 59



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

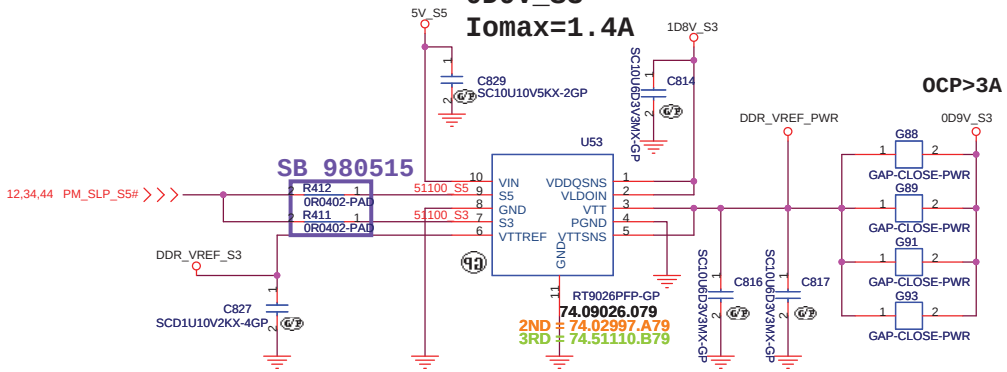
Title: TPS51124_1D1V_1D2V

Size	Document Number	Rev
A3	SJV50-TR	-1

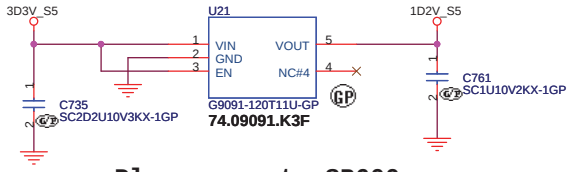
Date: Monday, June 29, 2009 Sheet 45 of 59

0D9V_S3
Iomax=1.4A

OCP>3A



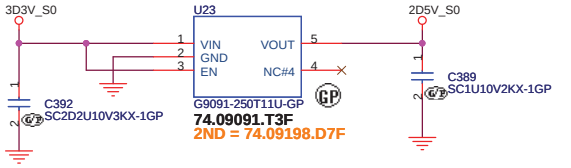
1D2V_S5
Iomax=0.2A



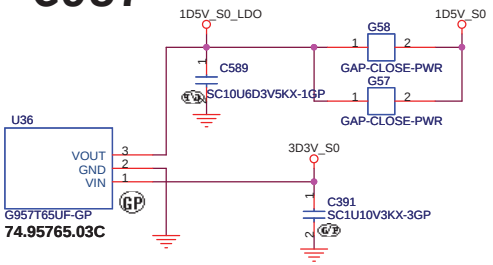
Place near to SB600

2D5V_S0
Iomax=200mA

OCP>430mA



G957
1D5V_S0
Iomax=1A

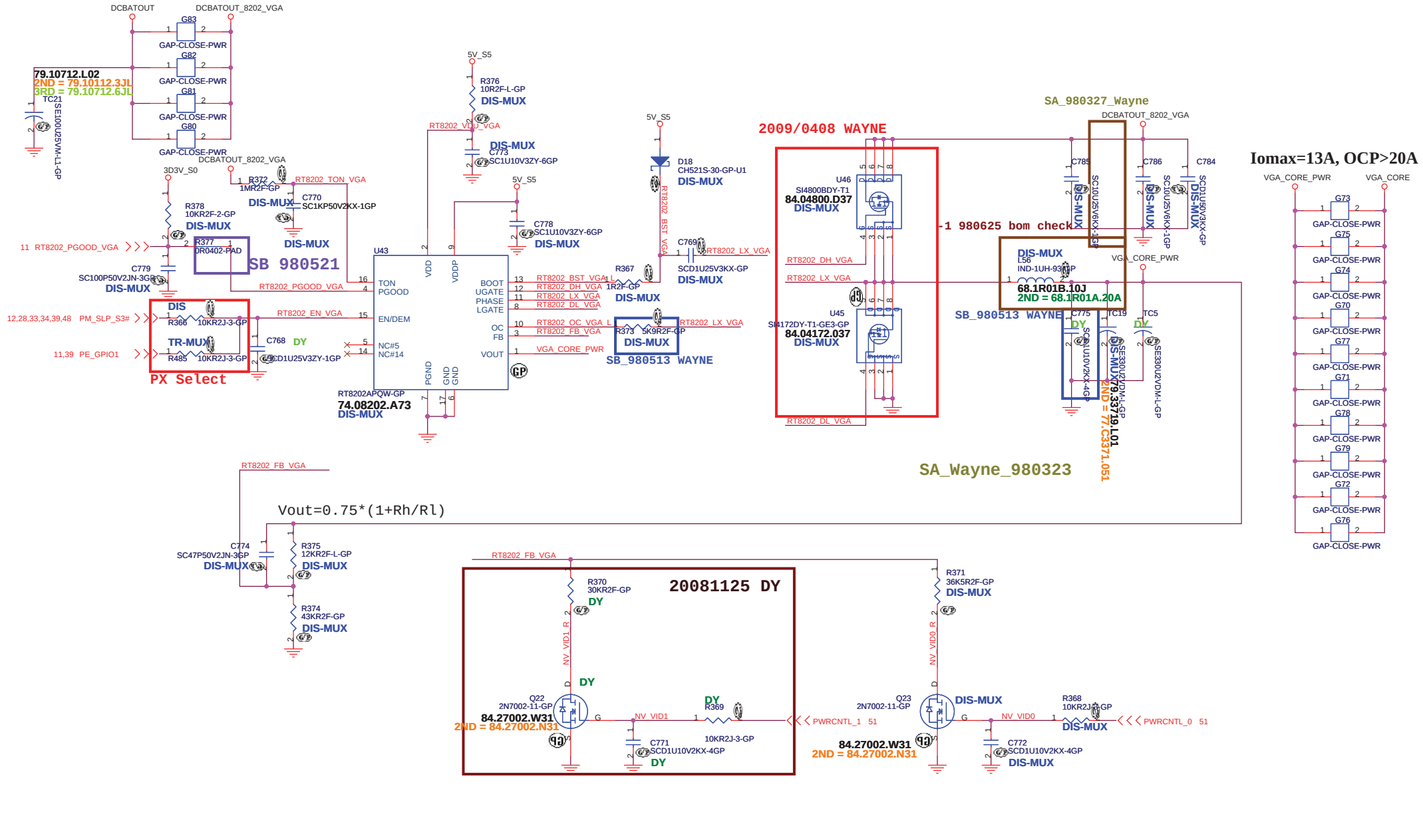


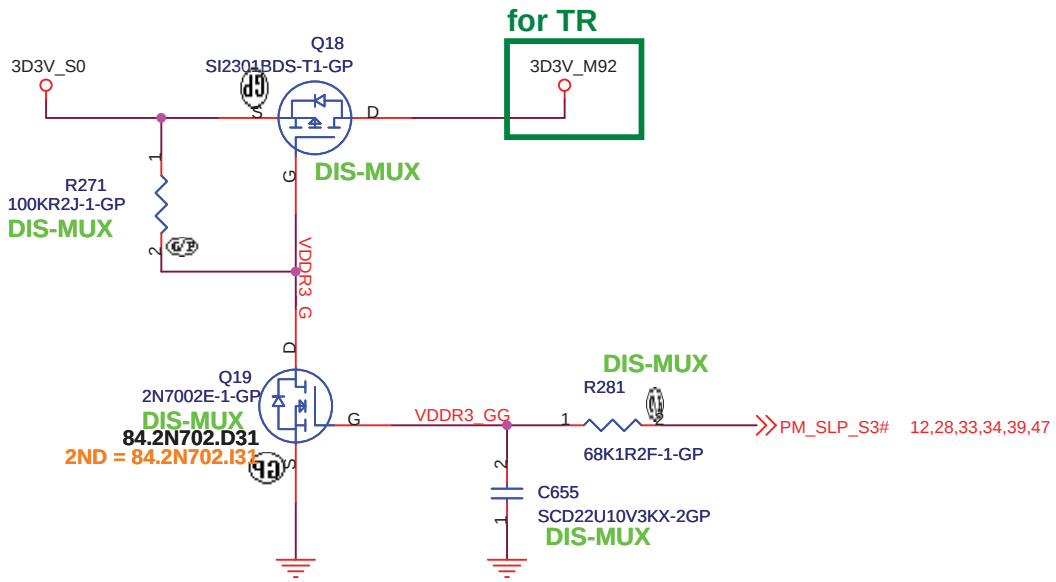
For MINI Card power SW

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 2D5V/1D5V0D9V		
Size: A3	Document Number: SJV50-TR	Rev: -1
Date: Monday, June 29, 2009	Sheet 46 of 59	


DCBATOUT
DCBATOUT_8202_VGA
79.10712.L02
2ND = 79.10112.3JL
3RD = 79.10712.6JL
GAP-CLOSE-PWR
3D3V_S0
5V_S5
SB 980521
PX Select
DIS-MUX
TR-MUX
U43
RT8202_PGOOD_VGA
RT8202_EN_VGA
RT8202_TON_VGA
RT8202_VDD_VGA
RT8202_BST_VGA
RT8202_DH_VGA
RT8202_LX_VGA
RT8202_DL_VGA
RT8202_OC_VGA_L
RT8202_FB_VGA
VGA_CORE_PWR
RT8202APQW-GP
74.08202.A73
SB_980513 WAYNE
2009/0408 WAYNE
SA_980327_Wayne
-1 980625 bom check
SB_980513 WAYNE
SA_Wayne_980323
Iomax=13A, OCP>20A
Vout=0.75*(1+Rh/Rl)
20081125 DY
PWRCNTL_1 51
PWRCNTL_0 51
84.27002.W31
2ND = 84.27002.N31
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
RT8202A_VGA CORE
SJV50-TR
Monday, June 29, 2009

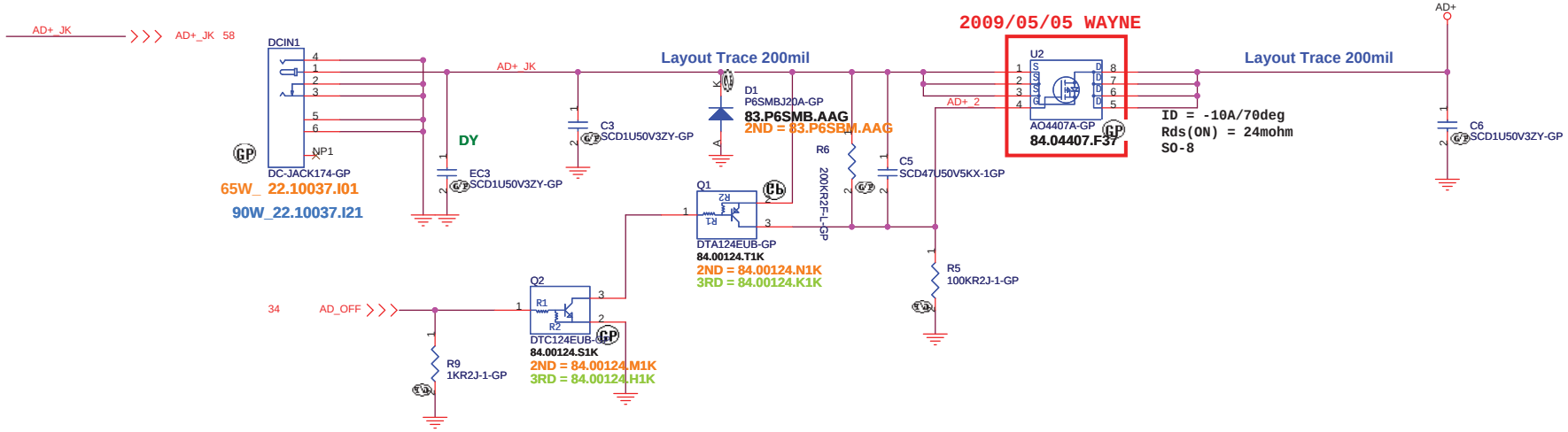


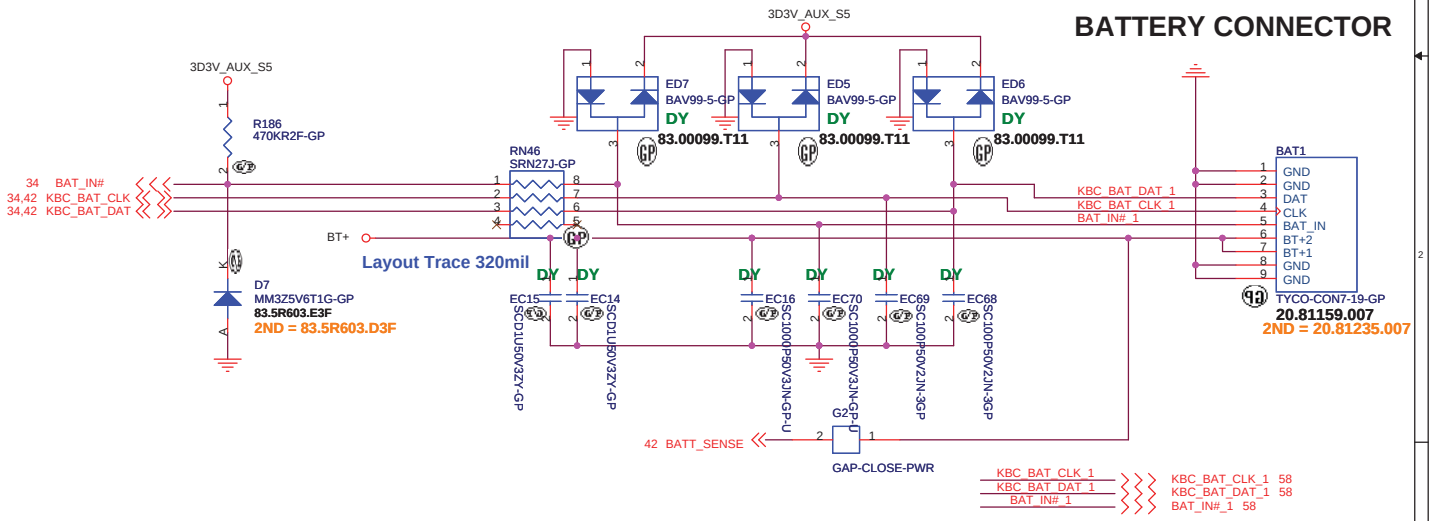
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***VDDR3***	
Size A4	Document Number **SJV50-TR**	Rev **-1**
Date: Monday, June 29, 2009	Sheet 48 of 59	

Adaptor in to generate DCBATOUT





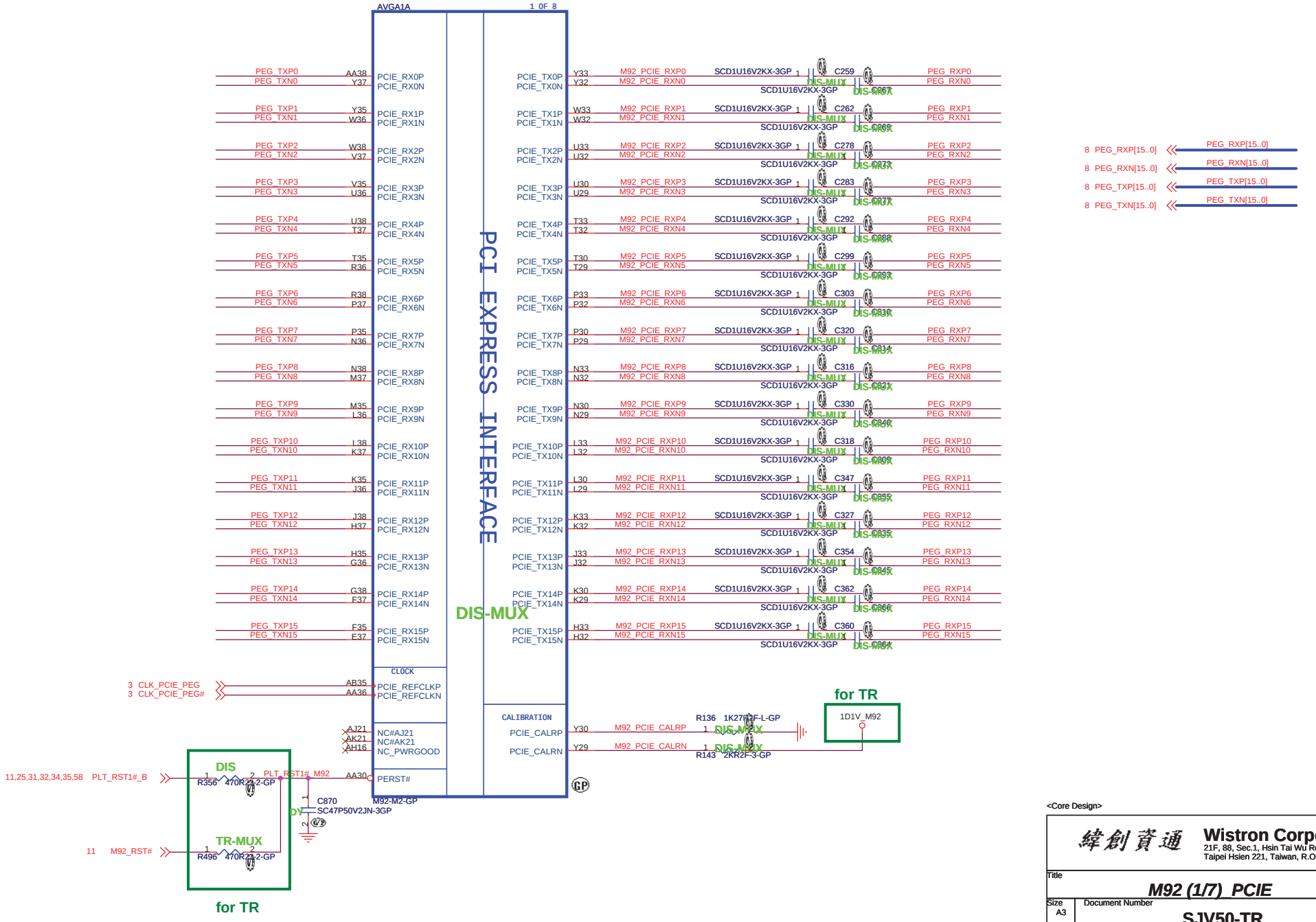
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

Size	Document Number	Rev
A3	SJV50-TR	-1

Date: Monday, June 29, 2009 Sheet 49 of 59



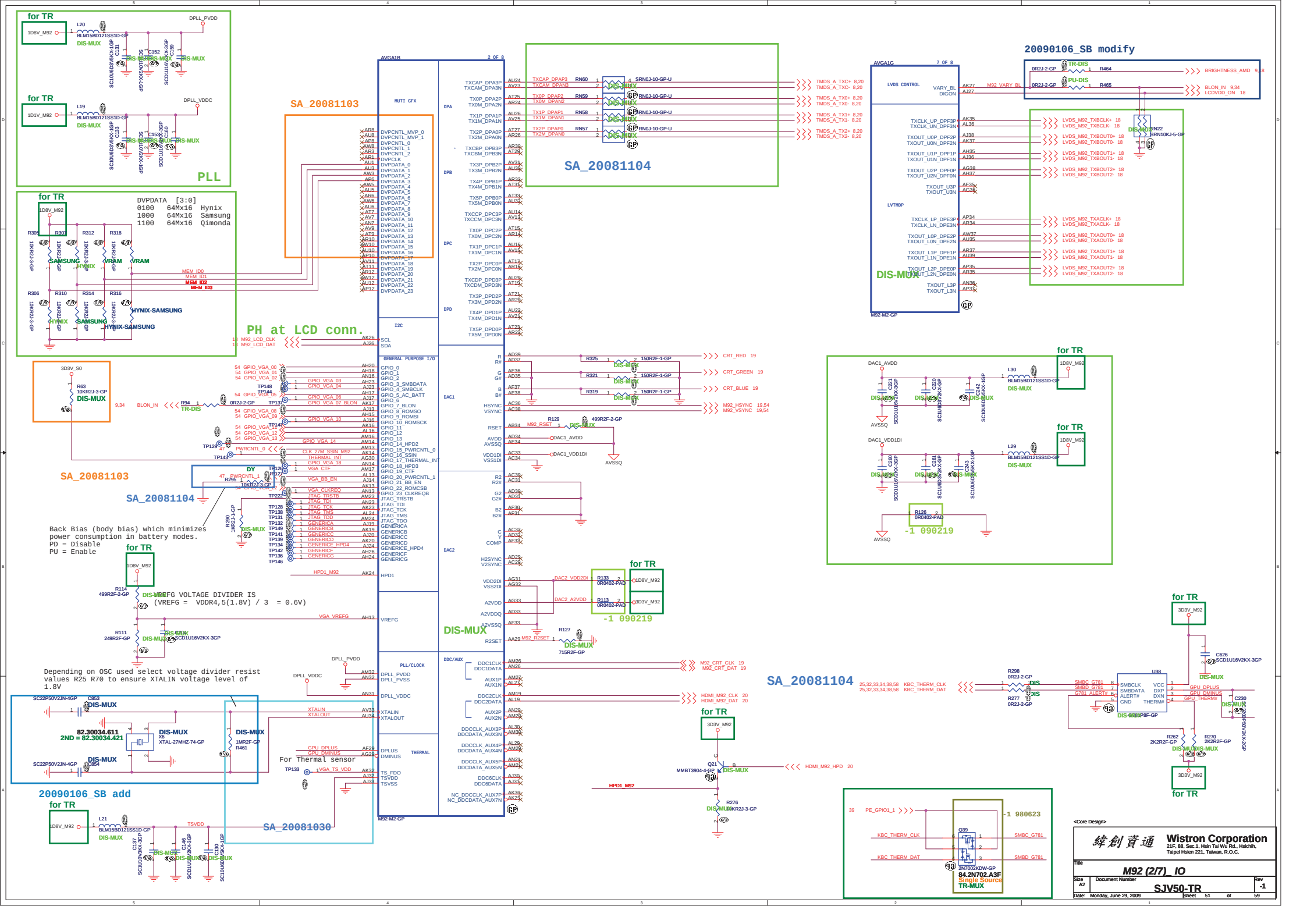
<Core Design>

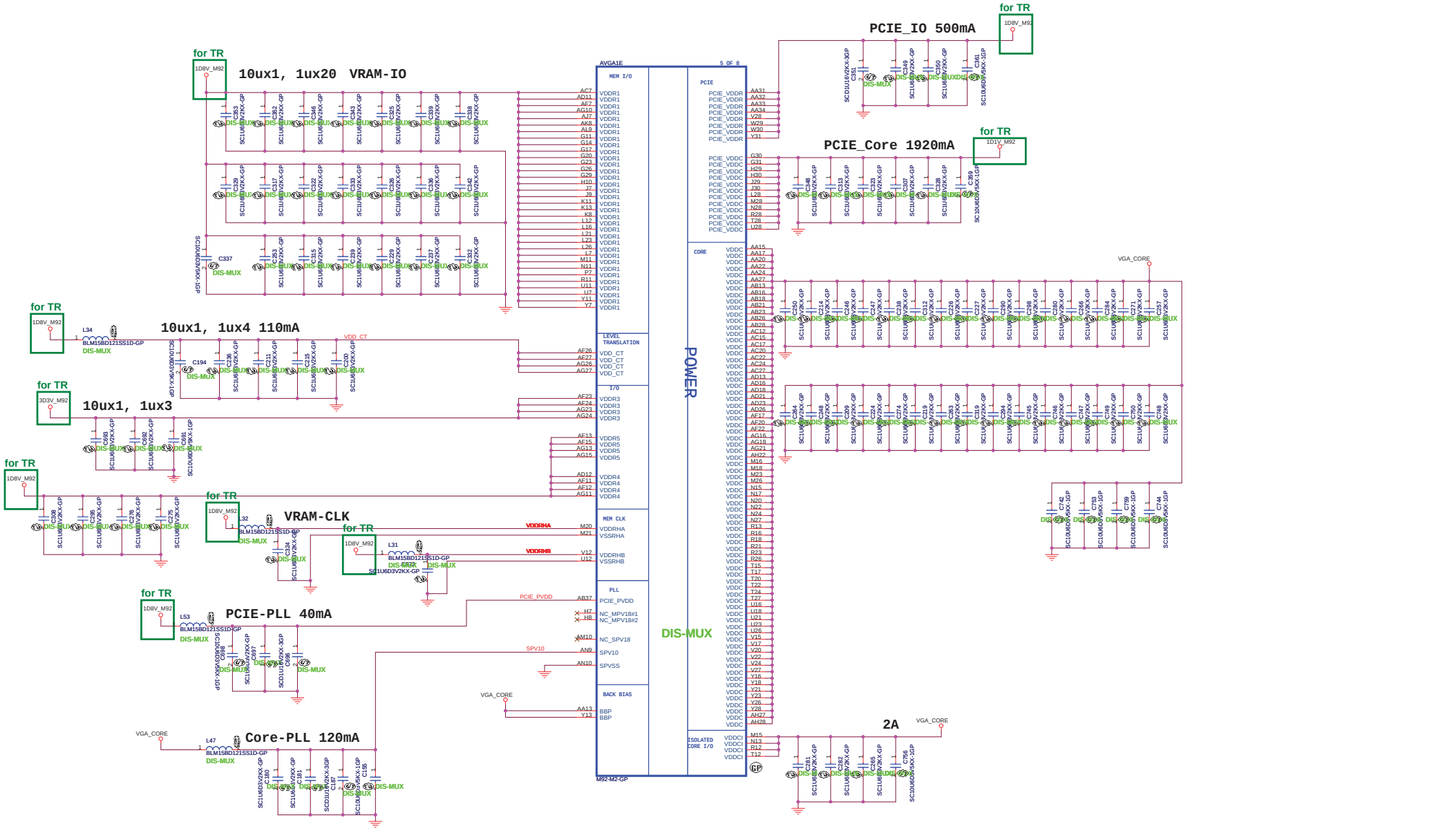
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: M92 (1/7) PCIE

Size	Document Number	Rev
A3	SJV50-TR	-1

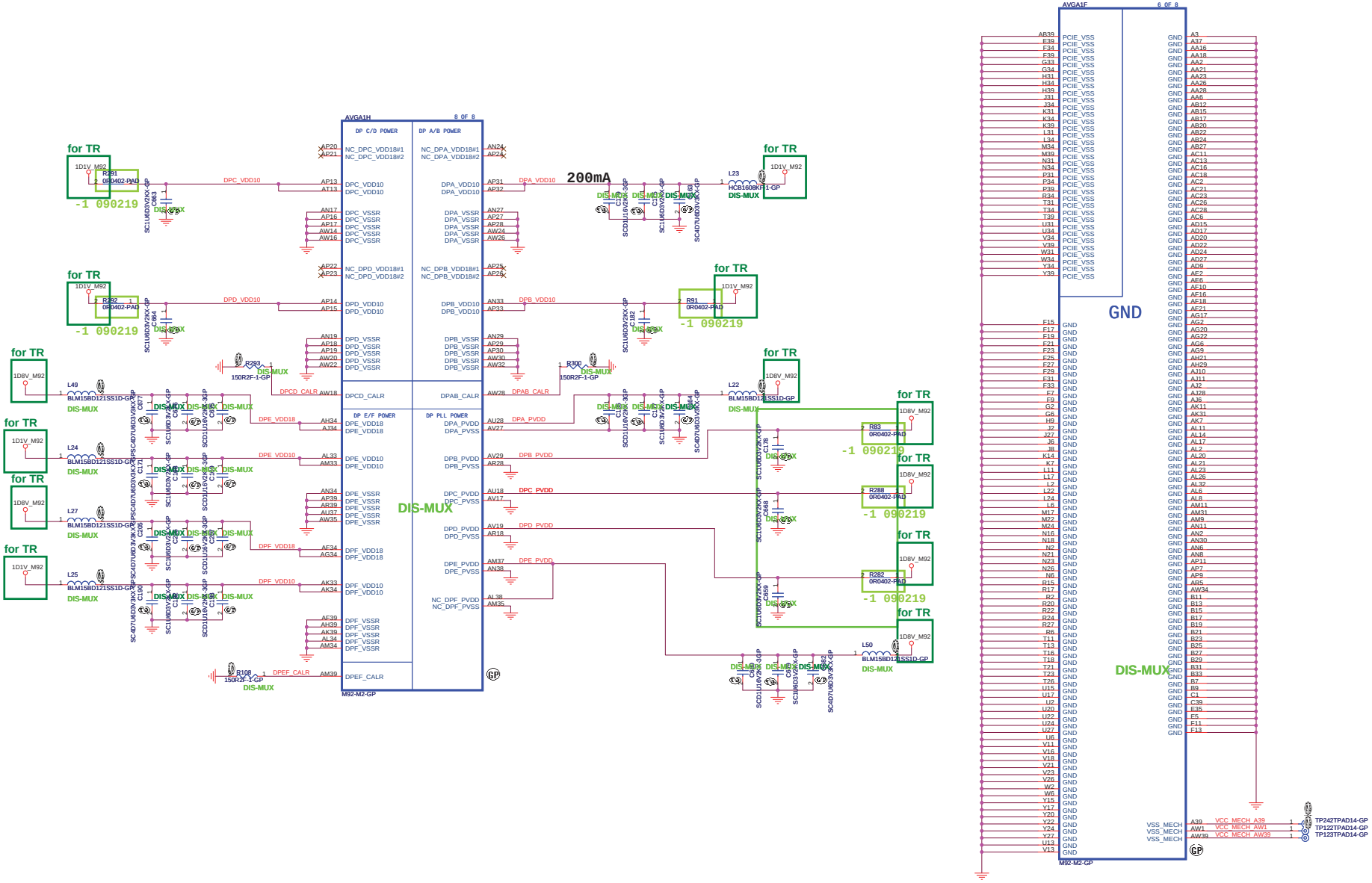
Date: Monday, June 29, 2009 Sheet 50 of 59


for TR
1D8V_M92
DPLL_PVDD
L20
BLM15BD121SS1D-GP
DIS-MUX
1D1V_M92
DPLL_VDDC
L19
PLL
DVPDATA [3:0]
0100 64Mx16 Hynix
1000 64Mx16 Samsung
1100 64Mx16 Qimonda
SAMSUNG
HYNIX
VRAM
HYNIX-SAMSUNG
MEM_ID0
MEM_ID1
MEM_ID2
MEM_ID3
SA_20081103
SA_20081104
PH at LCD conn.
M92_LCD_CLK
M92_LCD_DAT
3D3V_S0
R63
10KR2J-3-GP
BLON_IN
R94
TR-DIS
0R2J-2-GP
DY
Back Bias (body bias) which minimizes
power consumption in battery modes.
PD = Disable
PU = Enable
R114
499R2F-2-GP
VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)
VGA_VREFG
R111
249R2F-GP
Depending on OSC used select voltage divider resist
values R25 R70 to ensure XTALIN voltage level of
1.8V
82.30034.611
2ND = 82.30034.421
XTAL-27MHZ-74-GP
SA_20081030
20090106_SB add
TSVDD
L21
BLM15BD121SS1D-GP
AVGA1B
2 OF 8
MUTI GFX
I2C
GENERAL PURPOSE I/O
DAC1
DAC2
DDC/AUX
PLL/CLOCK
THERMAL
M92-M2-GP
SA_20081104
SRN0J-10-GP-U
RN0J-10-GP-U
TMDS_A_TXC+ 8,20
TMDS_A_TXC- 8,20
TMDS_A_TX0+ 8,20
TMDS_A_TX0- 8,20
TMDS_A_TX1+ 8,20
TMDS_A_TX1- 8,20
TMDS_A_TX2+ 8,20
TMDS_A_TX2- 8,20
20090106_SB modify
AVGA1G
7 OF 8
LVDS CONTROL
DIS-MUX
M92-M2-GP
TR-DIS
PU-DIS
R464
R465
BRIGHTNESS_AMD 9,18
BLON_IN 9,34
LCDVDD_ON 18
SRN10KJ-5-GP
LVDS_M92_TXBCLK+ 18
LVDS_M92_TXBCLK- 18
LVDS_M92_TXBOUT0+ 18
LVDS_M92_TXBOUT0- 18
LVDS_M92_TXBOUT1+ 18
LVDS_M92_TXBOUT1- 18
LVDS_M92_TXBOUT2+ 18
LVDS_M92_TXBOUT2- 18
LVDS_M92_TXACLK+ 18
LVDS_M92_TXACLK- 18
LVDS_M92_TXAOUT0+ 18
LVDS_M92_TXAOUT0- 18
LVDS_M92_TXAOUT1+ 18
LVDS_M92_TXAOUT1- 18
LVDS_M92_TXAOUT2+ 18
LVDS_M92_TXAOUT2- 18
CRT_RED 19
CRT_GREEN 19
CRT_BLUE 19
M92_HSYNC 19,54
M92_VSYNC 19,54
499R2F-2-GP
DAC1_AVDD
DAC1_VDD1DI
L30
L29
BLM15BD121SS1D-GP
-1 090219
DAC2_VDD2DI
DAC2_A2VDD
M92_R2SET
715R2F-GP
M92_CRT_CLK 19
M92_CRT_DAT 19
HDMI_M92_CLK 20
HDMI_M92_DAT 20
HDMI_M92_HPD 20
MMBT3904-4-GP
HPD1_M92
SA_20081104
KBC_THERM_CLK
KBC_THERM_DAT
SMBC_G781
SMBD_G781
GPU_DPLUS
GPU_DMINUS
GPU_THERM#
-1 980623
2N7002KDW-GP
84.2N702.A3F
Single Source
TR-MUX
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
M92 (2/7)_ IO
Size A2
Document Number
SJV50-TR
Rev -1
Date: Monday, June 29, 2009
Sheet 51 of 59



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *M92 (3/7) Power*		
Size: A2	Document Number: SJV50-TR	Rev: -1
Date: Monday, June 29, 2009	Sheet 52 of 59	



<Core Design>

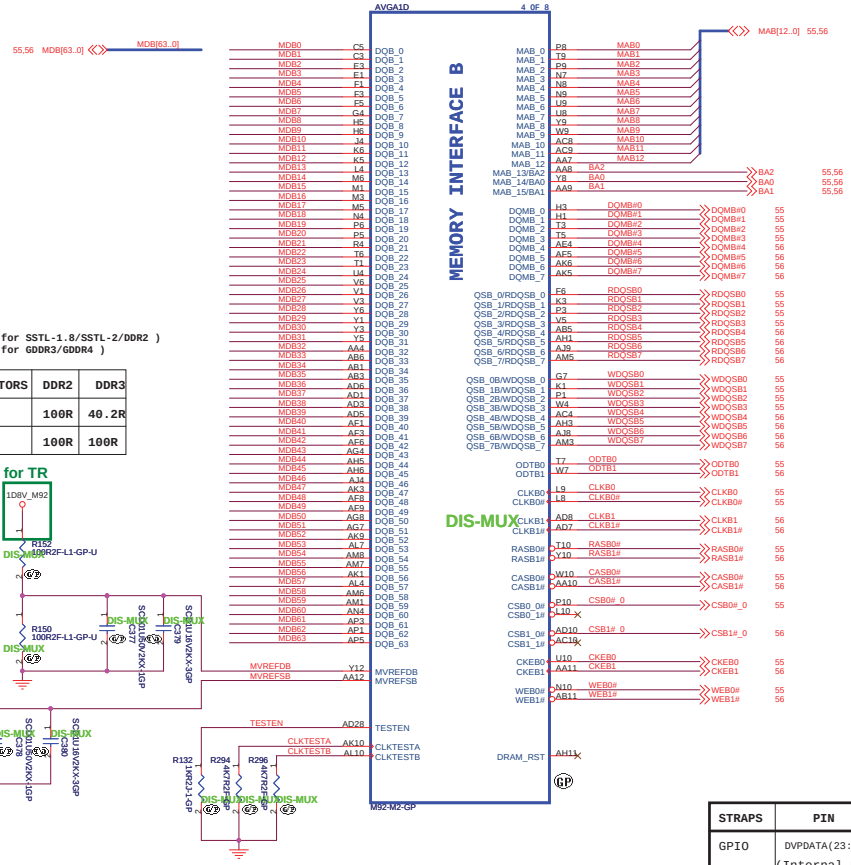
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: M92 (4/7) DP POWER_GND

Size	Document Number	Rev
A2	SJV50-TR	-1

Date: Monday, June 29, 2009 Sheet 53 of 59

M92-M2 uses memory group B only

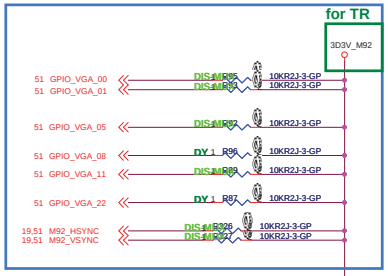


(0.5 * VDDR1) (for SSTL-1.8/SSTL-2/DDR2)
(0.7 * VDDR1) (for GDDR3/GDDR4)

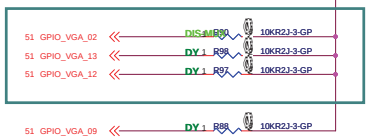
DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

STRAPS	PIN	DESCRIPTION
GPIO	DVPDATA(23:20) (Internal PD)	Initialization Behavior: This signal is input during reset (no reference clock is required). After reset, the default state is output low (0 V). The signals above can be left unconnected if not used.

SA_20081104



SA_20081105



HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

STRAPS	PIN	DESCRIPTION
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s
AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V
ROMSO	GPIO8	BIF_CLK_PM_EN Serial ROM Output from ROM
ROMSI	GPIO9	VGA ENABLED Serial ROM Input to ROM
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory apeture size
PWRCNTL_[1,0]	GPIO[15,20]	Power control signals to control the core voltage regulator
BB_EN	GPIO21	Back Bias (body bias) which minimizes power consumption in battery modes. 0V = Disable 3D3V = Enable
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI
CCBYPASS	GENERICC	

RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
1
1
1
0
0
X X X
0
1
0

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO , GPIO21_BB_EN

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

<Core Design>

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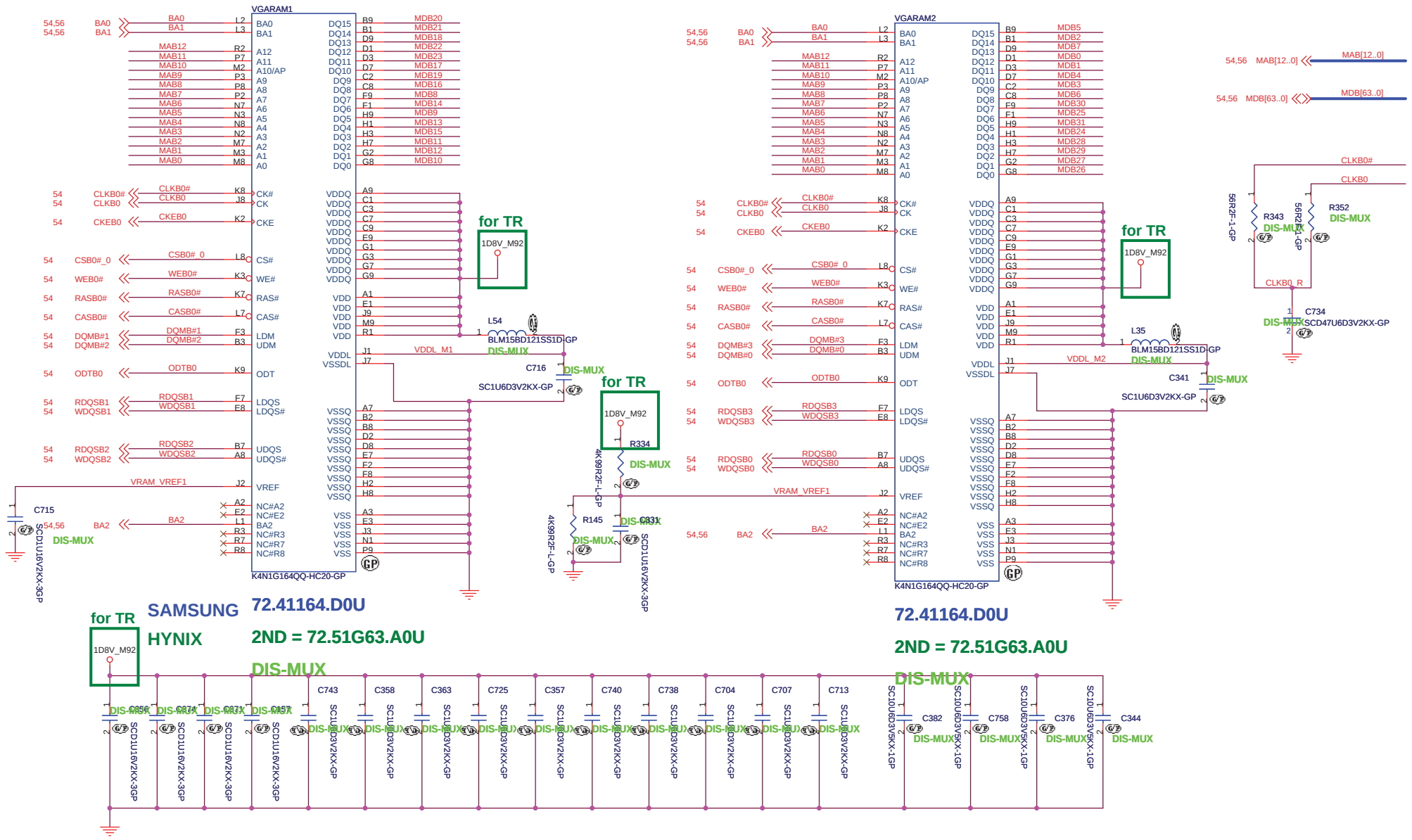
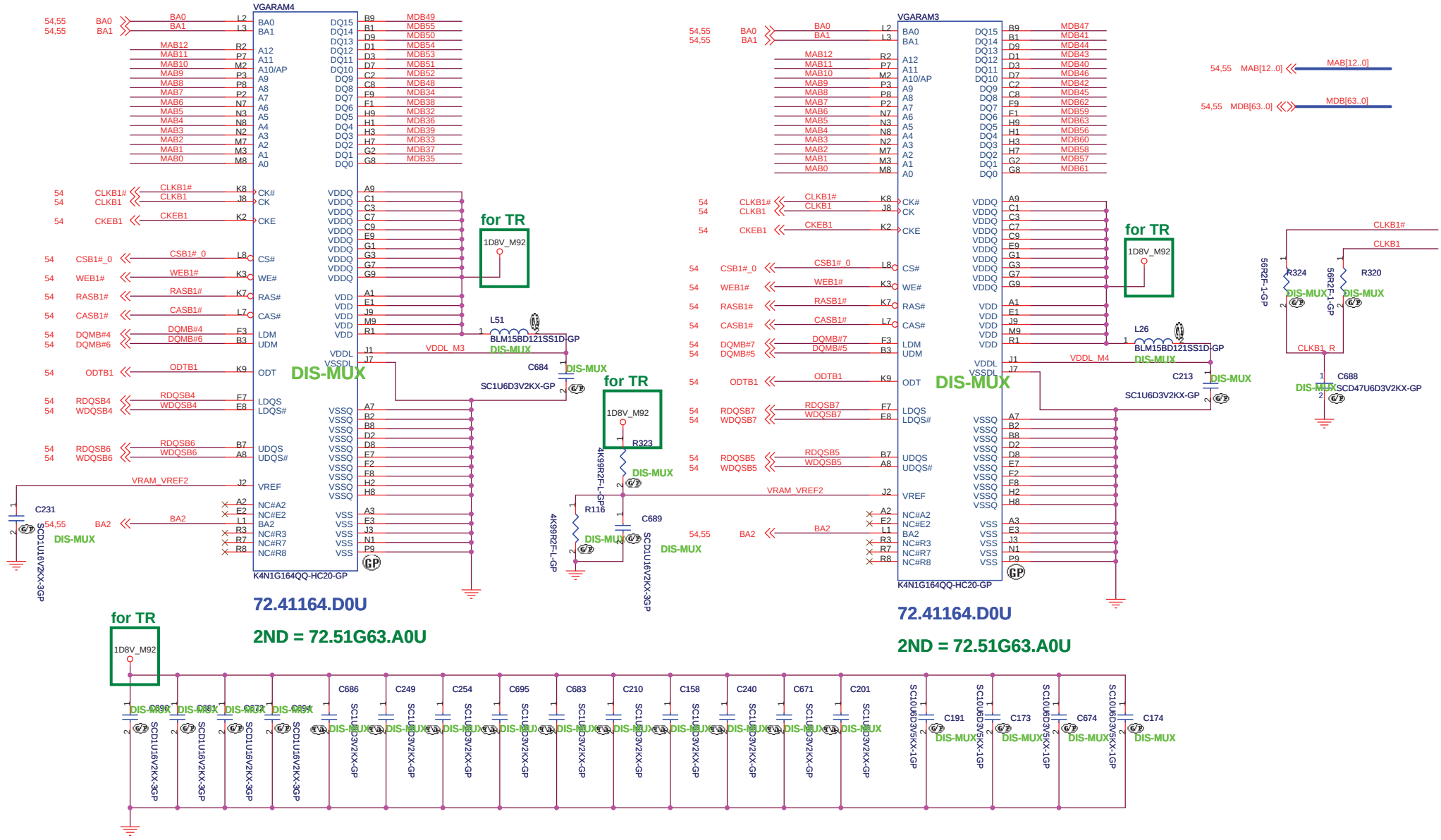
Title: M92 (5/7) Memory Straps

Size: A2 | Document Number: SJV50-TR | Rev: -1

Date: Monday, June 29, 2009 | Sheet 54 of 59


VGARAM1
K4N1G164QQ-HC20-GP
VGARAM2
K4N1G164QQ-HC20-GP
for TR
1D8V_M92
DIS-MUX
SAMSUNG
HYNIX
72.41164.D0U
2ND = 72.51G63.A0U
DIS-MUX
72.41164.D0U
2ND = 72.51G63.A0U
DIS-MUX
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
M92 (6/7) VRAM B0
Size A3
Document Number
SJV50-TR
Rev -1
Date: Monday, June 29, 2009
Sheet 55 of 59



<Core Design>

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Title: M92 (7/7) VRAM B1

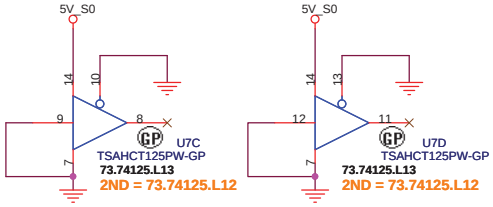
Size	Document Number	Rev
A3	SJV50-TR	-1

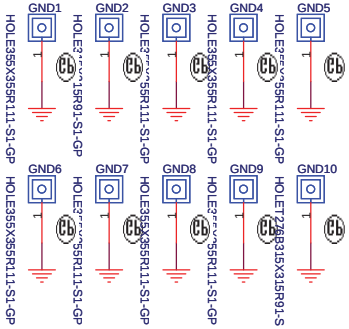
Date: Monday, June 29, 2009 Sheet 56 of 59

SA

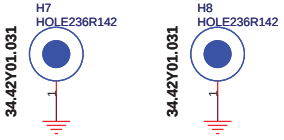
SB

-1

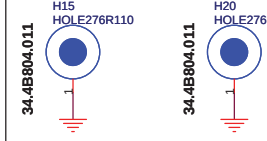




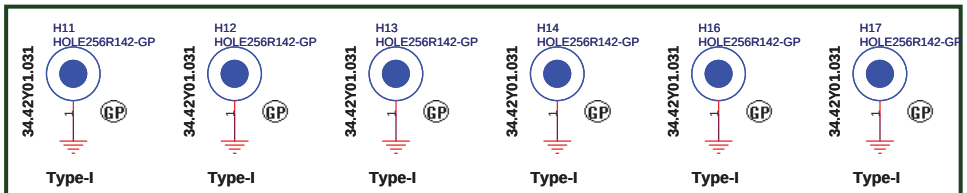
use 34.42Y01.031
M-STANDOFF
2nd 34.42Y01.021



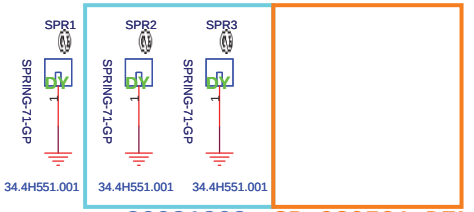
use 34.4B804.011
S-STANDOFF
2nd 34.4B804.001



DY



use 34.42Y01.031/ZZ.00PAD.801
2nd 34.42Y01.021

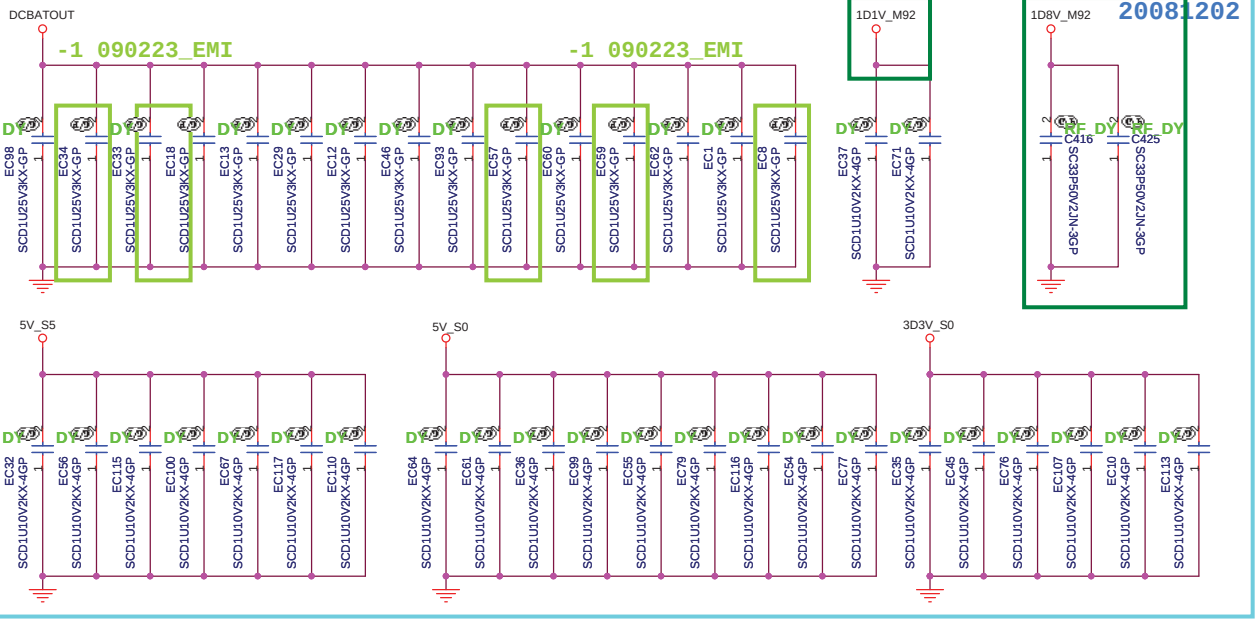


20081203 SB 980521 DEL

for TR

SB 980519_RF

20081202



<Core Design>

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Title: EMI/Spring/Boss

Size | Document Number: SJV50-TR | Rev: -1

Date: Monday, June 29, 2009 | Sheet 57 of 59

BT Conn. Test Point

23 USB_5- → TE14P-GP TP214
23 USB_5+ → TE14P-GP TP212
23 3D3V_BT_S0 → TE14P-GP TP210
AFTE14P-GP TP43

AD+, BAT Conn. Test Point

49 AD+_JK → AFTE14P-GP TP6, AFTE14P-GP TP5
AFTE14P-GP TP22
AFTE14P-GP TP17
49 KBC_BAT_CLK_1 → AFTE14P-GP TP7
49 KBC_BAT_DAT_1 → TE14P-GP TP9
49 BAT_IN#_1 → TE14P-GP TP8
BT+ → TE14P-GP TP15
TE14P-GP TP12
AFTE14P-GP TP19
AFTE14P-GP TP21

FAN Conn. Test Point

33 FAN1_VCC → TE14P-GP TP94
33 FAN1_FG1 → AFTE14P-GP TP92
AFTE14P-GP TP63

TouchPad Conn. Test Point

5V_S0 → AFTE14P-GP TP192
AFTE14P-GP TP188
36 TP_DATA → AFTE14P-GP TP189
36 TP_CLK → TE14P-GP TP187
TE14P-GP TP184
TE14P-GP TP185
36,37 TP_RIGHT → AFTE14P-GP TP173
36,37 TP_LEFT → AFTE14P-GP TP174

KB Conn. Test Point

34 KCOL1 → TE14P-GP TP75
34 KCOL2 → TE14P-GP TP83
34 KCOL3 → TE14P-GP TP101
34 KCOL4 → TE14P-GP TP78
34 KCOL5 → TE14P-GP TP91
34 KCOL6 → TE14P-GP TP104
34 KCOL7 → TE14P-GP TP82
34 KCOL8 → TE14P-GP TP99
34 KCOL9 → TE14P-GP TP89
34 KCOL10 → TE14P-GP TP103
34 KCOL11 → TE14P-GP TP79
34 KCOL12 → TE14P-GP TP98
34 KCOL13 → TE14P-GP TP84
34 KCOL14 → TE14P-GP TP102
34 KCOL15 → TE14P-GP TP90
34 KCOL16 → TE14P-GP TP100
34 KCOL17 → AFTE14P-GP TP105
34 KCOL18 → TE14P-GP TP81
34 KROW1 → TE14P-GP TP93
34 KROW2 → TE14P-GP TP80
34 KROW3 → TE14P-GP TP85
34 KROW4 → TE14P-GP TP95
34 KROW5 → TE14P-GP TP86
34 KROW6 → TE14P-GP TP88
34 KROW7 → TE14P-GP TP96
34 KROW8 → TE14P-GP TP87
AFTE14P-GP TP50

USBCN1 Conn. Test Point

12,24 USB_OC#3 → TE14P-GP TP20
TE14P-GP TP24
12,23 USBPN5 → AFTE14P-GP TP213
12,23 USBPP5 → TE14P-GP TP211
TE14P-GP TP61
12,24 USBPN7 → AFTE14P-GP TP25
12,24 USBPP7 → TE14P-GP TP30
TE14P-GP TP31
TE14P-GP TP16
24,34 USB_PWR_EN# → TE14P-GP TP34
5V_S5 → TE14P-GP TP41
5V_S5 → TE14P-GP TP40
5V_S5 → AFTE14P-GP TP46
5V_S5 → AFTE14P-GP TP45

PowerButton Conn. Test Point

37 KBC_PWRBTN#_R → TE14P-GP TP11
AFTE14P-GP TP225

AMic Conn. Test Point

18,27 INT_MIC1 → TE14P-GP TP13
AFTE14P-GP TP10

CCD Conn. Test Point

18 CCD_PWR → AFTE14P-GP TP27
18 USBPN10_R → AFTE14P-GP TP18
18 USBPP10_R → TE14P-GP TP14
AFTE14P-GP TP26
AFTE14P-GP TP23

MMB Conn. Test Point

3D3V_S0 → AFTE14P-GP TP51
TE14P-GP TP49
25,32,33,34,38,51 KBC_THERM_CLK → AFTE14P-GP TP65
25,32,33,34,38,51 KBC_THERM_DAT → AFTE14P-GP TP66
TE14P-GP TP53
TE14P-GP TP32
34,38 MEDIA_INT → TE14P-GP TP58
38 WLAN_LED#_MMB → TE14P-GP TP57
38 CAP_LED#_MMB → TE14P-GP TP59
38 NUM_LED#_MMB → TE14P-GP TP56
38 MEDIA_LED#_MMB → TE14P-GP TP55
3D3V_S0 → TE14P-GP TP60
38 BT_LED#_MMB → TE14P-GP TP54
AFTE14P-GP TP35
AFTE14P-GP TP42

SPKR Conn. Test Point

29 SPKR_L-_R → TE14P-GP TP3
29 SPKR_L+_R → TE14P-GP TP1
29 SPKR_R-_R → AFTE14P-GP TP2
29 SPKR_R+_R → AFTE14P-GP TP4

Check test point

3D3V_AUX_S5 → TE14P-GP TP71
3D3V_S5 → TE14P-GP TP208
3D3V_S0 → AFTE14P-GP TP157
5V_S5 → TE14P-GP TP195
12,34 PM_PWRBTN# → AFTE14P-GP TP167
6,9 LDT_RST#_CPU → AFTE14P-GP TP37
6,11 CPU_PWRGD → AFTE14P-GP TP191
34,43 S5_ENABLE → AFTE14P-GP TP124
13 PSW_CLR# → G27 GAP-OPEN

20081201

Test Point放在Dimm Door打開可量測處

3D3V_S0 → TE14P-GP TP155
11,34,35 LPC_LAD0 → AFTE14P-GP TP153
11,34,35 LPC_LAD1 → AFTE14P-GP TP150
11,34,35 LPC_LAD2 → AFTE14P-GP TP145
11,34,35 LPC_LAD3 → AFTE14P-GP TP135
11,34,35 LPC_LFRAME# → TE14P-GP TP130
11,25,31,32,34,35,50 PLT_RST1#_B → TE14P-GP TP62
11,15,35 PCLK_FWH → TE14P-GP TP119
TE14P-GP TP117
AFTE14P-GP TP111
AFTE14P-GP TP121

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Title: Test point		
Size	Document Number: SJV50-TR	Rev: -1
Date: Monday, June 29, 2009	Sheet 58 of 59	

R297-->PU-DIS & TR-DIS 0 ohm
PU-UMA & TR-UMA & MUX 5.1K ohm

R52-->PU-DIS & TR-DIS 100K ohm
PU-UMA & TR-UMA & MUX 10K ohm

C645~C652
Non-Level shift UMA mount 0 ohm
DIS use DUMMY

<Core Design>

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Title: Change List

Size | Document Number: SJV50-TR | Rev: -1

Date: Monday, June 29, 2009 | Sheet 59 of 59