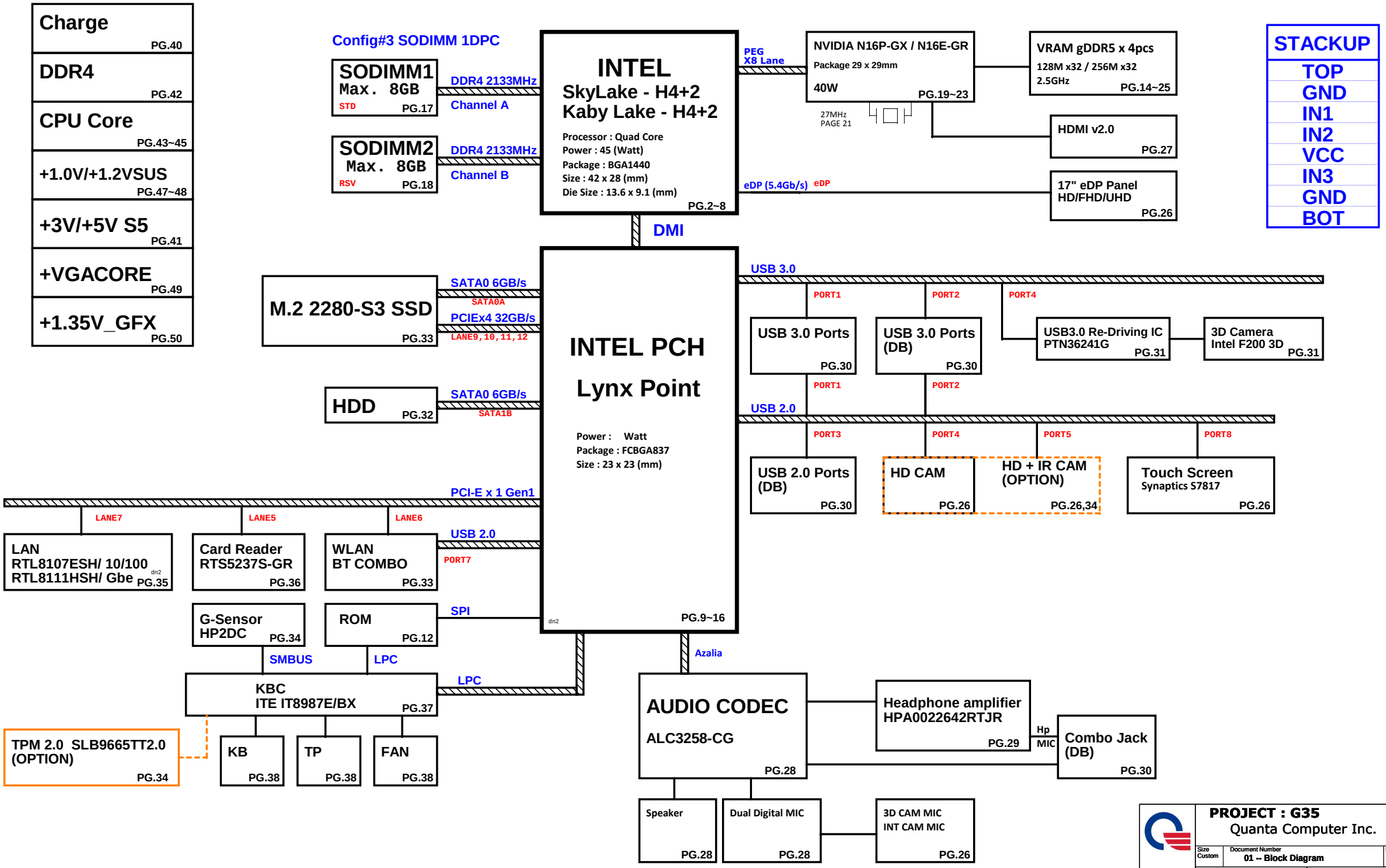
POWER PAVILION PUFF INTEL SKL / KABY -H SYSTEM DIAGRAM

01



PROJECT : G35
Quanta Computer Inc.

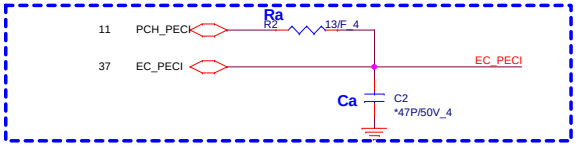
Size	Document Number	Rev
Custom	01 -- Block Diagram	1A

Date: Thursday, December 24, 2015 | Sheet 1 of 51

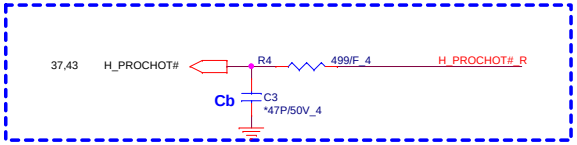
SKYLAKE Processor (CLK,MISC,JTAG)

02

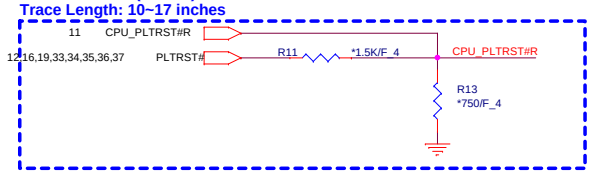
H_PECI (50ohm)
Trace Length: <0.5 iches
Ra,Ca need placement close to PCH.



PROCHOT# (50ohm)
Trace Length <11 inches
Cb need placment near VR

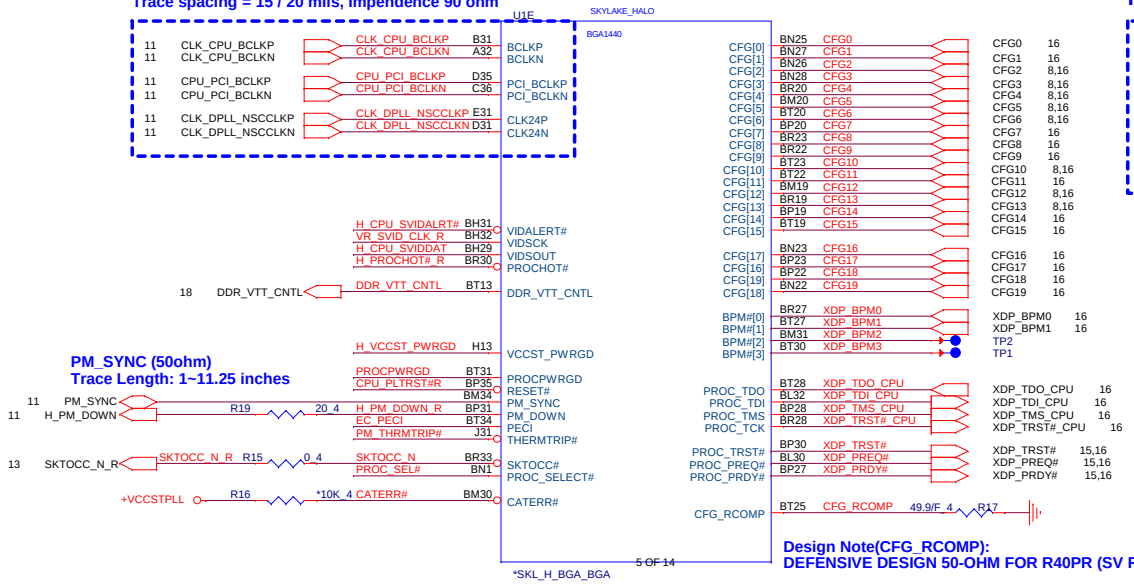


CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

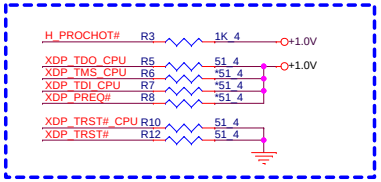


Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impendence 90 ohm

PM_SYNC (50ohm)
Trace Length: 1~11.25 inches



Processor pull-up (CPU)

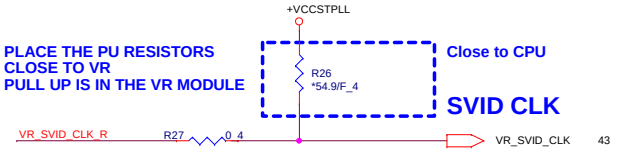


Design Note(CFG_RCOMP):
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

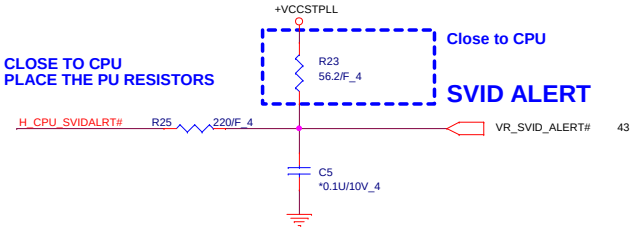
CPU CORE SVID

Layout note:
1.Need routing together
2.ALERT need between CLK and DATA.

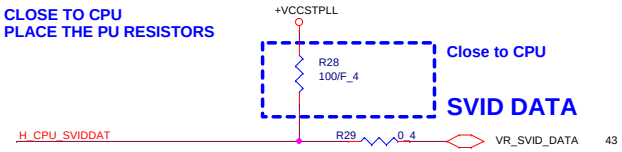
PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE



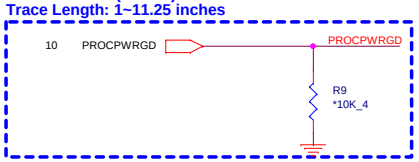
CLOSE TO CPU
PLACE THE PU RESISTORS



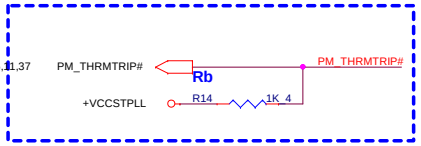
CLOSE TO CPU
PLACE THE PU RESISTORS



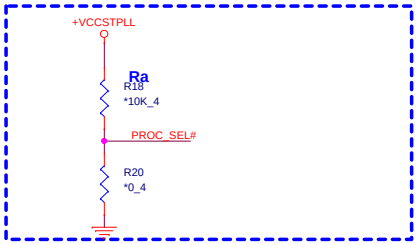
PROCPWRGD (50ohm)
Trace Length: 1~11.25 inches



THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches
Rb need placment near PCH

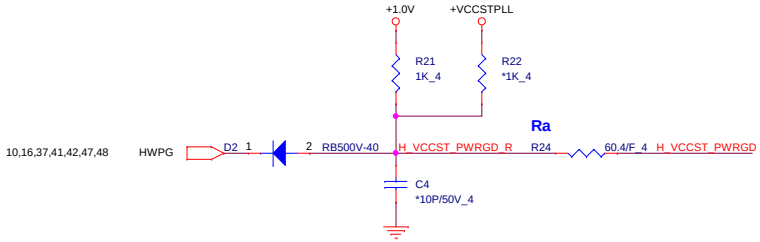


Ra(R10804) Not install in SKL-H



HWPD

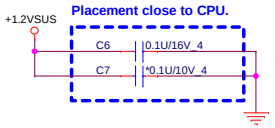
Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



CPU VDDQ

Note: please keep plane is enough for VDDQ 2.8A

Placement close to CPU.



PROJECT : G35
Quanta Computer Inc.

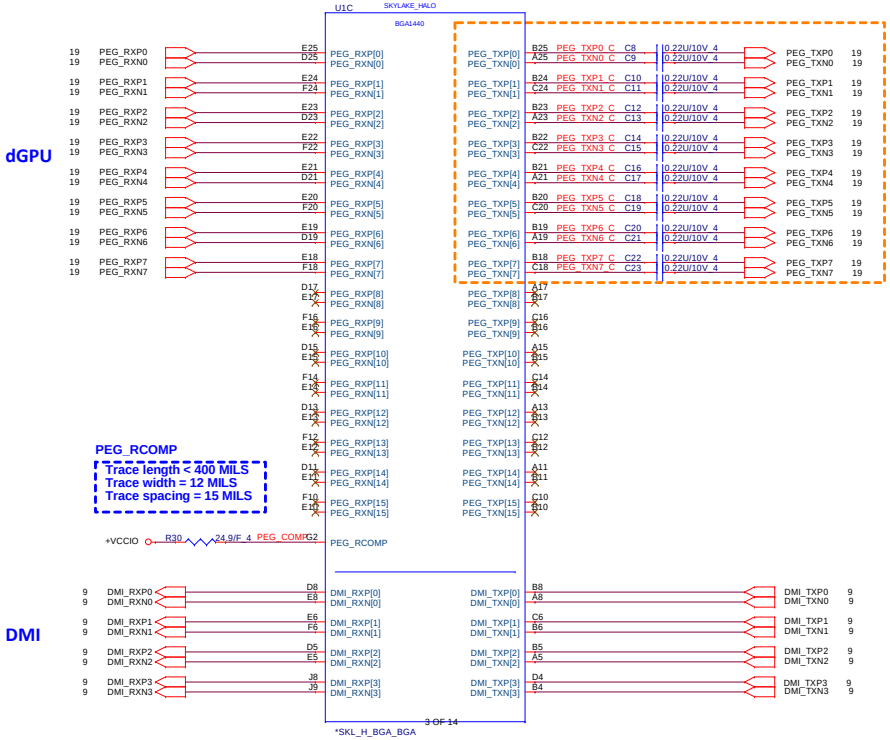
Size	Document Number	Rev
Custom	02 -- SKL 1/7 (JTAG/MISC)	1A

Date: Thursday, December 24, 2015 | Sheet 2 of 51

SKYLAKE Processor (DMI,PEG,FDI)

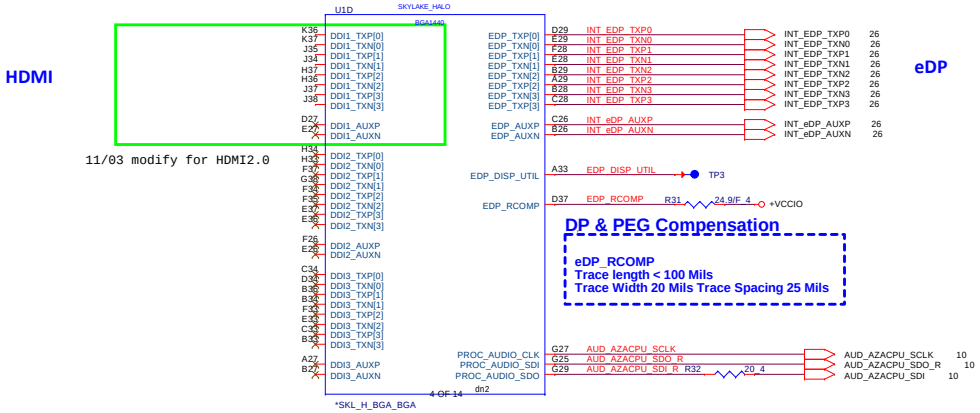
03

DIS : Stuff
UMA: Un-Stuff



PEG_RCOMP

- Trace length < 400 MILS
- Trace width = 12 MILS
- Trace spacing = 15 MILS



11/03 modify for HDMI2.0

DP & PEG Compensation

- eDP_RCOMP
- Trace length < 100 Mils
- Trace Width 20 Mils Trace Spacing 25 Mils

+1.2VSUS 2,6,10,17,18,42,48,51
+3VS5 10,12,14,16,26,33,37,41,42,46,4
+3V 5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,3

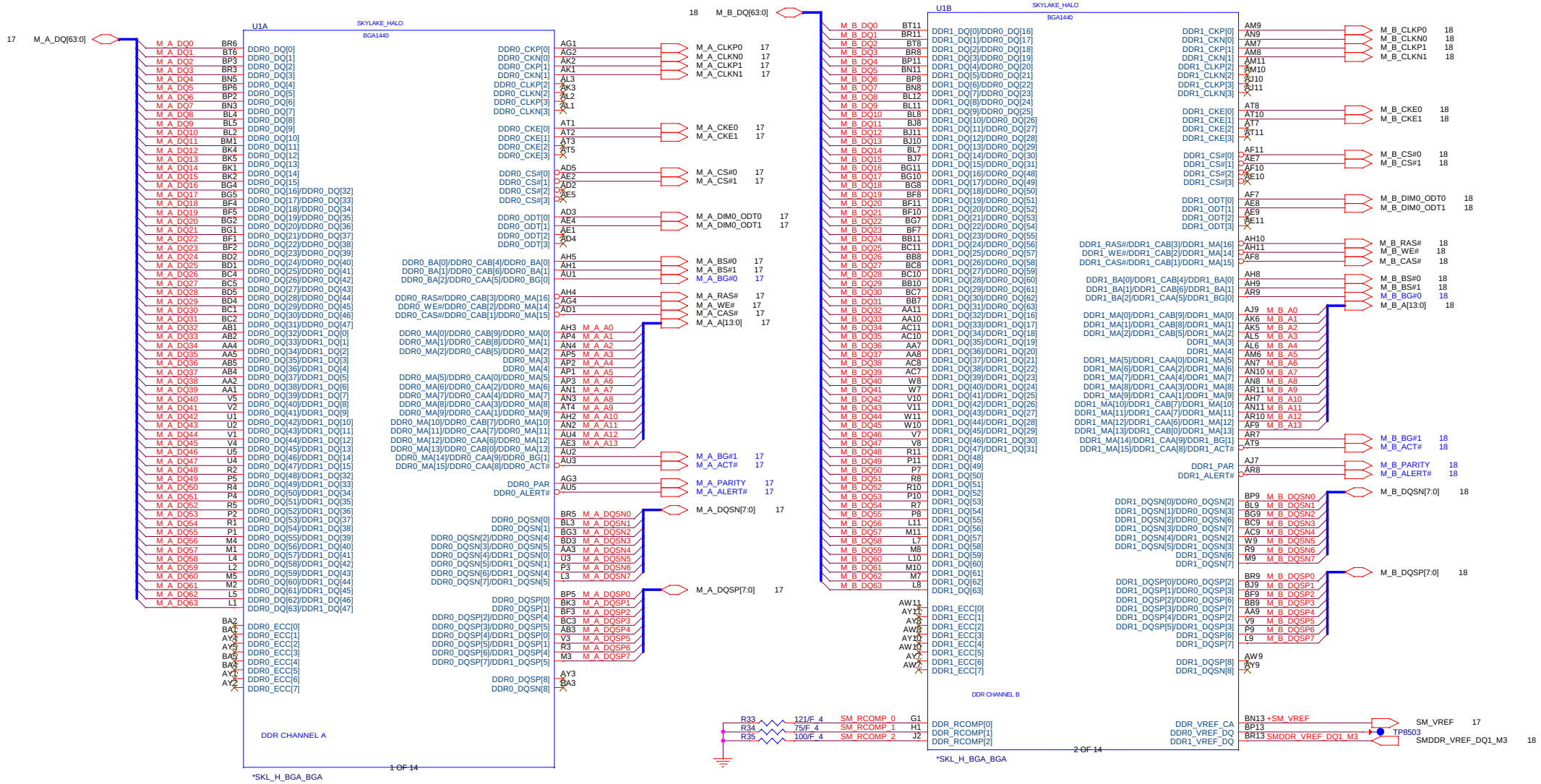
PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	03 – SKL 2/7 (DMI/EDP/PEG)	1A

Date: Thursday, December 24, 2015 | Sheet 3 of 51

SKYLAKE Processor (DDR4)

04



PROJECT : G35

Quanta Computer Inc.

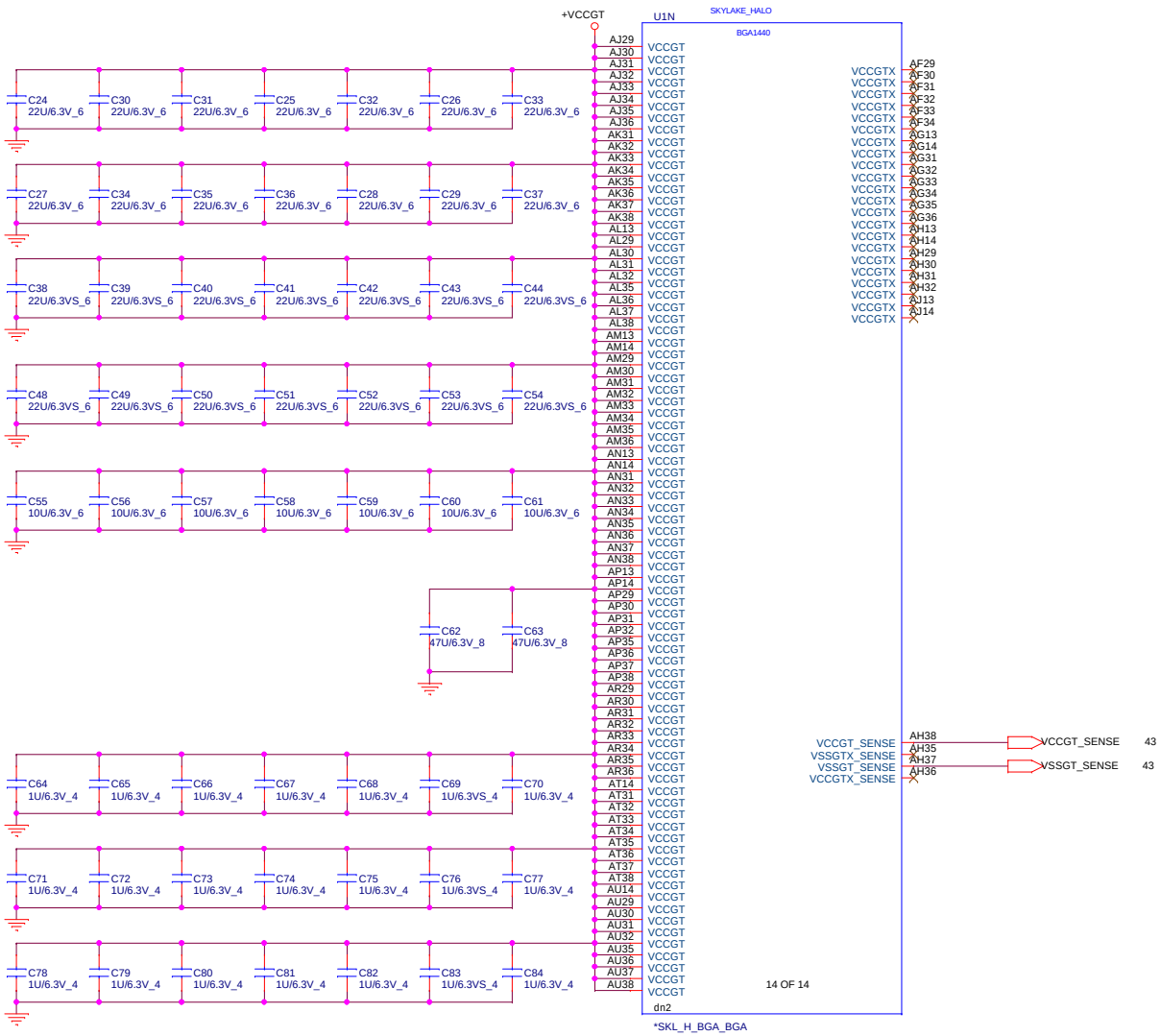
Size	Document Number	Rev
Custom	04 -- SKL 3/7 (DDR4 I/F)	1A

Date: Thursday, December 24, 2015 | Sheet 4 of 51

SKYLAKE Processor (POWER)

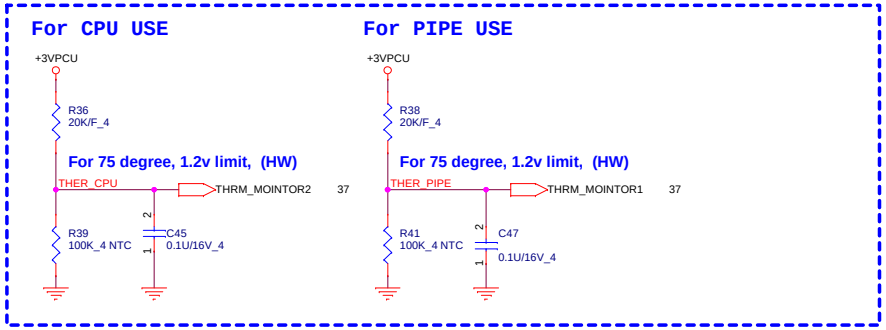
05

Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A



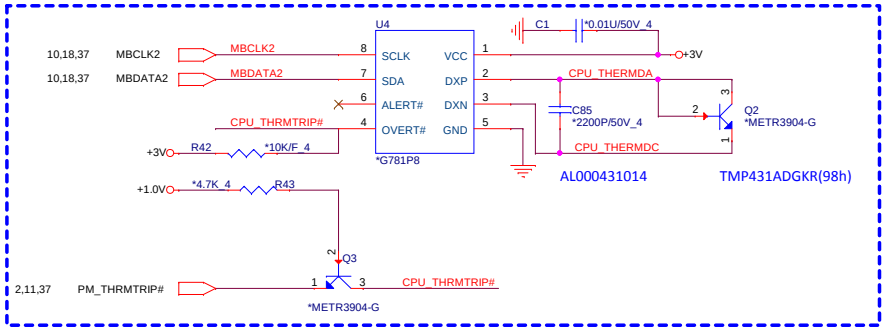
IO Thrm Protect

Location need thermal confirm



CPU Thermal Sensor

Location need thermal confirm

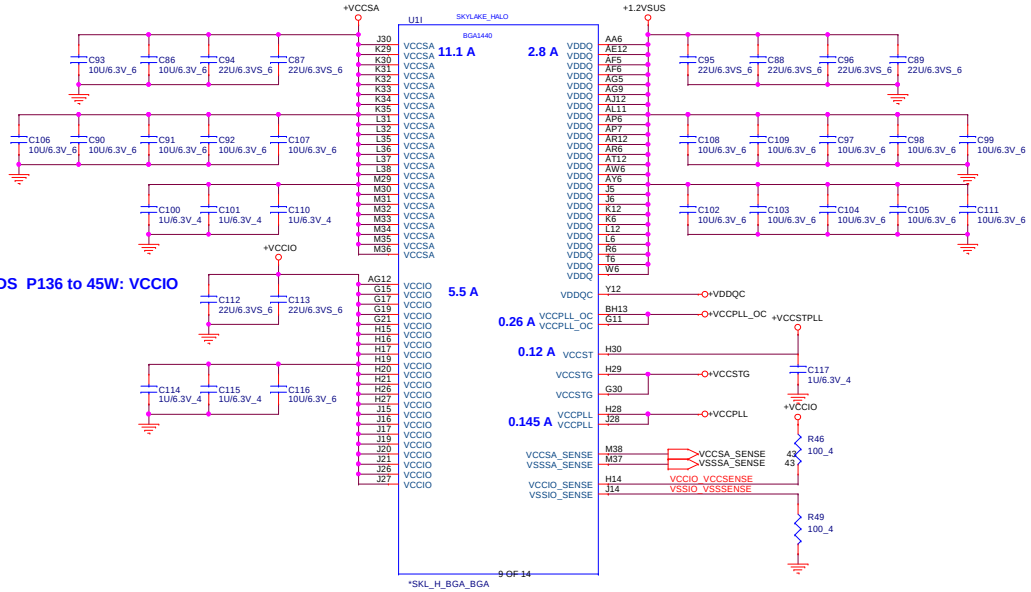


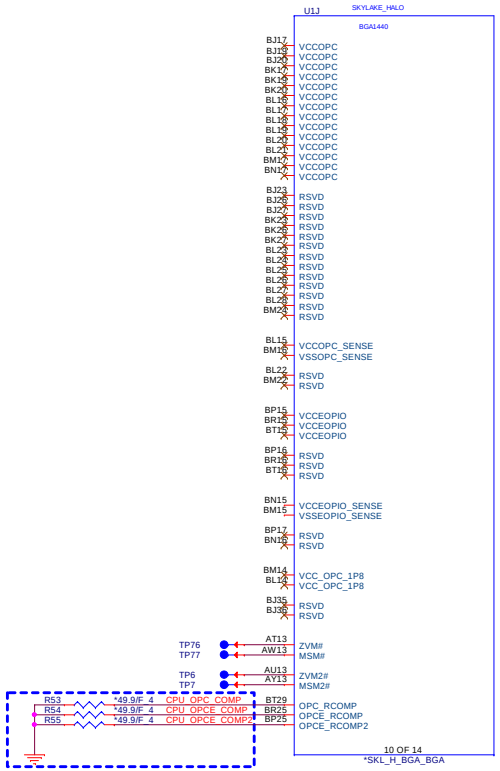
PROJECT : G35 Quanta Computer Inc.		
Size Custom	Document Number 05 -- SKL 4/7 (POWER)	Rev 1A
Date: Thursday, December 24, 2015	Sheet 5 of 51	

Follow SKL H EDS page 135 to 45W(GT2): VCCSA=11.1A

Follow SKL H EDS page 135 45W: VDDQ=2.8A

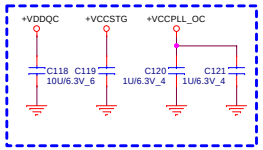
Follow SKL H EDS P136 to 45W: VCCIO
+VCCIO = 0.95V



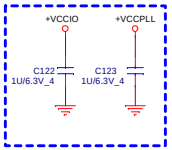


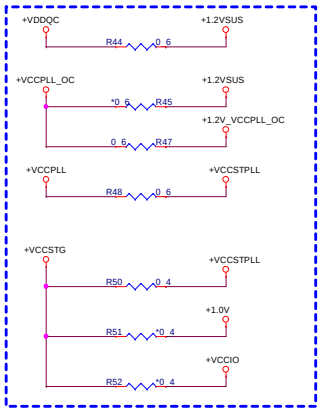
Unconnected for Processors without OPC.

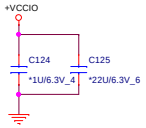
Under CPU



Close CPU



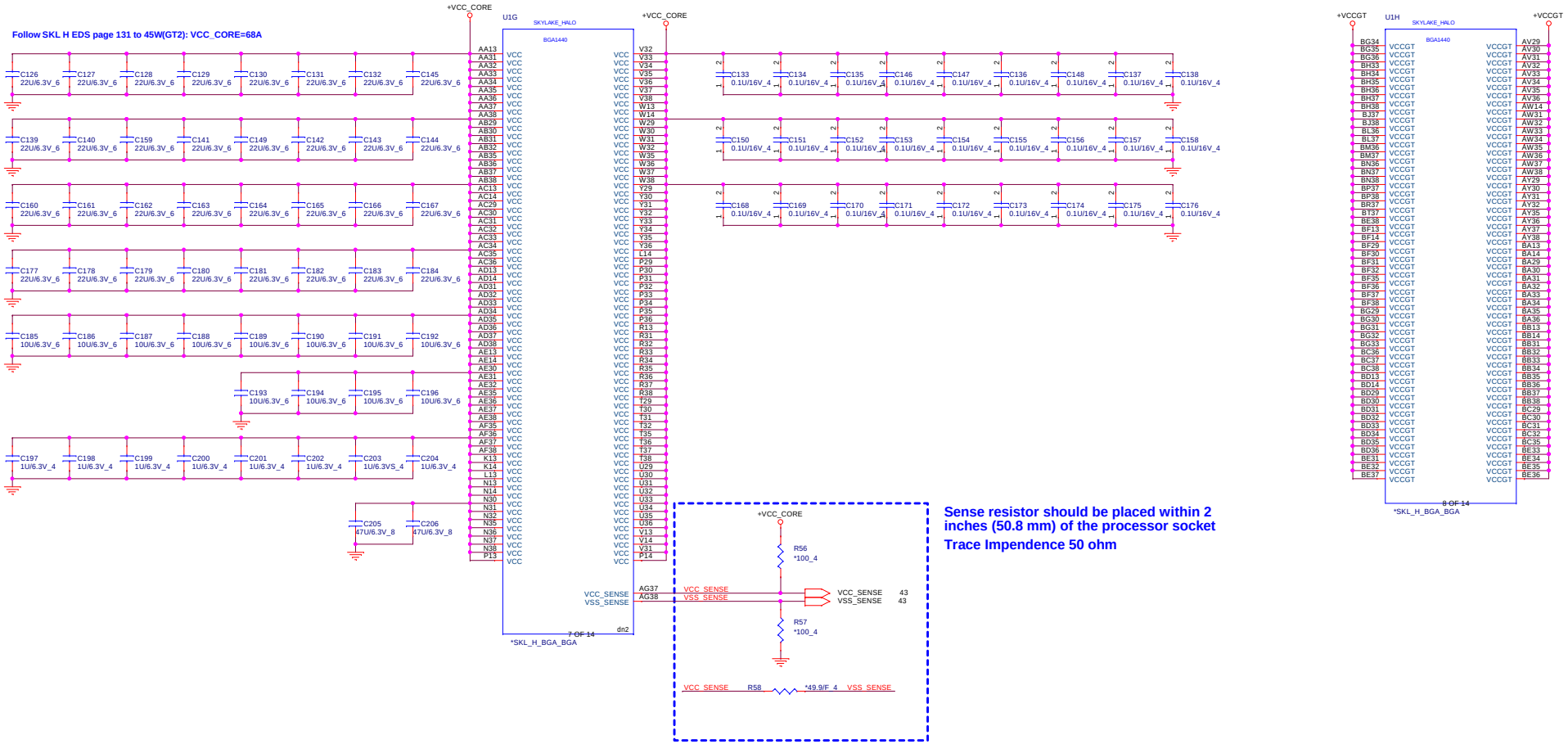




PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	06 -- SKL 5/7 (POWER&GND)	1A

Date: Thursday, December 24, 2015 Sheet 6 of 51



Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket

Trace Impendence 50 ohm

+VCC_CORE 43,44

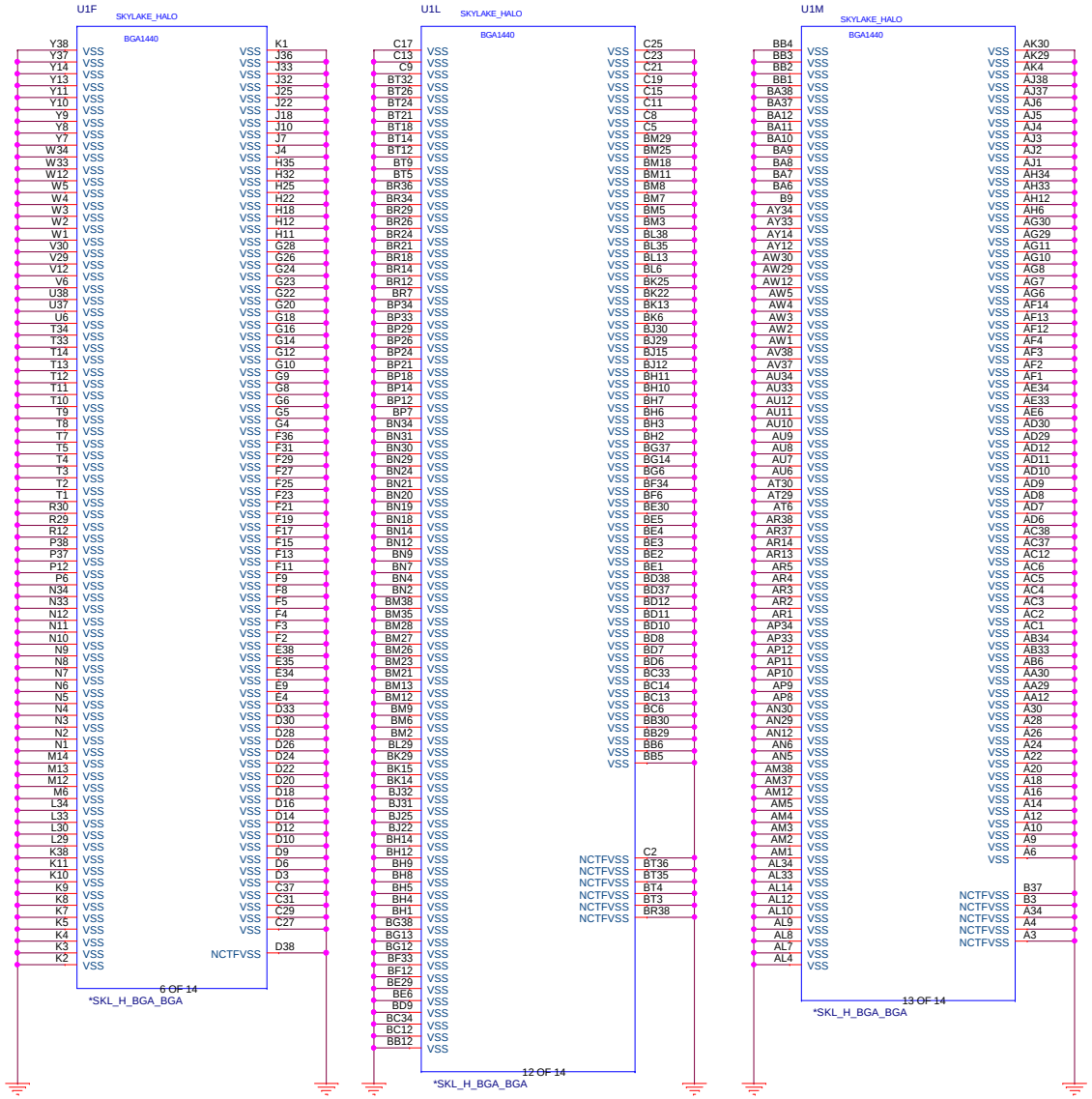
PROJECT : G35

Quanta Computer Inc.

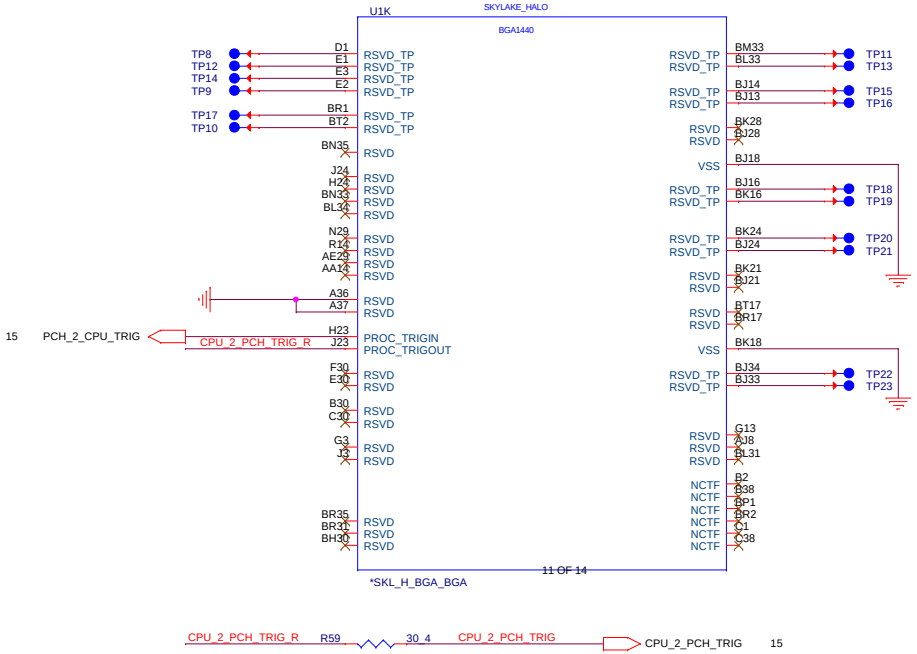
Size	Document Number	Rev
Custom	07 -- SKL 6/7 (POWER&GND)	1A

Date: Thursday, December 24, 2015 | Sheet 7 of 51

SKL-HProcessor (GND)



SKL-H Processor (RESERVED, CFG)

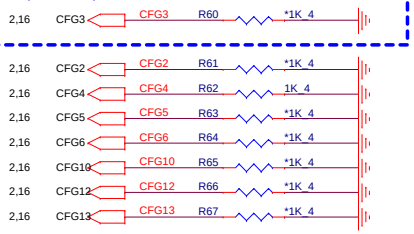


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

0 Enable; SET DFX ENABLED BIT IN DEBUG

1 , Disable;

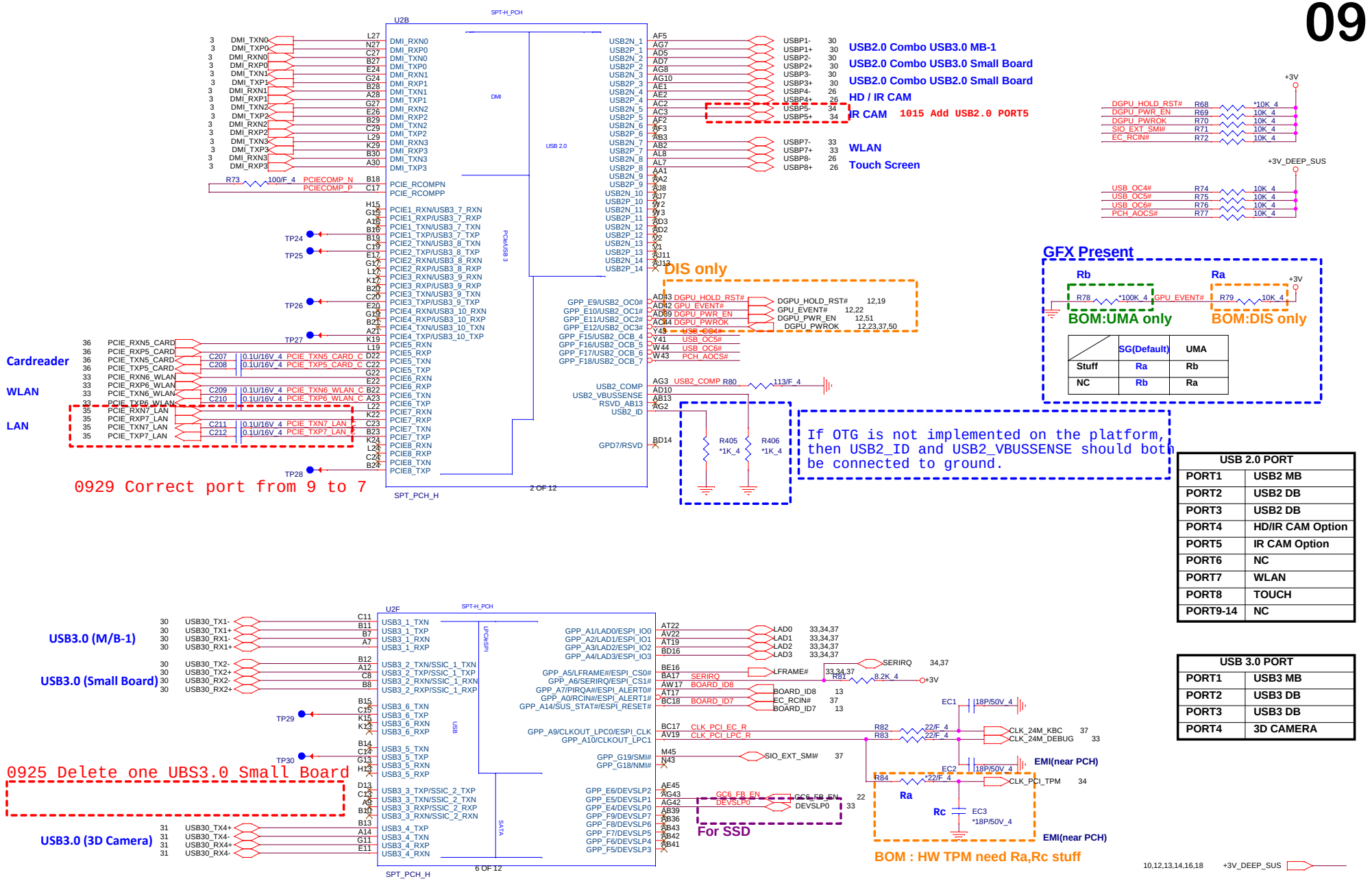


PROJECT : G35

Quanta Computer Inc.

Size	Document Number	Rev
Custom	08 -- SKL 7/7 (GND)	1A

Date: Thursday, December 24, 2015 | Sheet 8 of 51



	SG(Default)	UMA
Stuff	Ra	Rb
NC	Rb	Ra

USB 2.0 PORT	
PORT1	USB2 MB
PORT2	USB2 DB
PORT3	USB2 DB
PORT4	HD/IR CAM Option
PORT5	IR CAM Option
PORT6	NC
PORT7	WLAN
PORT8	TOUCH
PORT9-14	NC

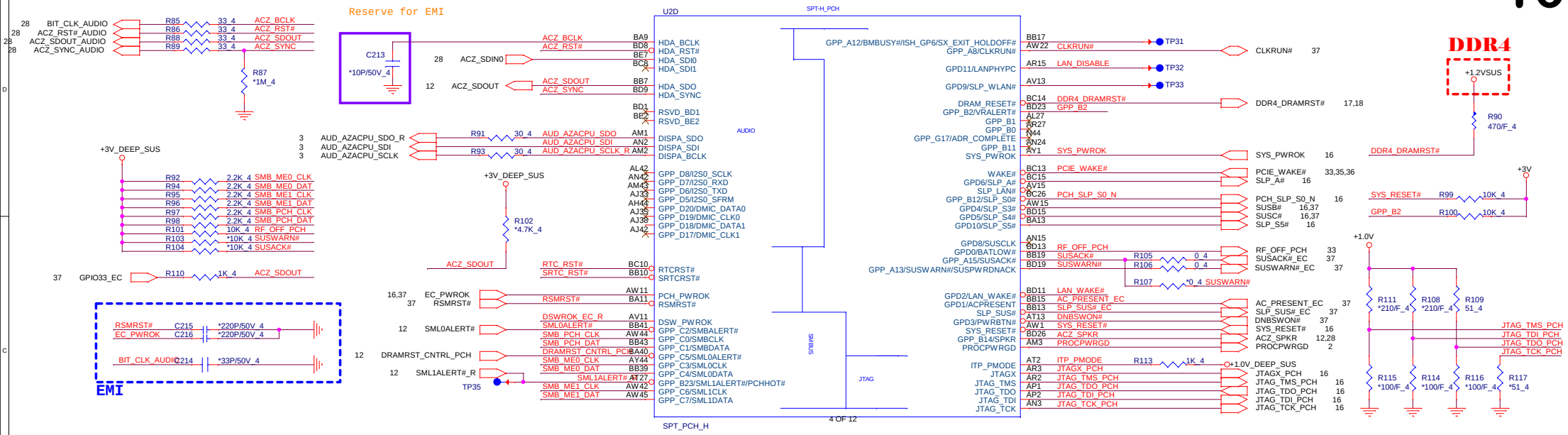
USB 3.0 PORT	
PORT1	USB3 MB
PORT2	USB3 DB
PORT3	USB3 DB
PORT4	3D CAMERA

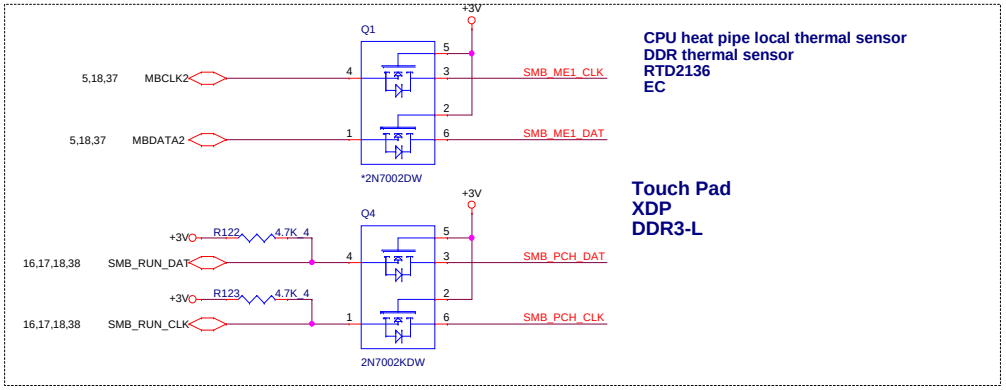
PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	09 -- PCH 1/7 (DMI/USB/PCIE)	1A

Date: Thursday, December 24, 2015 | Sheet 9 of 51

HDA Bus(CLG)

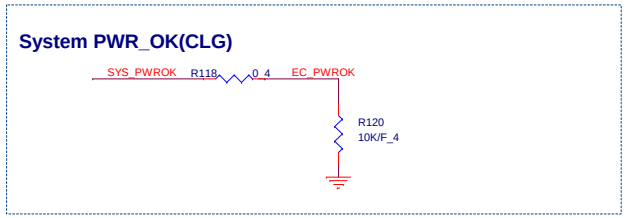




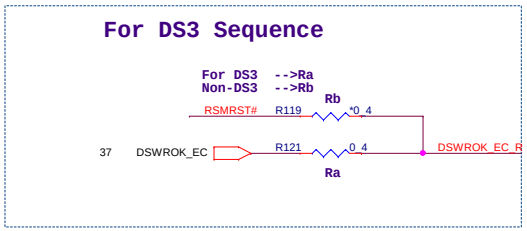
CPU heat pipe local thermal sensor
DDR thermal sensor
RTD2136
EC

Touch Pad
XDP
DDR3-L

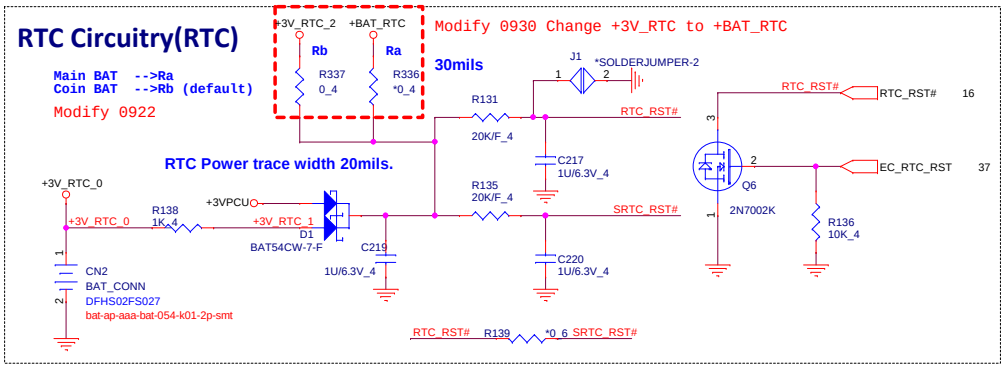
System PWR_OK(CLG)



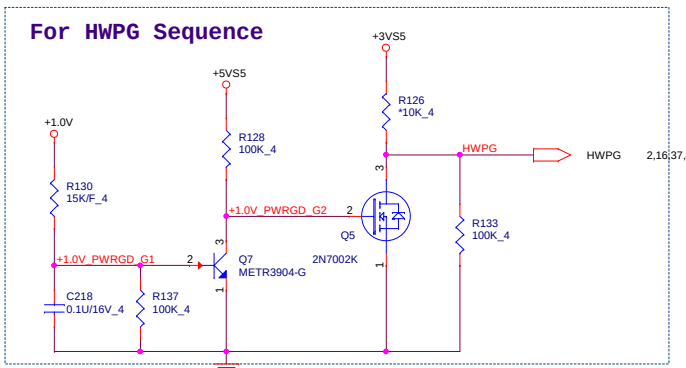
For DS3 Sequence

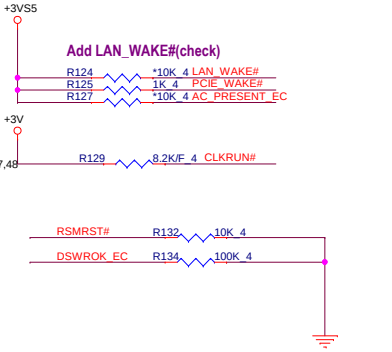


RTC Circuitry(RTC)



For HWPG Sequence





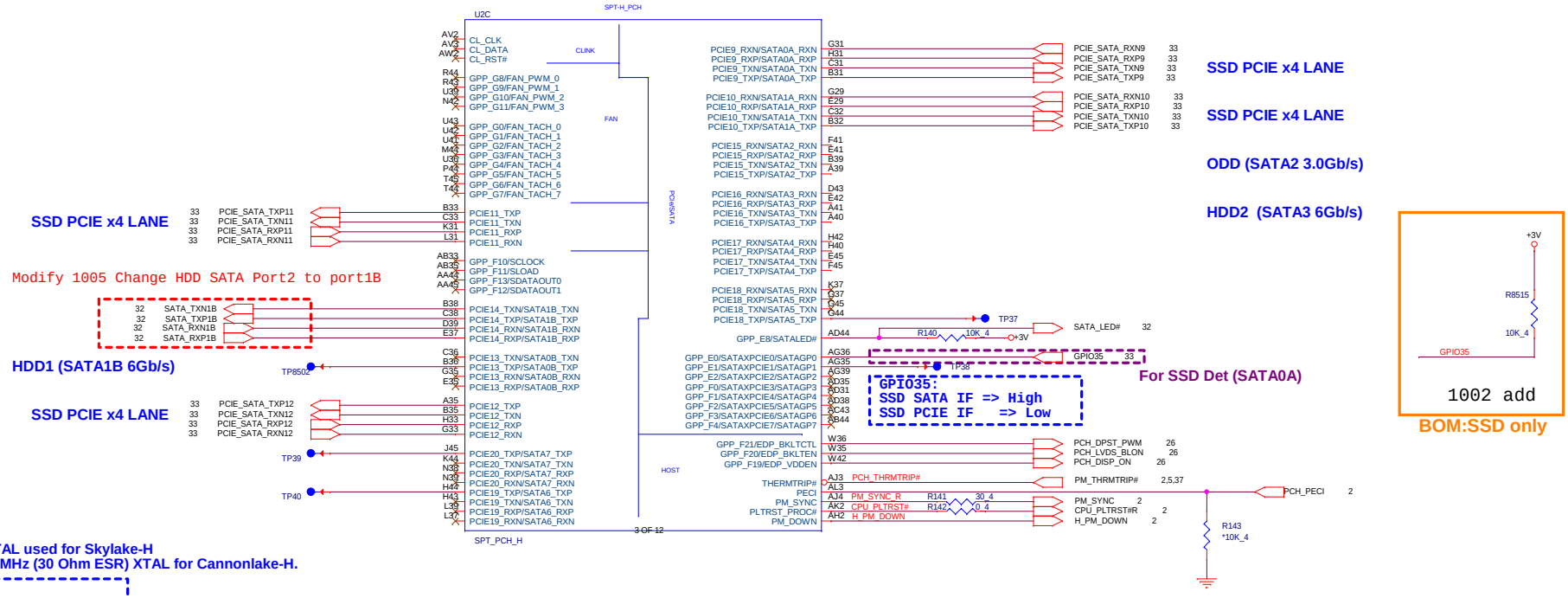
9,12,13,14,16,18 +3V_DEEP_SUS

PROJECT : G35
Quanta Computer Inc.

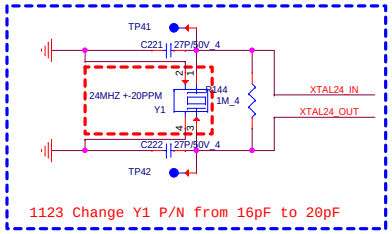
Size	Document Number	Rev
Custom	10 -- PCH 2/7 (HDA/SMBUS)	1A

Date: Thursday, December 24, 2015 Sheet 10 of 51

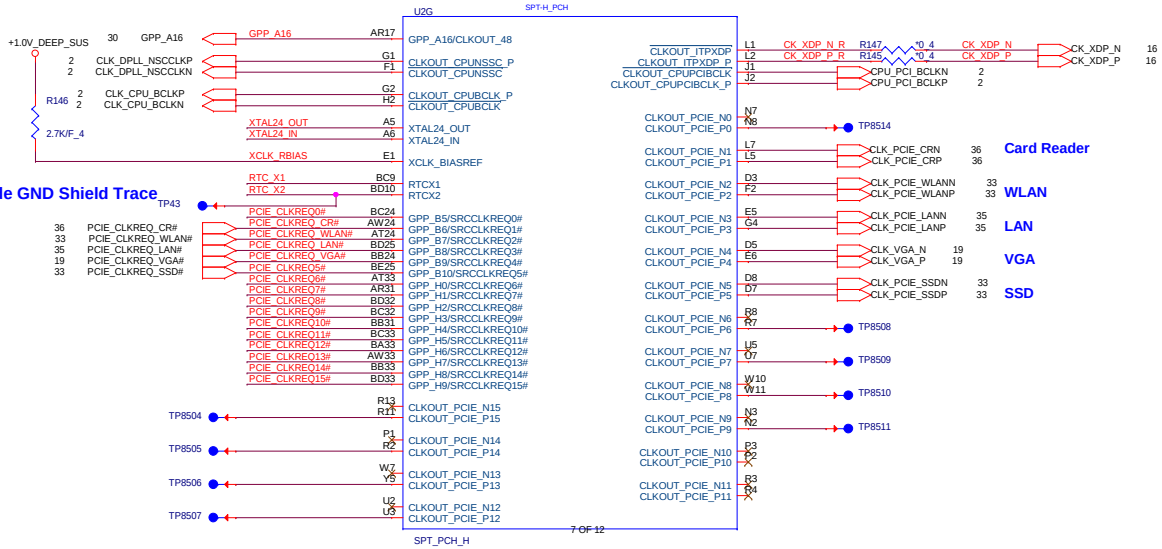
HSIO MUX PORT	
PCIE1-4	NC
PCIE5	Cardreader
PCIE6	Wlan
PCIE7	Lan
PCIE8	NC
PCIE9/SATA0A	SSD PCIE * 4
PCIE10	
PCIE11	
PCIE12	
PCIE13	NC
PCIE14	NC
PCIE15	HDD
PCIE16	NC
PCIE17	NC
PCIE18-20	NC



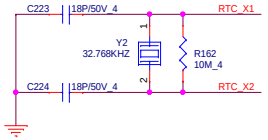
The 24 MHz (50 Ohm ESR) XTAL used for Skylake-H
needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-H.



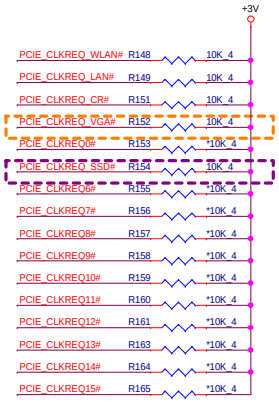
Crystal Components with Surrounding 10 mil Wide GND Shield Trace
Break Out:4-10 mil Wide GND Shield Trace



RTC Clock 32.768KHz



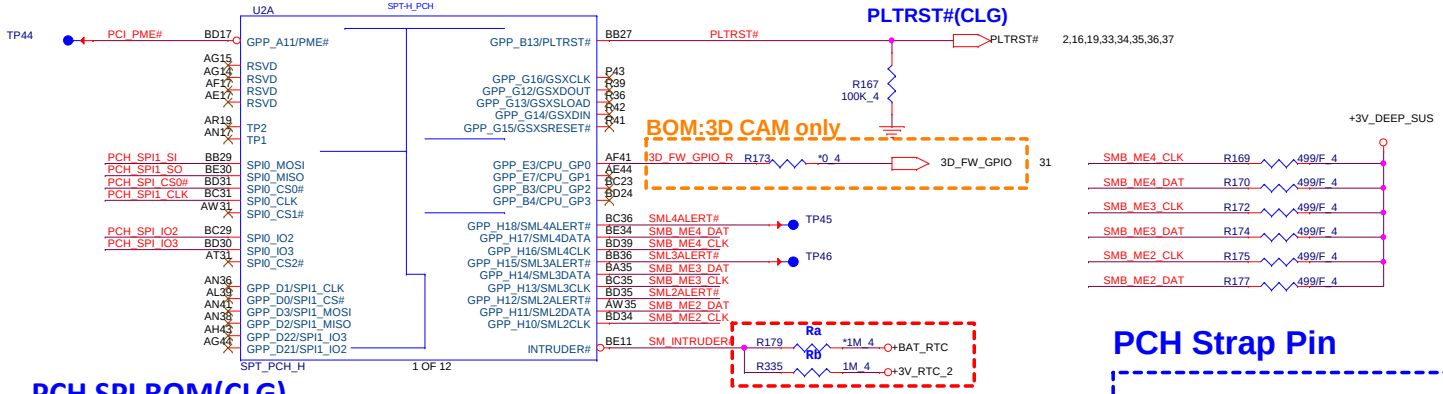
32.768KHz
BG332768453 CRYSTAL SMD 32.768KHZ(+-20PPM,12.5PF)
footprint: xtl-3_2X1_5-2_5-0_8h



PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	11 -- PCH 3/7 (SATA/LPC/CLK)	1A

Date: Thursday, December 24, 2015 | Sheet 11 of 51



PLTRST#(CLG)

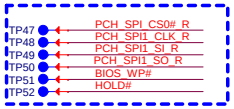
PLTRST# 2,16,19,33,34,35,36,37

BOM:3D CAM only

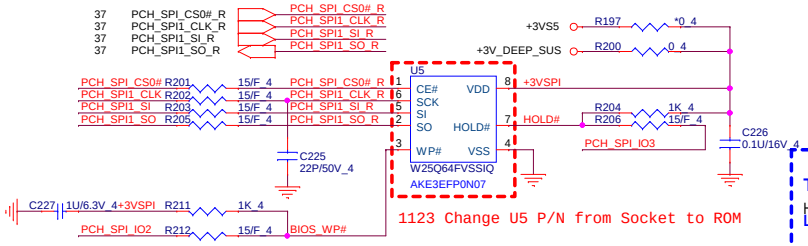
support HW TPM -->Ra
support SW TPM -->Rb (default)

Modify 0930 Change +3V_RTC to +BAT_RTC

PCH SPI ROM(CLG)



Place to TOP



1123 Change U5 P/N from Socket to ROM

Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

PCH Strap Pin

RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

+3V_DEEP_SUS
R166 *20K/F_4
PCH_SPI1_SO
R171 *4.7K_4

ESPI FLASH SHARING MODE

HIGH:SLAVE ATTACEHD FLASH SHARING
LOW: 0: MASTER ATTACHED FLASH SHARING
This strap should sample LOW.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

+3V_DEEP_SUS
R168 *4.7K_4
SML2ALERT#
R176 *20K/F_4

BOOT SELECT STRAP

HIGH:LPC
LOW: SPI. (Default)

+3V_DEEP_SUS
R184 *4.7K_4
13 S_GPIO
R186 *20K/F_4

RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

+3V_DEEP_SUS
R208 *20K/F_4
PCH_SPI1_SI
R214 *4.7K_4

DFX TEST MODE QUALIFIER FOR OTHER DFX STRAP WHEN SAMPLED LOW

+3V_DEEP_SUS
R180 *1K_4
15 PGDMON
R182 *1K_4

DFX TEST MODE

XTAL INPUT IS SINGLE ENDED IF SAMPLED LOW ELSE DIFFERENTIAL

+3V_DEEP_SUS
R188 *10K_4
9,23,37,50 DGPU_PWROK
R190 *10K_4

TOP SWAP OVERRIDE STRAP

HIGH:TOP SWAP ENABLED (CRB)
LOW:TOP SWAP DISABLED(DEFAULT)

+3V
R183 *150K/F_4
10,28 ACZ_SPKR
R185 *20K/F_4

TLS CONFIDENTIALITY ENABLED

HIGH: Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.(CRB)
LOW: security measures defined in the Flash Descriptor. (Default)

+3V_DEEP_SUS
R210 *1K_4
10 ACZ_SDOUT
R215 1K_4

RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

+3V_DEEP_SUS
R187 *20K/F_4
PCH_SPI_IO2
R189 *4.7K_4

RING OSCILLATOR BYPASS

9,19 DGPU_HOLD_RST#
R194 100K_4

XTAL INPUT FREQUENCY[0]

9,22 GPU_EVENT#
R199 *10K_4

XTAL INPUT FREQUENCY[1]

9,51 DGPU_PWR_EN
R209 *10K_4

RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

+3V_DEEP_SUS
R193 *20K/F_4
PCH_SPI_IO3
R198 *100_4

NO REBOOT IF SAMPLED HIGH

HIGH:TOP SWAP ENABLED (CRB)
LOW: Disable "No Reboot" mode. (Default)

+3V
R191 4.7K_4
13 BBS_BIT1
R195 *20K/F_4

ESPI/LPC SELECT STRAP

HIGH:eSPI Is selected for EC.
LOW: LPC Is selected for EC. (Default)

+3V_DEEP_SUS
R192 *4.7K_4
10 DRAMRST_CNTRL_PCH
R196 4.7K_4

TLS CONFIDENTIALITY ENABLED

HIGH:T Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). (CRB)
LOW: Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)

+3V_DEEP_SUS
R207 4.7K_4
10 SML0ALERT#
R213 *20K/F_4

RESERVED

This strap should sample LOW.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

+3V_DEEP_SUS
R178 *4.7K_4
10 SML1ALERT#_R
R181 *20K/F_4

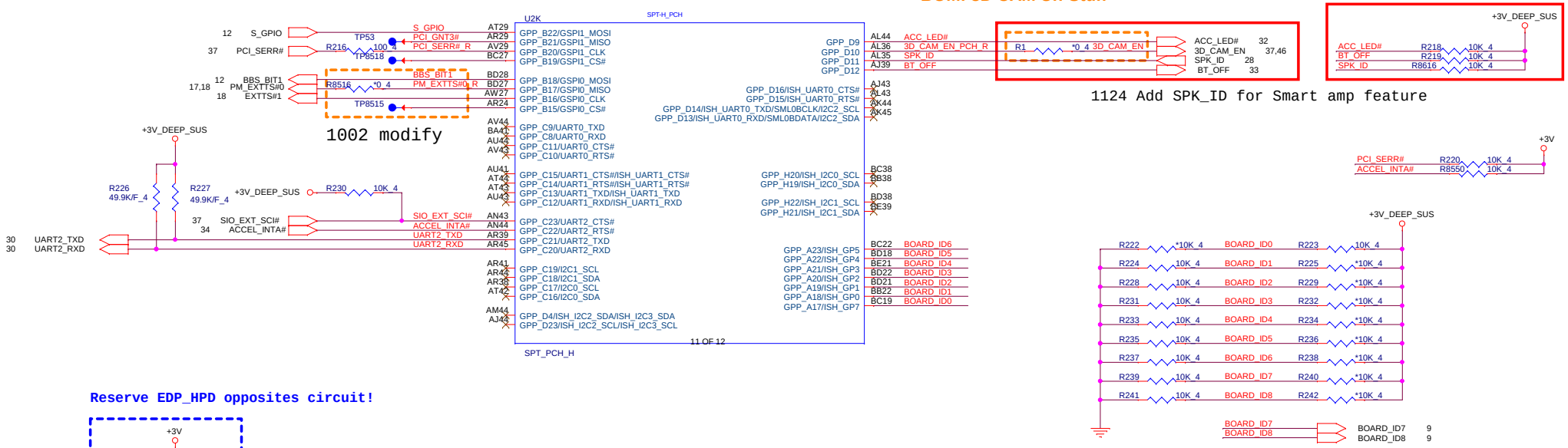
PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	12 -- PCH 4/7 (GPIO/MISC)	1A

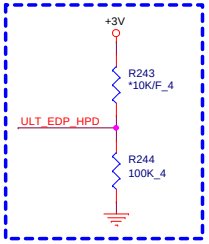
Date: Thursday, December 24, 2015 Sheet 12 of 51

9,10,12,14,16,18 +3V_DEEP_SUS

3D CAMERA
BOM: 3D CAM Un-Stuff

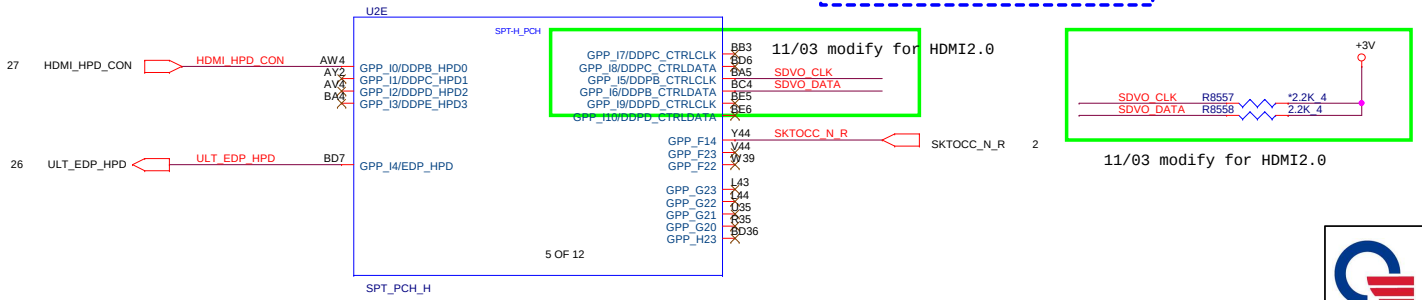


Reserve EDP_HPD opposites circuit!



Model	BOARD_ID[8:7] ID8;ID7	BOARD_ID[6:5] ID6;ID5	Board ID [4:3] ID4;ID3	BOARD_ID[2:1] ID2;ID1	BOARD_ID0 ID0
Definition	00 Non 3D SKU 01 3D SKU	00 Reserve	00 Reserve	00 15" 01 17" 10 17" SP	0 : UMA 1 : DIS

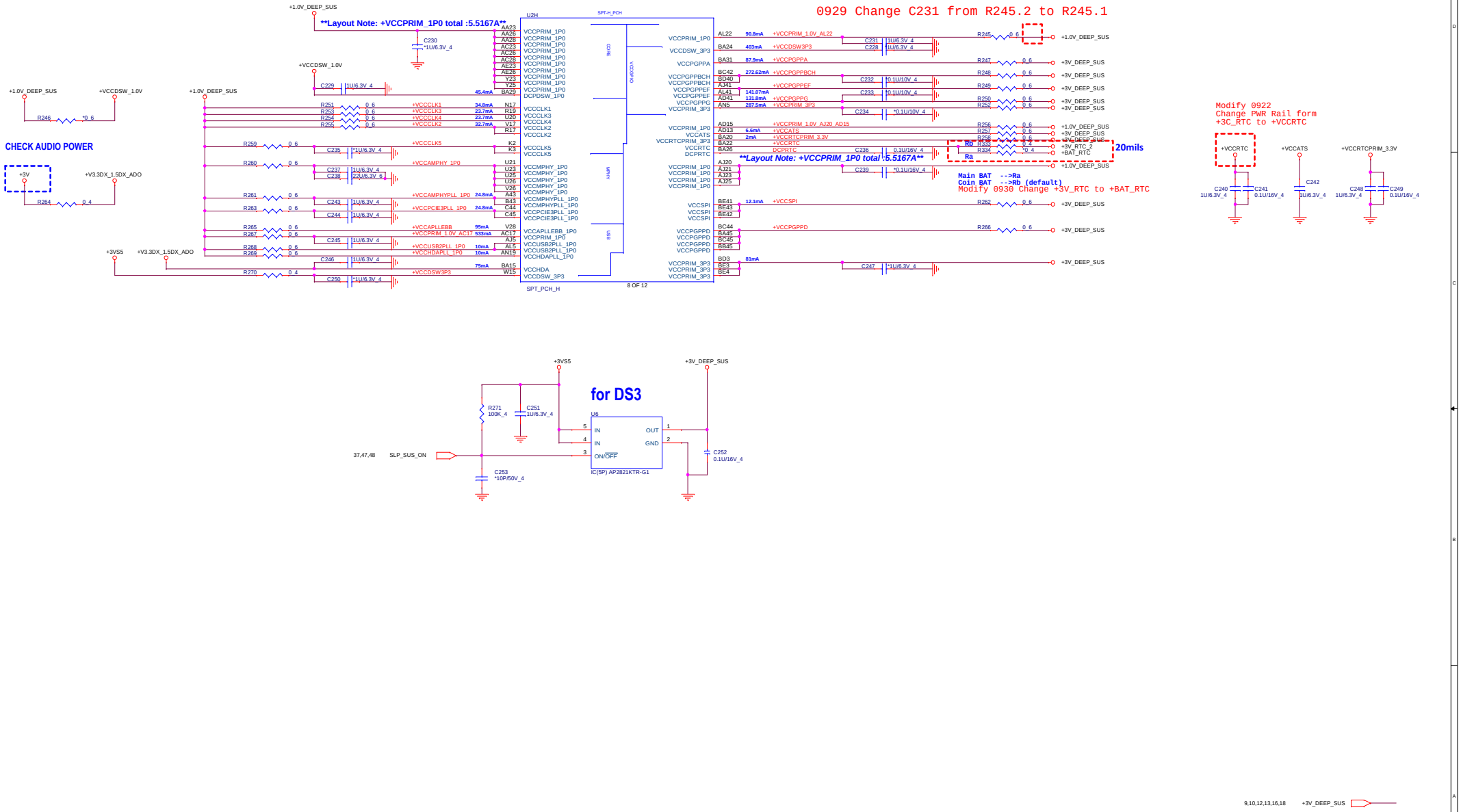
This signal has a weak internal pull-down.
0 = Port C and D is not detected.
1 = Port C and D is detected.



PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	13 -- PCH 5/7 (GPIO)	1A

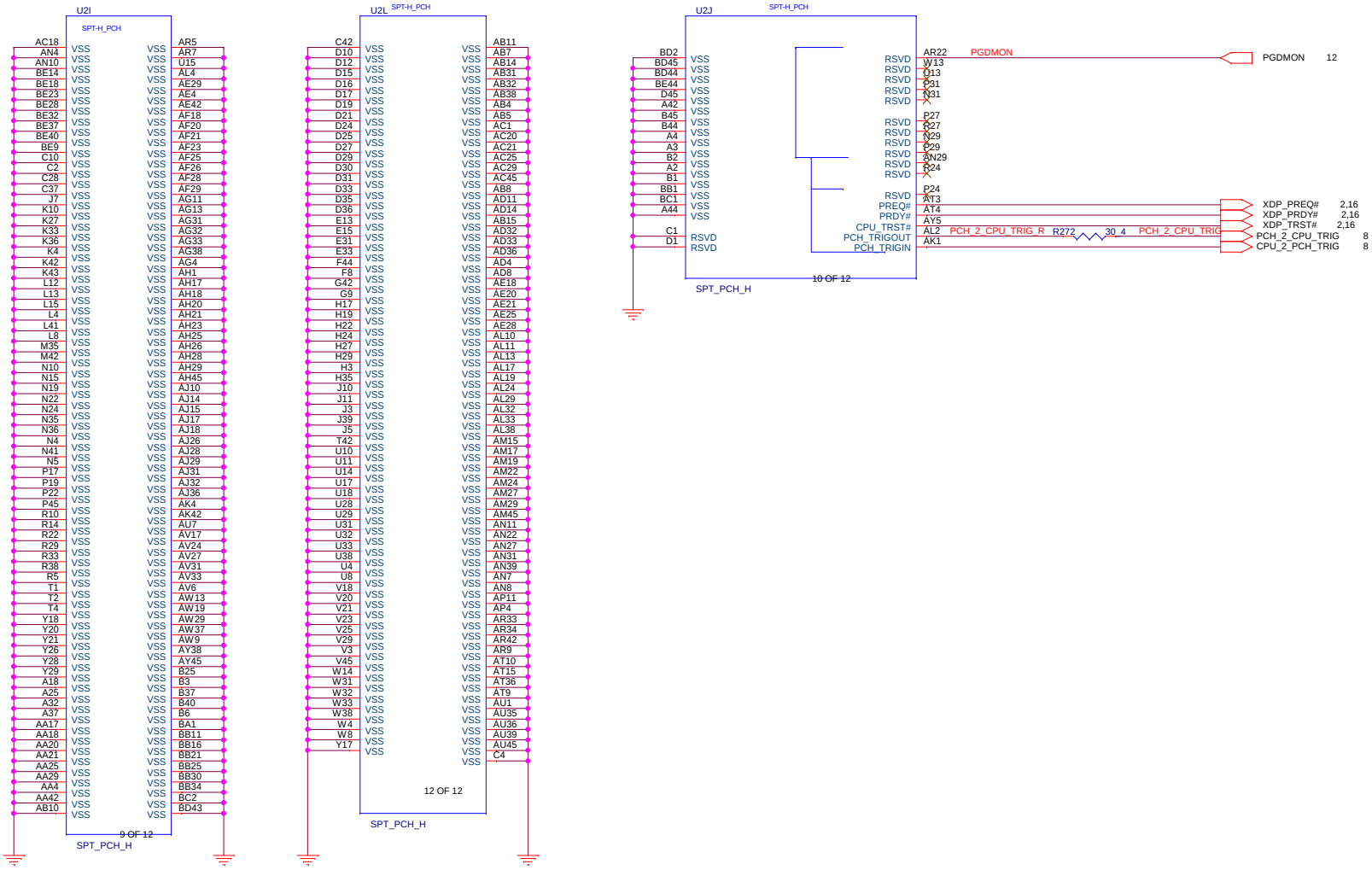
Date: Thursday, December 24, 2015 Sheet 13 of 51



PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	14 -- PCH 6/7 (POWER)	1A

Date: Thursday, December 24, 2015 Sheet 14 of 51

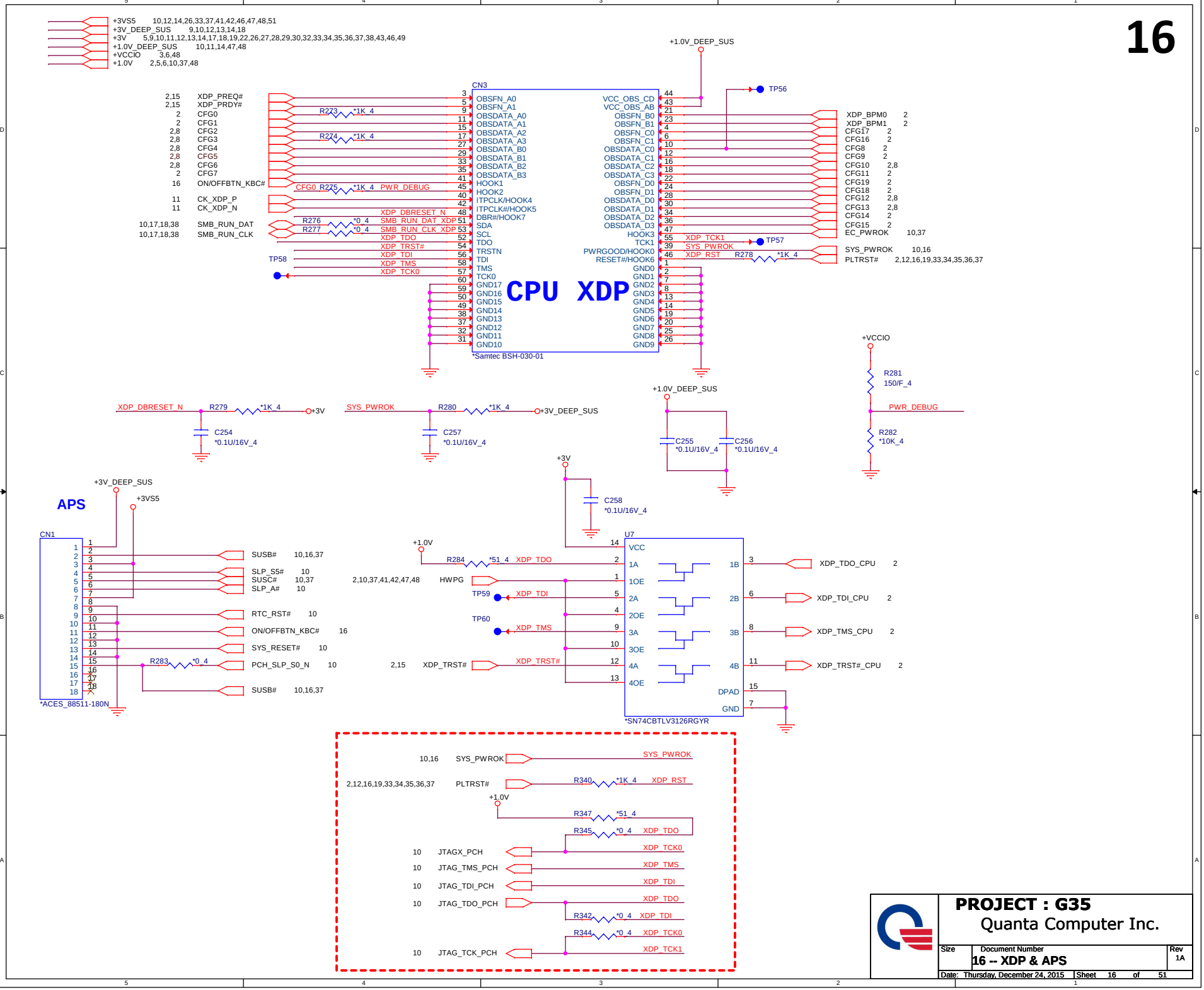


PROJECT : G35

Quanta Computer Inc.

Size	Document Number	Rev
Custom	15 -- PCH 7/7 (GND)	1A

Date: Thursday, December 24, 2015 | Sheet 15 of 51

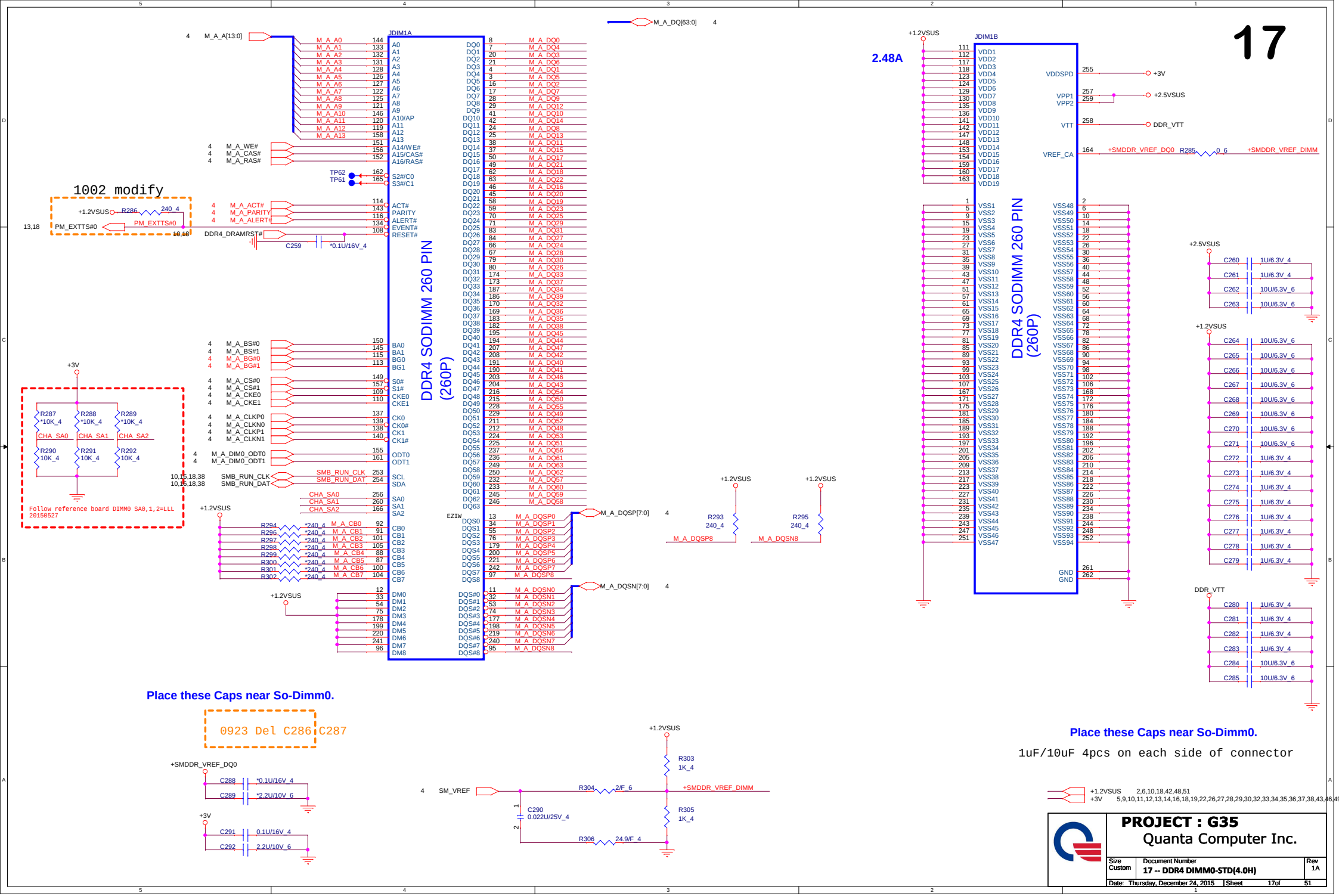


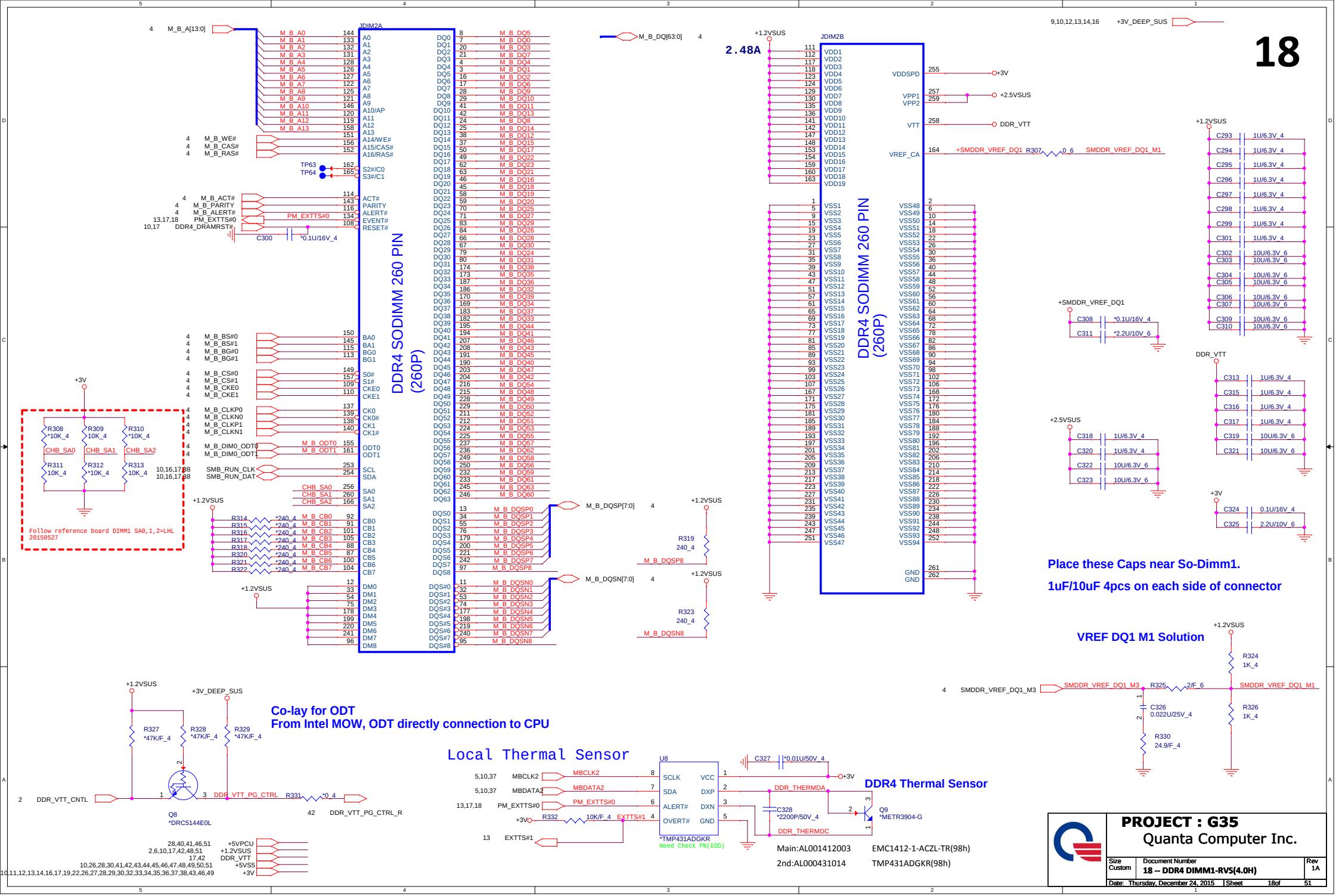
PROJECT : G35

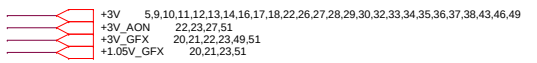
Quanta Computer Inc.

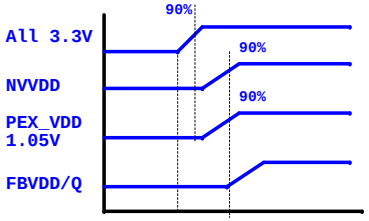
Size	Document Number	Rev
	16 -- XDP & APS	1A

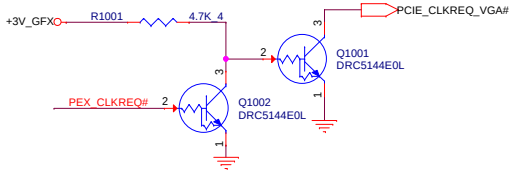
Date: Thursday, December 24, 2015 | Sheet 16 of 51

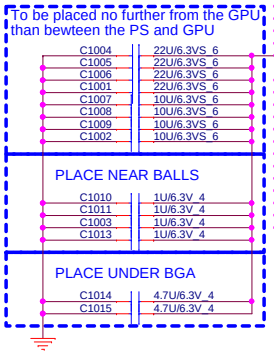

JDIM1A
DDR4 SODIMM 260 PIN (260P)
M_A_A[13:0]
M_A_DQ[63:0]
M_A_DQSP[7:0]
M_A_DQSN[7:0]
M_A_WE#
M_A_CAS#
M_A_RAS#
M_A_ACT#
M_A_PARITY
M_A_ALERT#
DDR4_DRAMRST#
PM_EXTTS#0
1002 modify
+1.2VSUS
+3V
M_A_BS#0
M_A_BS#1
M_A_BG#0
M_A_BG#1
M_A_CS#0
M_A_CS#1
M_A_CKE0
M_A_CKE1
M_A_CLKP0
M_A_CLKN0
M_A_CLKP1
M_A_CLKN1
M_A_DIM0_ODT0
M_A_DIM0_ODT1
SMB_RUN_CLK
SMB_RUN_DAT
CHA_SA0
CHA_SA1
CHA_SA2
Follow reference board DIMM0 SA0,1,2=LLL 20150527
Place these Caps near So-Dimm0.
0923 Del C286 C287
+SMDDR_VREF_DQ0
SM_VREF
+SMDDR_VREF_DIMM
JDIM1B
2.48A
DDR4 SODIMM 260 PIN (260P)
VDDSPD
VPP1
VPP2
VTT
VREF_CA
+2.5VSUS
DDR_VTT
Place these Caps near So-Dimm0.
1uF/10uF 4pcs on each side of connector
+1.2VSUS 2,6,10,18,42,48,51
+3V 5,9,10,11,12,13,14,16,18,19,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,49
PROJECT : G35
Quanta Computer Inc.
Size Custom
Document Number
17 -- DDR4 DIMM0-STD(4.0H)
Rev 1A
Date: Thursday, December 24, 2015
Sheet 17of 51

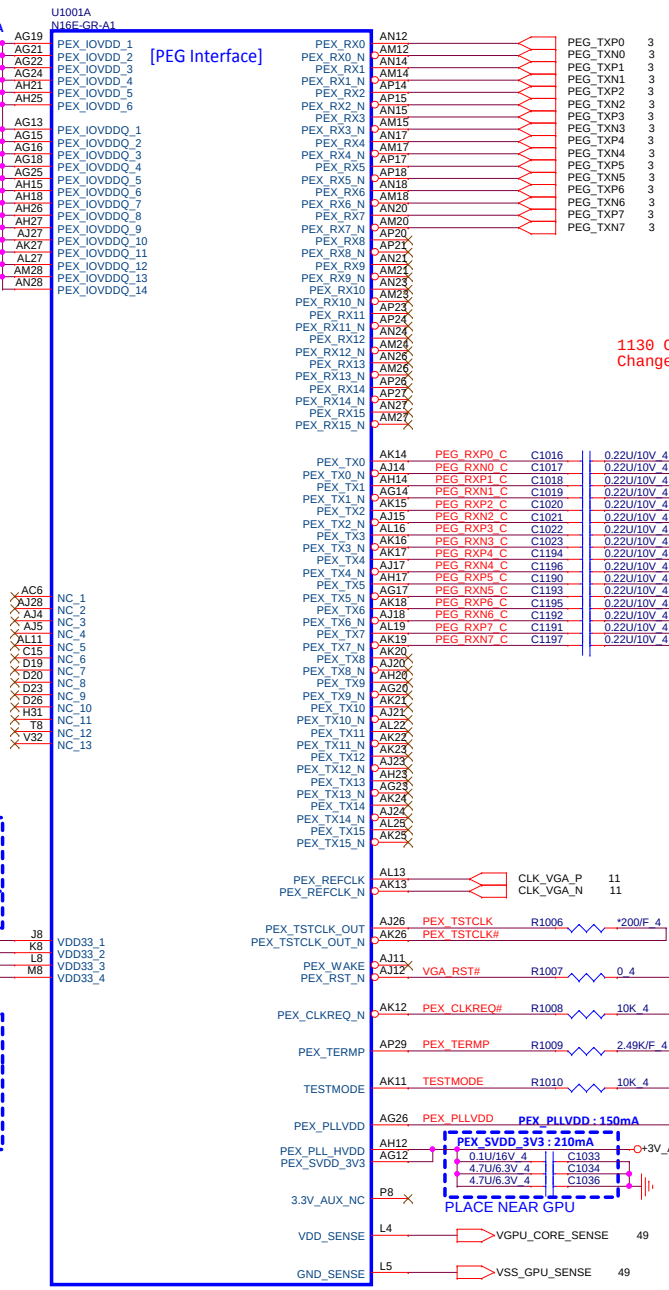

JDIM2A
DDR4 SODIMM 260 PIN (260P)
M_B_A[13:0]
M_B_DQ[63:0]
M_B_DQSP[7:0]
M_B_DQSN[7:0]
M_B_WE#
M_B_CAS#
M_B_RAS#
M_B_ACT#
M_B_PARITY
M_B_ALERT#
PM_EXTTS#0
DDR4_DRAMRST#
C300
*0.1U/16V_4
M_B_BS#0
M_B_BS#1
M_B_BG#0
M_B_BG#1
M_B_CS#0
M_B_CS#1
M_B_CKE0
M_B_CKE1
M_B_CLKP0
M_B_CLKN0
M_B_CLKP1
M_B_CLKN1
M_B_DIM0_ODT0
M_B_DIM0_ODT1
SMB_RUN_CLK
SMB_RUN_DAT
CHB_SA0
CHB_SA1
CHB_SA2
+3V
R308 *10K_4
R309 10K_4
R310 *10K_4
R311 10K_4
R312 *10K_4
R313 10K_4
Follow reference board DIMM1 SA0,1,2=LHL 20150527
+1.2VSUS
R314 *240_4
R315 *240_4
R316 *240_4
R317 *240_4
R318 *240_4
R320 *240_4
R321 *240_4
R322 *240_4
R319 240_4
R323 240_4
M_B_DQSP8
M_B_DQSN8
JDIM2B
DDR4 SODIMM 260 PIN (260P)
2.48A
VDDSPD
+3V
VPP1
VPP2
+2.5VSUS
VTT
DDR_VTT
VREF_CA
+SMDDR_VREF_DQ1
R307 0_6
SMDDR_VREF_DQ1_M1
9,10,12,13,14,16
+3V_DEEP_SUS
+SMDDR_VREF_DQ1
C308 *0.1U/16V_4
C311 *2.2U/10V_6
C293 1U/6.3V_4
C294 1U/6.3V_4
C295 1U/6.3V_4
C296 1U/6.3V_4
C297 1U/6.3V_4
C298 1U/6.3V_4
C299 1U/6.3V_4
C301 1U/6.3V_4
C302 10U/6.3V_6
C303 10U/6.3V_6
C304 10U/6.3V_6
C305 10U/6.3V_6
C306 10U/6.3V_6
C307 10U/6.3V_6
C309 10U/6.3V_6
C310 10U/6.3V_6
C313 1U/6.3V_4
C315 1U/6.3V_4
C316 1U/6.3V_4
C317 1U/6.3V_4
C319 10U/6.3V_6
C321 10U/6.3V_6
C318 1U/6.3V_4
C320 1U/6.3V_4
C322 10U/6.3V_6
C323 10U/6.3V_6
C324 0.1U/16V_4
C325 2.2U/10V_6
Place these Caps near So-Dimm1.
1uF/10uF 4pcs on each side of connector
VREF DQ1 M1 Solution
SMDDR_VREF_DQ1_M3
R325 2/F_6
R324 1K_4
R326 1K_4
C326 0.022U/25V_4
R330 24.9/F_4
Co-lay for ODT
From Intel MOW, ODT directly connection to CPU
R327 *47K/F_4
R328 *47K/F_4
R329 *47K/F_4
DDR_VTT_CNTL
DDR_VTT_PG_CTRL
R331 *0_4
DDR_VTT_PG_CTRL_R
Q8 *DRC5144E0L
Local Thermal Sensor
U8
MBCLK2
MBDATA2
PM_EXTTS#0
EXTTS#1
R332 10K/F_4
SCLK
SDA
ALERT#
OVERT#
VCC
DXP
DXN
GND
*TMP431ADGKR
Need Check PN(EOD)
C327 *0.01U/50V_4
DDR_THERMDA
DDR_THERMDC
C328 *2200P/50V_4
Q9 *METR3904-G
DDR4 Thermal Sensor
+5VPCU
+1.2VSUS
DDR_VTT
+5VS5
+3V
Main:AL001412003
2nd:AL000431014
EMC1412-1-ACZL-TR(98h)
TMP431ADGKR(98h)
PROJECT : G35
Quanta Computer Inc.
Size Custom
Document Number
18 -- DDR4 DIMM1-RVS(4.0H)
Rev 1A
Date: Thursday, December 24, 2015
Sheet 18of 51

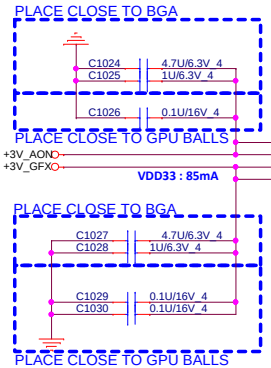






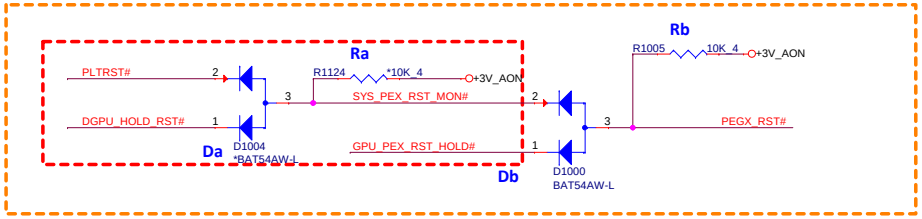


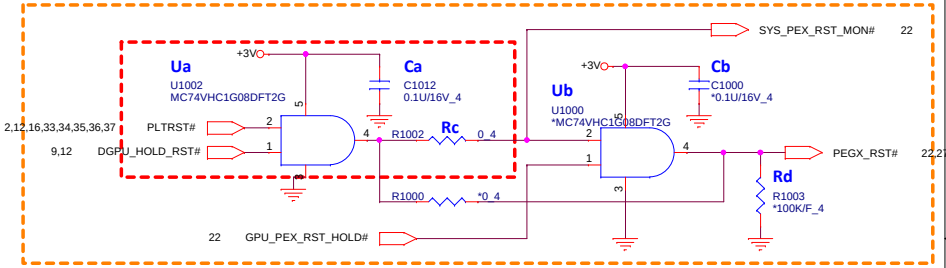




1130 Change D1004,R1124 from I to NI
Change U1002,R1002,C1012 from NI to I

If stuff Da,Db,Ra,Rb, do not stuff Ua,Ub,Ca,Cb,Rc,Rd





GPU type	Part Number	Part Description	Where USed
N16P-GT	AJ0N16P0T05	IC CTRL(908P)N16P-GT-A2(BGA)TOPBSQ	G35A
	AJ0N16P0T06	IC CTRL(908P)N16P-GT-A2(BGA)QBCON	
N16P-GX	AJ0N16P0T14	IC CTRL(908P)N16P-GX-A2(BGA)TOPBSQ	G35A / G37A
	AJ0N16P0T15	IC CTRL(908P)N16P-GX-A2(BGA)QBCON	
N16E-GR	AJ0N16E0T02	IC CTRL(908P)N16E-GR-A1(BGA)TOPBSQ	G35A / G37A
	AJ0N16E0T03	IC CTRL(908P)N16E-GR-A1(BGA)QBCON	

PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N16P-GX/GT - 1/5 (PCIE)	1A

Date: Thursday, December 24, 2015 Sheet 19 of 51

+3V_GFX 19,21,22,23,49,51
+1.35V_GFX 23,24,25,50
+1.05V_GFX 19,21,23,51
NV_PLLVDD 21

U1001B
N16E-GR-A1
[MEMORY I/F A]

U1001C
N16E-GR-A1
MEMORY I/F C

24 FBA_CMD[31:0]
FBA_CMD0 U30
FBA_CMD1 T31
FBA_CMD2 U29
FBA_CMD3 R34
FBA_CMD4 R33
FBA_CMD5 U32
FBA_CMD6 U33
FBA_CMD7 U28
FBA_CMD8 V28
FBA_CMD9 V29
FBA_CMD10 V30
FBA_CMD11 U34
FBA_CMD12 U31
FBA_CMD13 V34
FBA_CMD14 V33
FBA_CMD15 Y32
FBA_CMD16 AA31
FBA_CMD17 AA29
FBA_CMD18 AA28
FBA_CMD19 AC34
FBA_CMD20 AC33
FBA_CMD21 AA32
FBA_CMD22 AA33
FBA_CMD23 Y28
FBA_CMD24 Y29
FBA_CMD25 W31
FBA_CMD26 Y30
FBA_CMD27 AA34
FBA_CMD28 Y31
FBA_CMD29 Y34
FBA_CMD30 Y33
FBA_CMD31 V31

24 FBA_DBI[7:0]
FBA_DBI0 P30
FBA_DBI1 F31
FBA_DBI2 F34
FBA_DBI3 M32
FBA_DBI4 AD31
FBA_DBI5 AL29
FBA_DBI6 AM32
FBA_DBI7 AF34

24 FBA_EDC[7:0]
FBA_EDC0 M31
FBA_EDC1 G31
FBA_EDC2 E33
FBA_EDC3 M33
FBA_EDC4 AE31
FBA_EDC5 AK30
FBA_EDC6 AN33
FBA_EDC7 AF33

GDDR5 NO USE
M30 H30 E34 M34 AF30 AK31 AM34 AF32

+1.35V_GFX
AA27 AA30 AB27 AB33 AC27 AD27 AE27 AF27 AG27 B13 B16 B19 E13 E16 E19 H10 H11 H12 H13 H14 H15 H16 H18 H19 H20 H21 H22 H23 H24 H8 H9 L27 M27 N27 P27 R27 T27 T30 T33 V27 W27 W30 W33 Y27

PLACE CLOSE TO GPU BALLS
C1037 4.7U/6.3V_4
C1038 4.7U/6.3V_4
C1039 4.7U/6.3V_4
C1040 4.7U/6.3V_4
C1041 1U/6.3V_4
C1042 1U/6.3V_4
C1043 1U/6.3V_4
C1044 1U/6.3V_4
C1045 0.1U/16V_4
C1046 0.1U/16V_4
C1047 0.1U/16V_4
C1048 0.1U/16V_4

PLACE CLOSE TO BGA
C1049 10U/6.3V_6
C1050 10U/6.3V_6
C1051 22U/6.3VS_6
C1052 22U/6.3VS_6

MUST BE on GPU ball
C1053 *22U/6.3V_6
C1055 *22U/6.3V_6

FBA_DQ00 L28 VMA_DQ0
FBA_DQ01 M29 VMA_DQ1
FBA_DQ02 L29 VMA_DQ2
FBA_DQ03 M28 VMA_DQ3
FBA_DQ04 N31 VMA_DQ4
FBA_DQ05 P29 VMA_DQ5
FBA_DQ06 R29 VMA_DQ6
FBA_DQ07 P28 VMA_DQ7
FBA_DQ08 J28 VMA_DQ8
FBA_DQ09 H29 VMA_DQ9
FBA_DQ10 J29 VMA_DQ10
FBA_DQ11 H28 VMA_DQ11
FBA_DQ12 G29 VMA_DQ12
FBA_DQ13 E31 VMA_DQ13
FBA_DQ14 E32 VMA_DQ14
FBA_DQ15 F30 VMA_DQ15
FBA_DQ16 C34 VMA_DQ16
FBA_DQ17 D32 VMA_DQ17
FBA_DQ18 B33 VMA_DQ18
FBA_DQ19 C33 VMA_DQ19
FBA_DQ20 F33 VMA_DQ20
FBA_DQ21 F32 VMA_DQ21
FBA_DQ22 H33 VMA_DQ22
FBA_DQ23 H32 VMA_DQ23
FBA_DQ24 P34 VMA_DQ24
FBA_DQ25 P32 VMA_DQ25
FBA_DQ26 P31 VMA_DQ26
FBA_DQ27 P33 VMA_DQ27
FBA_DQ28 L31 VMA_DQ28
FBA_DQ29 L34 VMA_DQ29
FBA_DQ30 L32 VMA_DQ30
FBA_DQ31 L33 VMA_DQ31
FBA_DQ32 AG28 VMA_DQ32
FBA_DQ33 AF29 VMA_DQ33
FBA_DQ34 AG29 VMA_DQ34
FBA_DQ35 AF28 VMA_DQ35
FBA_DQ36 AD30 VMA_DQ36
FBA_DQ37 AD29 VMA_DQ37
FBA_DQ38 AC29 VMA_DQ38
FBA_DQ39 AD28 VMA_DQ39
FBA_DQ40 AJ29 VMA_DQ40
FBA_DQ41 AK29 VMA_DQ41
FBA_DQ42 AJ30 VMA_DQ42
FBA_DQ43 AK28 VMA_DQ43
FBA_DQ44 AM29 VMA_DQ44
FBA_DQ45 AM31 VMA_DQ45
FBA_DQ46 AN29 VMA_DQ46
FBA_DQ47 AM30 VMA_DQ47
FBA_DQ48 AN31 VMA_DQ48
FBA_DQ49 AN32 VMA_DQ49
FBA_DQ50 AP30 VMA_DQ50
FBA_DQ51 AP32 VMA_DQ51
FBA_DQ52 AM33 VMA_DQ52
FBA_DQ53 AL31 VMA_DQ53
FBA_DQ54 AK33 VMA_DQ54
FBA_DQ55 AK32 VMA_DQ55
FBA_DQ56 AD34 VMA_DQ56
FBA_DQ57 AD32 VMA_DQ57
FBA_DQ58 AC30 VMA_DQ58
FBA_DQ59 AD33 VMA_DQ59
FBA_DQ60 AF31 VMA_DQ60
FBA_DQ61 AG34 VMA_DQ61
FBA_DQ62 AG32 VMA_DQ62
FBA_DQ63 AG33 VMA_DQ63

FBA_CLK0 R30 VMA_CLK0 24
FBA_CLK0_N R31 VMA_CLK0# 24
FBA_CLK1 AB31 VMA_CLK1 24
FBA_CLK1_N AC31 VMA_CLK1# 24

(FBA_DEBUG) FBA_DEBUG0 R28
(NC) FBA_DEBUG1 AC28
FB_VREF_NC H26

FBA_CMD_RFU0 R32 R1014 *60.4/F_4 +1.35V_GFX
FBA_CMD_RFU1 AC32 R1015 *60.4/F_4 +1.35V_GFX

FBA_WCK01 K31 VMA_WCK01 24
FBA_WCK01_N L30 VMA_WCK01# 24
FBA_WCK23 H34 VMA_WCK23 24
FBA_WCK23_N J34 VMA_WCK23# 24
FBA_WCK45 AG30 VMA_WCK45 24
FBA_WCK45_N AG31 VMA_WCK45# 24
FBA_WCK67 AJ34 VMA_WCK67 24
FBA_WCK67_N AK34 VMA_WCK67# 24

FBA_WCKB01 J30
FBA_WCKB01_N J31
FBA_WCKB23 J32
FBA_WCKB23_N J33
FBA_WCKB45 AH31
FBA_WCKB45_N AJ31
FBA_WCKB67 AJ32
FBA_WCKB67_N AJ33

R1016 10K_4

RSVD E1 PS_FB_CLAMP
FB_DLL_AVDD K27 +FB_DLLAVDD
FBA_PLL_AVDD U27 +FB_PLLAVDD
FBVDDQ_PROBE F1 FBVDDQ_SENSE TP1001
GND_PROBE F2 FB_GND_SENSE TP1000
FB_CAL_PD_VDDQ J27 FB_CAL_PD_VDDQ
FB_CAL_PU_GND H27 FB_CAL_PU_GND
FB_CALTERM_GND H25 FB_CAL_TERM_GND

C1054 0.1U/16V_4

Ra R1017 0_4 NV_PLLVDD
Rb R1018 *0_4 +FB_PLLAVDD

+FB_PLLAVDD : 62mA
C1057 0.1U/16V_4
C1058 22U/6.3VS_6

R1019 40.2/F_4 +1.35V_GFX
R1020 40.2/F_4
R1021 60.4/F_4

PLACE CLOSE TO GPU

BOM
N16E-GR: Ra (Default)
N16P-GX/GT/N16S-GTR-B: Rb

BOM
N16E-GR: La (Default)
N16P-GX/GT/N16S-GTR-B: Lb

1029 Change
+FB_PLLAVDD +FB_PLLAVDD
La L1001 BLM15PX330SN1D +3V_GFX
Lb L1000 *BLM15PX330SN1D +1.05V_GFX

25 FBB_CMD[31:0]
FBB_CMD0 D13
FBB_CMD1 E14
FBB_CMD2 F14
FBB_CMD3 A12
FBB_CMD4 B12
FBB_CMD5 C14
FBB_CMD6 B14
FBB_CMD7 G15
FBB_CMD8 F15
FBB_CMD9 E15
FBB_CMD10 D15
FBB_CMD11 A14
FBB_CMD12 D14
FBB_CMD13 A15
FBB_CMD14 B15
FBB_CMD15 C17
FBB_CMD16 D18
FBB_CMD17 E18
FBB_CMD18 F18
FBB_CMD19 A20
FBB_CMD20 B20
FBB_CMD21 C18
FBB_CMD22 B18
FBB_CMD23 G18
FBB_CMD24 G17
FBB_CMD25 F17
FBB_CMD26 D16
FBB_CMD27 A18
FBB_CMD28 D17
FBB_CMD29 A17
FBB_CMD30 B17
FBB_CMD31 E17

25 FBB_DBI[7:0]
FBB_DBI0 E11
FBB_DBI1 E3
FBB_DBI2 A3
FBB_DBI3 C9
FBB_DBI4 F23
FBB_DBI5 F27
FBB_DBI6 C30
FBB_DBI7 A24

25 FBB_EDC[7:0]
FBB_EDC0 D10
FBB_EDC1 D5
FBB_EDC2 C3
FBB_EDC3 B9
FBB_EDC4 E23
FBB_EDC5 E28
FBB_EDC6 B30
FBB_EDC7 A23

GDDR5 NO USE
D9 E4 B2 A9 D22 D28 A30 B23

FBC_DQ00 G9 VMB_DQ0
FBC_DQ01 E9 VMB_DQ1
FBC_DQ02 G8 VMB_DQ2
FBC_DQ03 F9 VMB_DQ3
FBC_DQ04 F11 VMB_DQ4
FBC_DQ05 G11 VMB_DQ5
FBC_DQ06 F12 VMB_DQ6
FBC_DQ07 G12 VMB_DQ7
FBC_DQ08 G6 VMB_DQ8
FBC_DQ09 F5 VMB_DQ9
FBC_DQ10 E6 VMB_DQ10
FBC_DQ11 F6 VMB_DQ11
FBC_DQ12 F4 VMB_DQ12
FBC_DQ13 G4 VMB_DQ13
FBC_DQ14 E2 VMB_DQ14
FBC_DQ15 F3 VMB_DQ15
FBC_DQ16 C2 VMB_DQ16
FBC_DQ17 D4 VMB_DQ17
FBC_DQ18 D3 VMB_DQ18
FBC_DQ19 C1 VMB_DQ19
FBC_DQ20 B3 VMB_DQ20
FBC_DQ21 C4 VMB_DQ21
FBC_DQ22 B5 VMB_DQ22
FBC_DQ23 C5 VMB_DQ23
FBC_DQ24 A11 VMB_DQ24
FBC_DQ25 C11 VMB_DQ25
FBC_DQ26 D11 VMB_DQ26
FBC_DQ27 B11 VMB_DQ27
FBC_DQ28 D8 VMB_DQ28
FBC_DQ29 A8 VMB_DQ29
FBC_DQ30 C8 VMB_DQ30
FBC_DQ31 B8 VMB_DQ31
FBC_DQ32 F24 VMB_DQ32
FBC_DQ33 G23 VMB_DQ33
FBC_DQ34 E24 VMB_DQ34
FBC_DQ35 G24 VMB_DQ35
FBC_DQ36 D21 VMB_DQ36
FBC_DQ37 E21 VMB_DQ37
FBC_DQ38 G21 VMB_DQ38
FBC_DQ39 F21 VMB_DQ39
FBC_DQ40 G27 VMB_DQ40
FBC_DQ41 D27 VMB_DQ41
FBC_DQ42 G26 VMB_DQ42
FBC_DQ43 E27 VMB_DQ43
FBC_DQ44 E29 VMB_DQ44
FBC_DQ45 F29 VMB_DQ45
FBC_DQ46 E30 VMB_DQ46
FBC_DQ47 D30 VMB_DQ47
FBC_DQ48 A32 VMB_DQ48
FBC_DQ49 C31 VMB_DQ49
FBC_DQ50 C32 VMB_DQ50
FBC_DQ51 B32 VMB_DQ51
FBC_DQ52 D29 VMB_DQ52
FBC_DQ53 A29 VMB_DQ53
FBC_DQ54 C29 VMB_DQ54
FBC_DQ55 B29 VMB_DQ55
FBC_DQ56 B21 VMB_DQ56
FBC_DQ57 C23 VMB_DQ57
FBC_DQ58 A21 VMB_DQ58
FBC_DQ59 C21 VMB_DQ59
FBC_DQ60 B24 VMB_DQ60
FBC_DQ61 C24 VMB_DQ61
FBC_DQ62 B26 VMB_DQ62
FBC_DQ63 C26 VMB_DQ63

VMA_DQ[63:0] VMA_DQ[63:0] 24
VMB_DQ[63:0] VMB_DQ[63:0] 25

FBC_DQM0 FBC_DQM1 FBC_DQM2 FBC_DQM3 FBC_DQM4 FBC_DQM5 FBC_DQM6 FBC_DQM7

FBC_DQS_WP0 FBC_DQS_WP1 FBC_DQS_WP2 FBC_DQS_WP3 FBC_DQS_WP4 FBC_DQS_WP5 FBC_DQS_WP6 FBC_DQS_WP7

FBC_DQS_RN0 FBC_DQS_RN1 FBC_DQS_RN2 FBC_DQS_RN3 FBC_DQS_RN4 FBC_DQS_RN5 FBC_DQS_RN6 FBC_DQS_RN7

FBC_CLK0 D12 VMB_CLK0 25
FBC_CLK0_N E12 VMB_CLK0# 25
FBC_CLK1 E20 VMB_CLK1 25
FBC_CLK1_N F20 VMB_CLK1# 25

(FBC_DEBUG) FBB_DEBUG0 G14
(NC) FBB_DEBUG1 G20

FBB_CMD_RFU0 C12 R1012 *60.4/F_4 +1.35V_GFX
FBB_CMD_RFU1 C20 R1013 *60.4/F_4

FBB_WCK01 F8 VMB_WCK01 25
FBB_WCK01_N E8 VMB_WCK01# 25
FBB_WCK23 A5 VMB_WCK23 25
FBB_WCK23_N A6 VMB_WCK23# 25
FBB_WCK45 D24 VMB_WCK45 25
FBB_WCK45_N D25 VMB_WCK45# 25
FBB_WCK67 B27 VMB_WCK67 25
FBB_WCK67_N C27 VMB_WCK67# 25

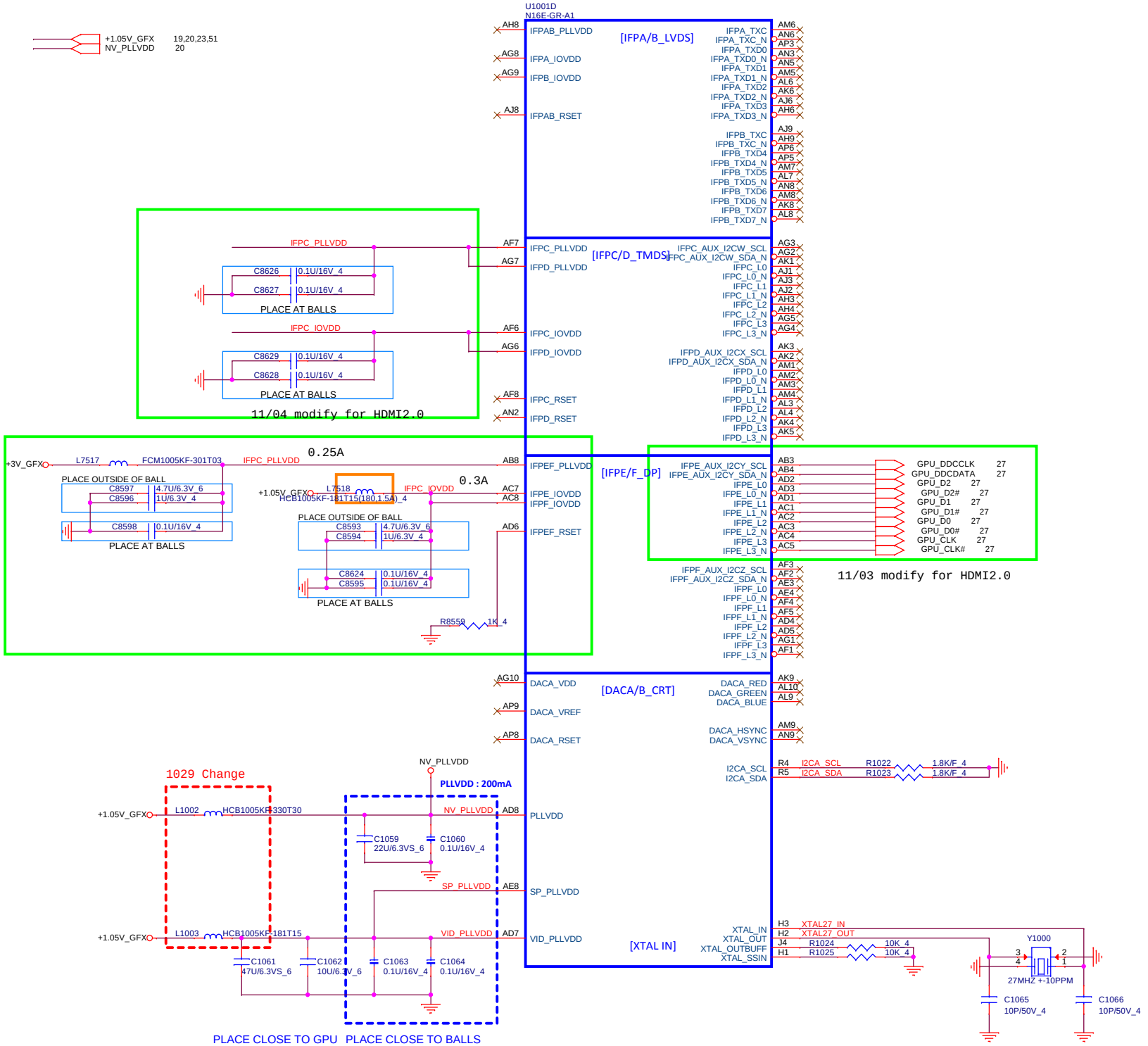
FBB_WCKB01 D6
FBB_WCKB01_N D7
FBB_WCKB23 C6
FBB_WCKB23_N B6
FBB_WCKB45 F26
FBB_WCKB45_N E26
FBB_WCKB67 A26
FBB_WCKB67_N A27

FBB_PLL_AVDD H17 +FB_PLLAVDD
C1056 0.1U/16V_4
PLACE CLOSE TO BALL

PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N16P-GX/GT - 2/5 (Memory)	1A

Date: Thursday, December 24, 2015 Sheet 20 of 51

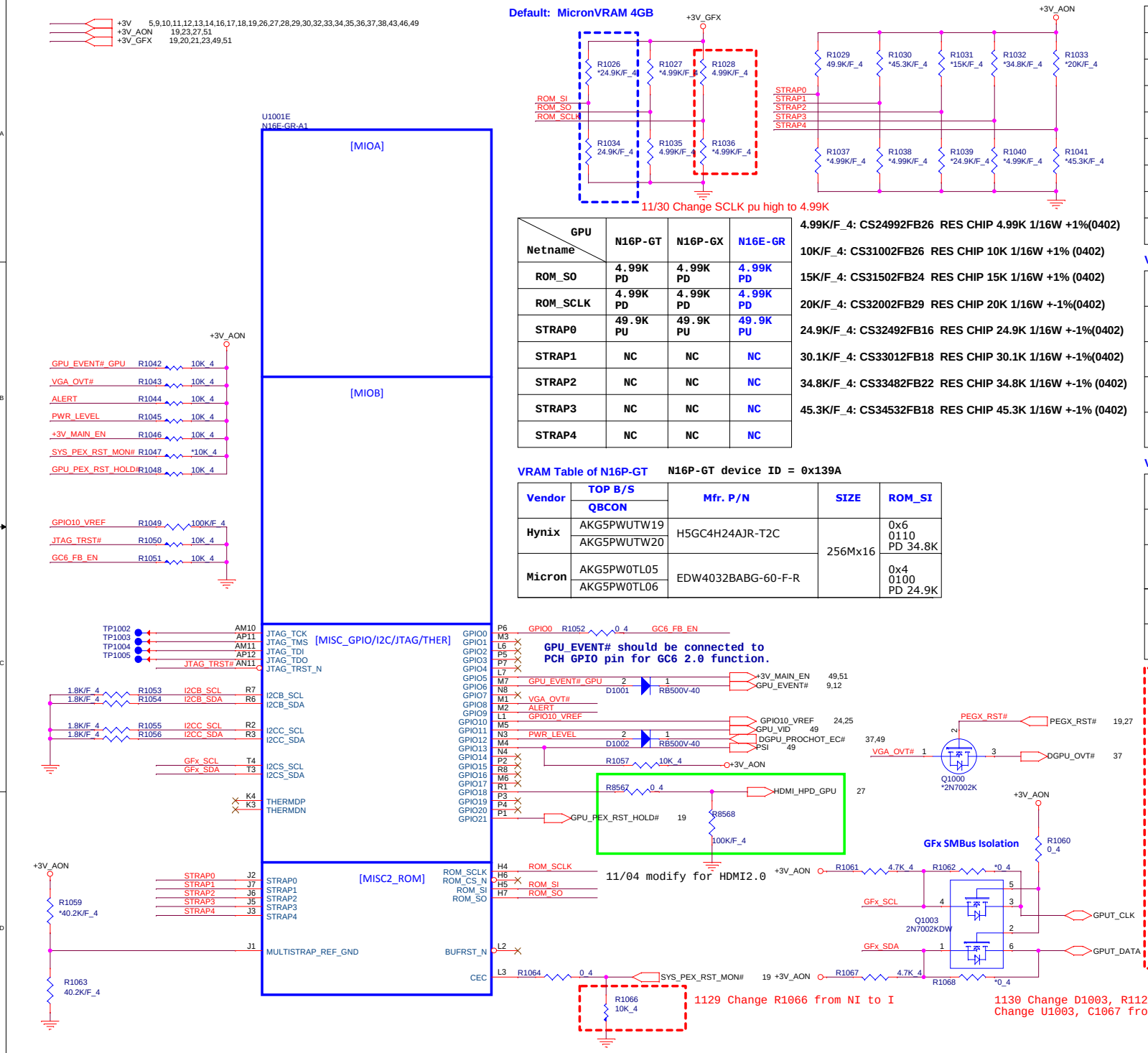


PROJECT : G35

Quanta Computer Inc.

Size	Document Number	Rev
A3	N16P-GX/GT - 3/5 (Display)	1A

Date: Thursday, December 24, 2015 | Sheet 21 of 51



Resistor Values	PU to 3V3_MAIN	PD to GND
4.99K OHM	1000	0000
10K OHM	1001	0001
15K OHM	1010	0010
20K OHM	1011	0011
24.9K OHM	1100	0100
30.1K OHM	1101	0101
34.8K OHM	1110	0110
45.3K OHM	1111	0111

GPU / Netname	N16P-GT	N16P-GX	N16E-GR
ROM_SO	4.99K PD	4.99K PD	4.99K PD
ROM_SCLK	4.99K PD	4.99K PD	4.99K PD
STRAP0	49.9K PU	49.9K PU	49.9K PU
STRAP1	NC	NC	NC
STRAP2	NC	NC	NC
STRAP3	NC	NC	NC
STRAP4	NC	NC	NC

4.99K/F_4: CS24992FB26 RES CHIP 4.99K 1/16W +1%(0402)

10K/F_4: CS31002FB26 RES CHIP 10K 1/16W +1% (0402)

15K/F_4: CS31502FB24 RES CHIP 15K 1/16W +1% (0402)

20K/F_4: CS32002FB29 RES CHIP 20K 1/16W +-1%(0402)

24.9K/F_4: CS32492FB16 RES CHIP 24.9K 1/16W +-1%(0402)

30.1K/F_4: CS33012FB18 RES CHIP 30.1K 1/16W +-1%(0402)

34.8K/F_4: CS33482FB22 RES CHIP 34.8K 1/16W +-1% (0402)

45.3K/F_4: CS34532FB18 RES CHIP 45.3K 1/16W +-1% (0402)

VRAM Table of N16P-GT N16P-GT device ID = 0x139A

Vendor	TOP B/S / QBCON	Mfr. P/N	SIZE	ROM_SI
Hynix	AKG5PWUTW19	H5GC4H24AJR-T2C	256Mx16	0x6 0110 PD 34.8K
	AKG5PWUTW20			
Micron	AKG5PW0TL05	EDW4032BABG-60-F-R		0x4 0100 PD 24.9K
	AKG5PW0TL06			

VRAM Table of N16P-GX N16P-GX device ID = 0x139B

Vendor	TOP B/S / QBCON	Mfr. P/N	SIZE	ROM_SI
Hynix	AKG5PWUTW19	H5GC4H24AJR-T2C	256Mx16	0x6 0110 PD 34.8K
	AKG5PWUTW20			
Micron	AKG5PW0TL05	EDW4032BABG-60-F-R		0x4 0100 PD 24.9K
	AKG5PW0TL06			
Micron	AKG5LGUTL02	MT51J256M32HF-60:A	256Mx32	0x9 1001 PU 10K
	AKG5LGUTL03			
Samsung	AKG5QGDT503	K4G80325FB-HC03		0x8 1000 PU 4.99K
	AKG5QGDT504			

VRAM Table of N16E-GR N16E-GR device ID = 0x1427

Vendor	TOP B/S / QBCON	Mfr. P/N	SIZE	ROM_SI
Hynix	AKG5PWUTW19	H5GC4H24AJR-T2C	256Mx16	0x0 0110 PD 4.99K
	AKG5PWUTW20			
Micron	AKG5PW0TL05	EDW4032BABG-60-F-R		0x1 0001 PD 10K
	AKG5PW0TL06			
Micron	AKG5LGUTL02	MT51J256M32HF-60:A	256Mx32	0x4 0100 PD 24.9K
	AKG5LGUTL03			
Samsung	AKG5QGDT503	K4G80325FB-HC03		0x3 0011 PD 20K
	AKG5QGDT504			

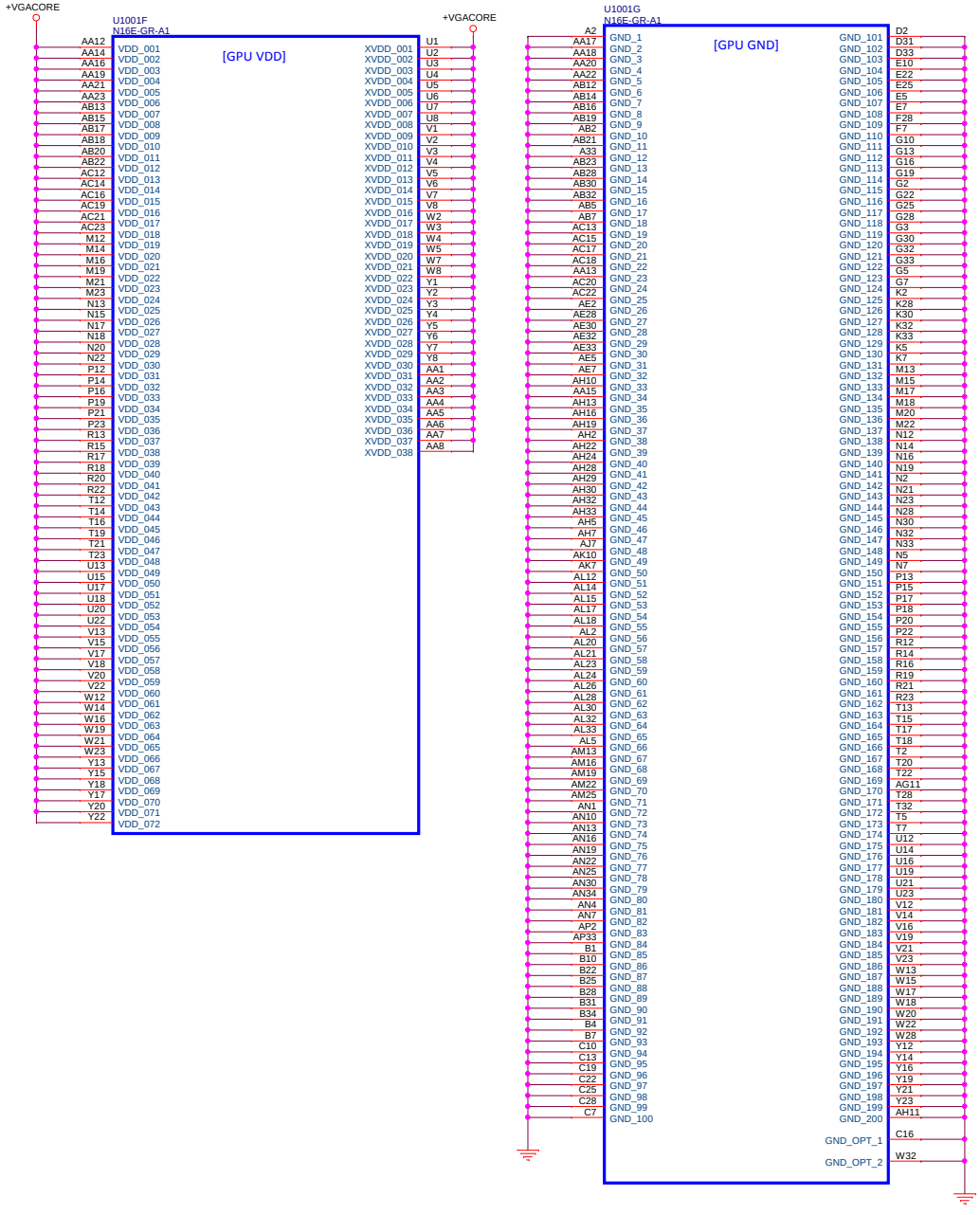
PROJECT : G35
Quanta Computer Inc.

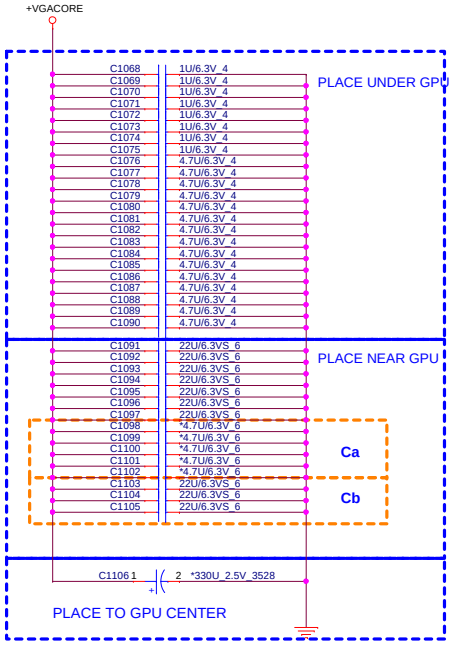
Size	Document Number	Rev
Custom	N16P-GX/GT - 4/5 (MISC)	1A

Date: Thursday, December 24, 2015 Sheet 22 of 51

+3V_AON 19,22,27,51
+3V_GFX 19,20,21,22,49,51
+1.35V_GFX 20,24,25,50
+1.05V_GFX 19,20,21,51
+VGACORE 49

VDD/XVDD : 62A





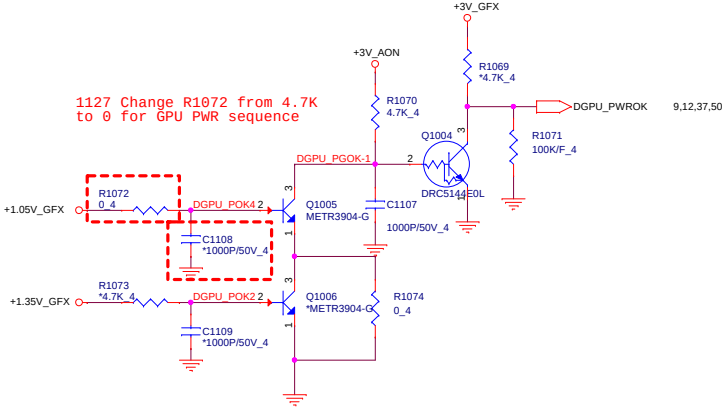
GPU BOM:

N16E-GR: Ca Unstuff, Cb Stuff (Default)

N16P-GX/GT/N16S-GTR-B: Ca change 4.7u stuff , Cb unstuff

4.7 uF : CH5471K9E07 CAP CHIP 4.7U 6.3V(+-10%,X5R,0603)

For meet Power down sequence for +3V_GFX



1127 Change R1072 from 4.7K to 0 for GPU PWR sequence

1127 Change C1108 from I to NI for GPU PWR sequence

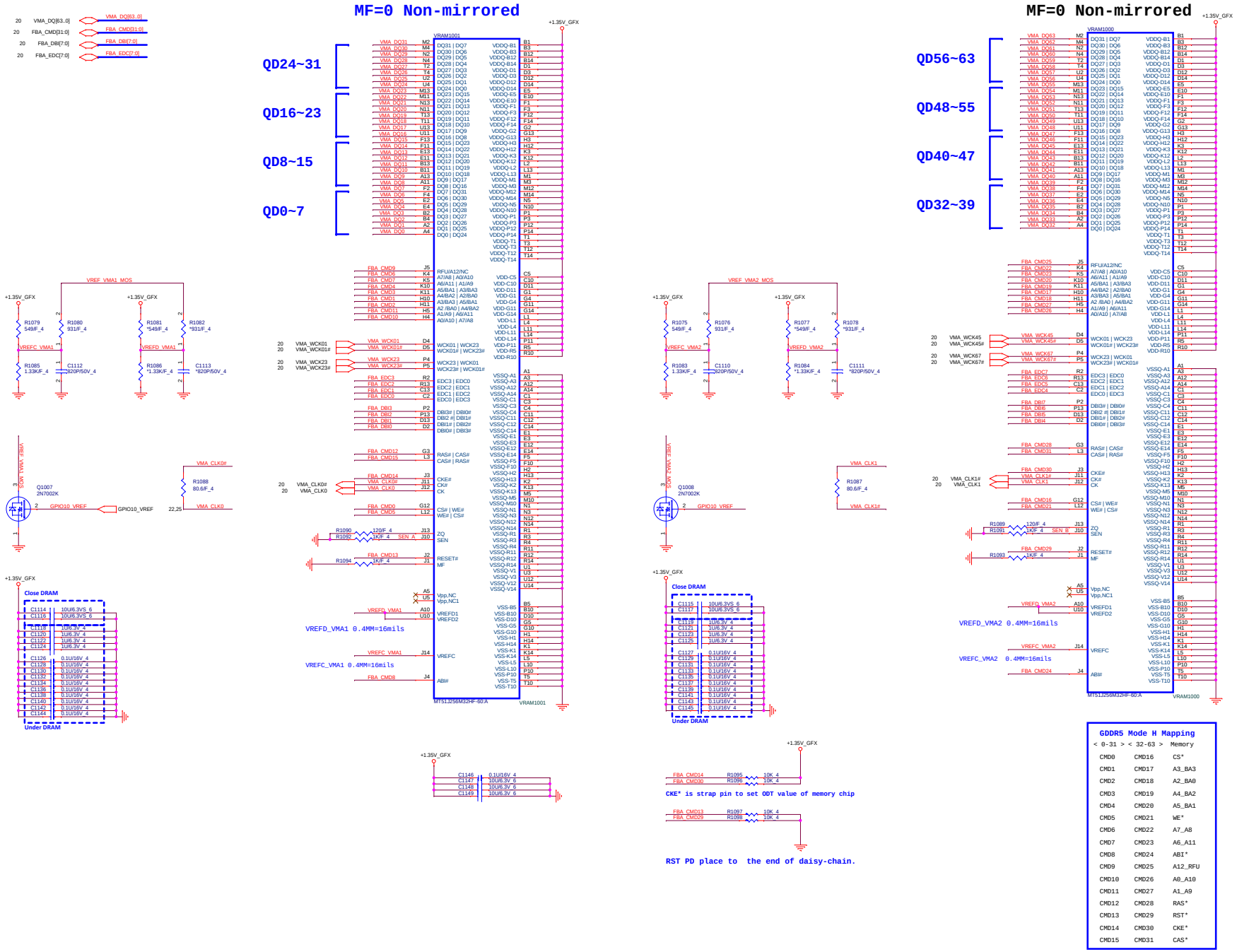
PROJECT : G35

Quanta Computer Inc.

Size	Document Number	Rev
Custom	N16P-GX/GT - 5/5 (Power)	1A

Date: Thursday, December 24, 2015 Sheet 23 of 51

CHANNEL A: 2G/4G GDDR5



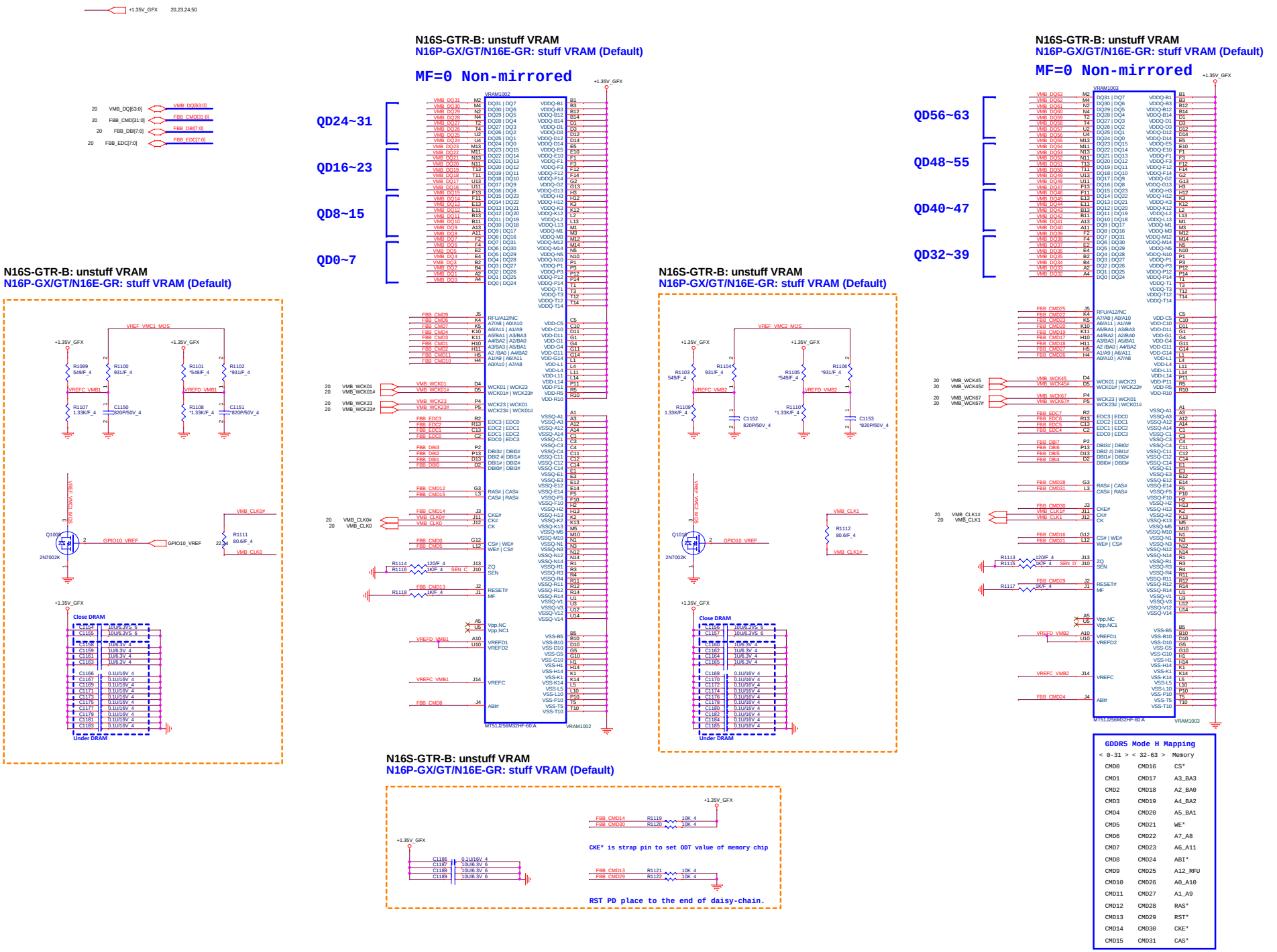
GDDR5 Mode H Mapping

< 0-31 >	< 32-63 >	Memory
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*

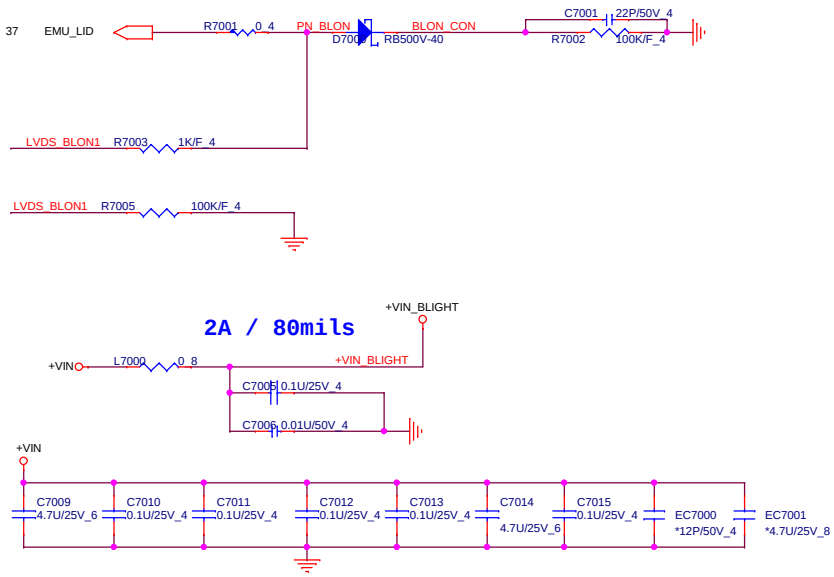
PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
	N16P-GX/GT GDDR5 VRAM 1/2	1A

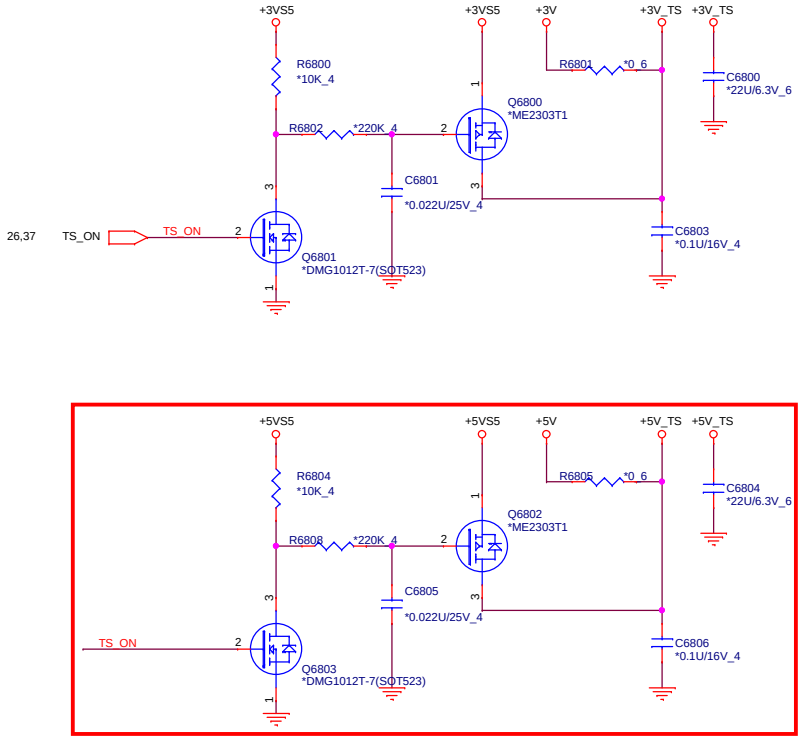
Thursday, September 24, 2015 Sheet 61


N16S-GTR-B: unstuff VRAM
N16P-GX/GT/N16E-GR: stuff VRAM (Default)
MF=0 Non-mirrored
QD24~31
QD16~23
QD8~15
QD0~7
QD56~63
QD48~55
QD40~47
QD32~39
VRAM1002
VRAM1003
M51J256M32HF-60A
+1.35V_GFX
VREF_VMC1_MOS
VREF_VMC2_MOS
VREFD_VMB1
VREFC_VMB1
VREFD_VMB2
VREFC_VMB2
GPIO10_VREF
VMB_CLK0#
VMB_CLK0
VMB_CLK1#
VMB_CLK1
VMB_WCK01
VMB_WCK01#
VMB_WCK23
VMB_WCK23#
VMB_WCK45
VMB_WCK45#
VMB_WCK67
VMB_WCK67#
FBB_CMD8
FBB_CMD13
FBB_CMD14
FBB_CMD29
FBB_CMD30
Close DRAM
Under DRAM
CKE* is strap pin to set ODT value of memory chip
RST PD place to the end of daisy-chain.
GDDR5 Mode H Mapping
< 0-31 > < 32-63 > Memory
CMD0 CMD16 CS*
CMD1 CMD17 A3_BA3
CMD2 CMD18 A2_BA0
CMD3 CMD19 A4_BA2
CMD4 CMD20 A5_BA1
CMD5 CMD21 WE*
CMD6 CMD22 A7_A8
CMD7 CMD23 A6_A11
CMD8 CMD24 ABI*
CMD9 CMD25 A12_RFU
CMD10 CMD26 A0_A10
CMD11 CMD27 A1_A9
CMD12 CMD28 RAS*
CMD13 CMD29 RST*
CMD14 CMD30 CKE*
CMD15 CMD31 CAS*
PROJECT : G35
Quanta Computer Inc.
Size
Document Number
N16P-GX/GT GDDR5 VRAM 2/2
Rev
1A
Thursday, December 24, 2015
Sheet 61

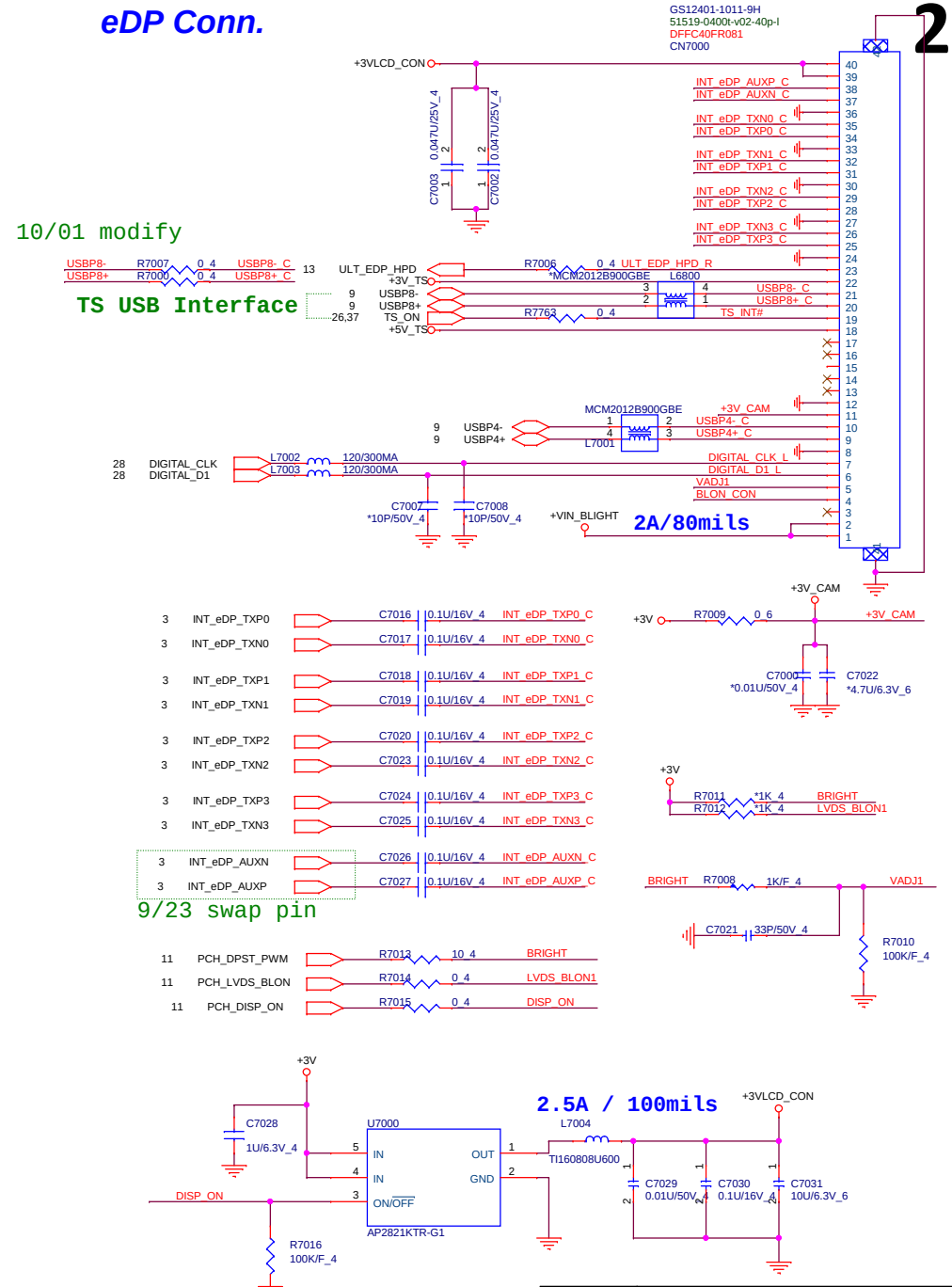
LID Switch



Touch screen



eDP Conn.

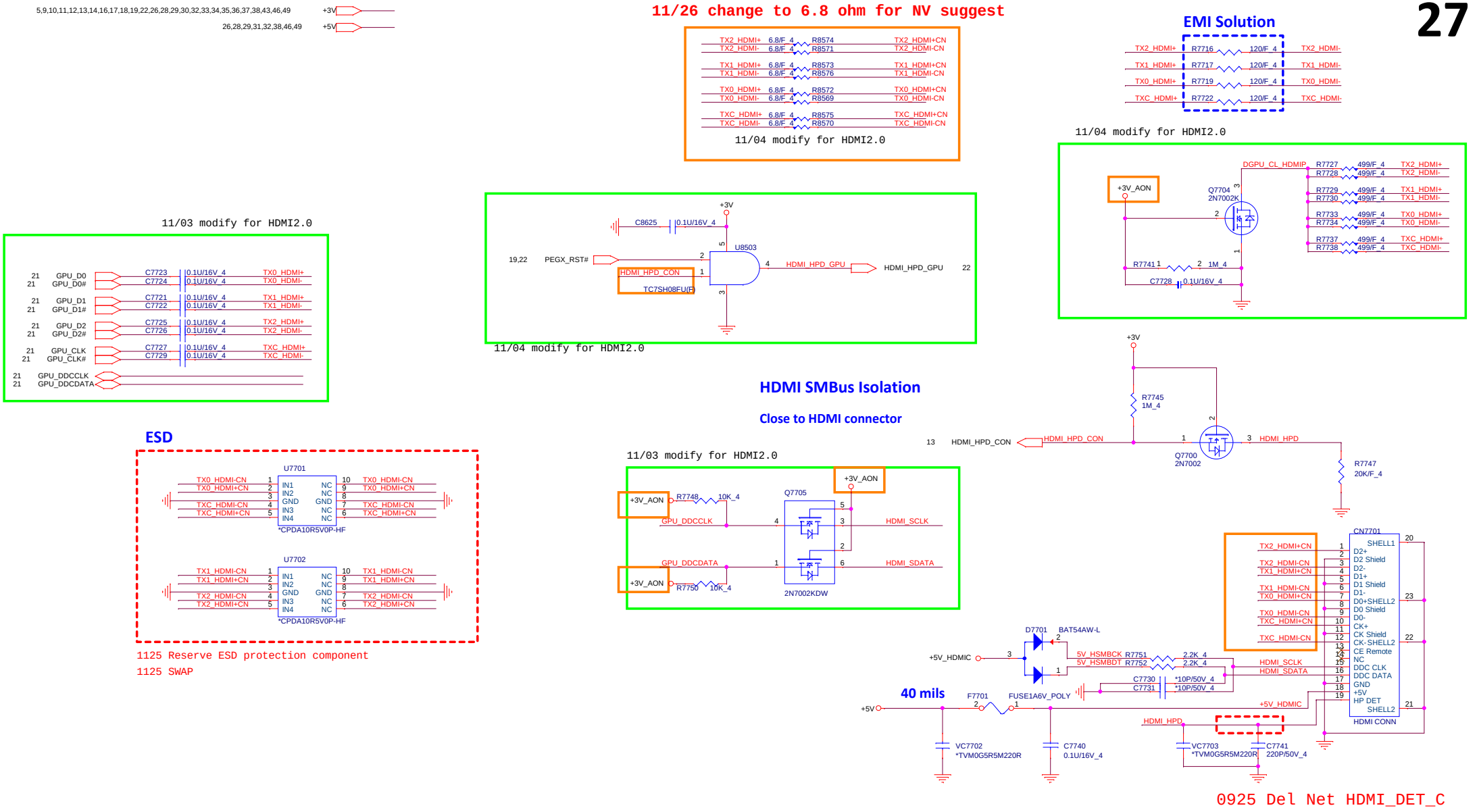


5,9,10,11,12,13,14,16,17,18,19,22,27,28,29,30,32,33,34,35,36,37,38,43,46,49 +3V
5,10,30,33,37,38,40,41 +3VPCU
27,28,29,31,32,38,46,49 +5V
38,39,40,41,42,43,44,45,46,47,48,49,50 +VIN

PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A

Date: Thursday, December 24, 2015 | Sheet 26 of 51

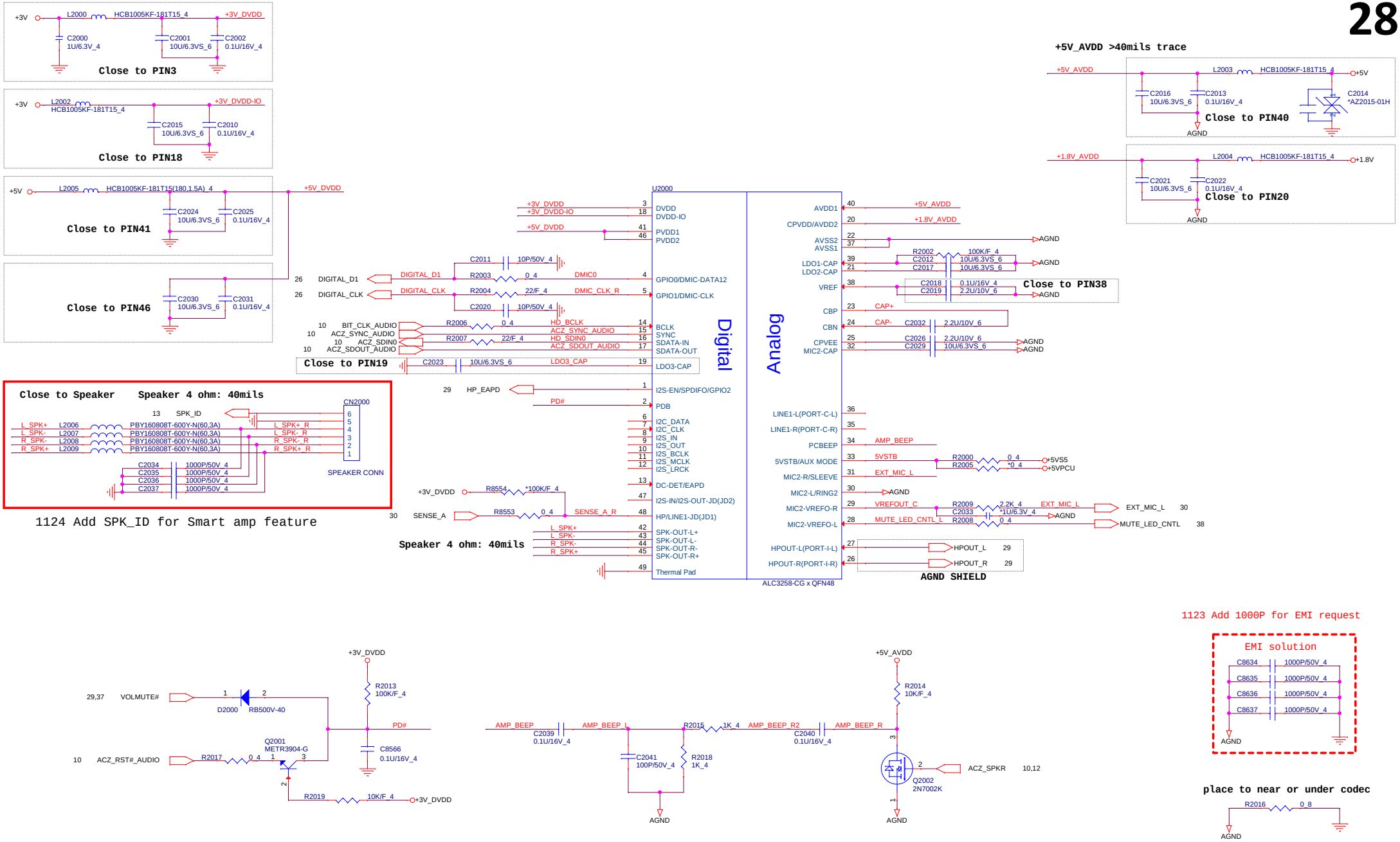


PROJECT : G35

Quanta Computer Inc.

Size	Document Number	Rev
Custom	27 -- HDMI/HDMI REDRIVER	1A

Date: Thursday, December 24, 2015 | Sheet 27 of 51

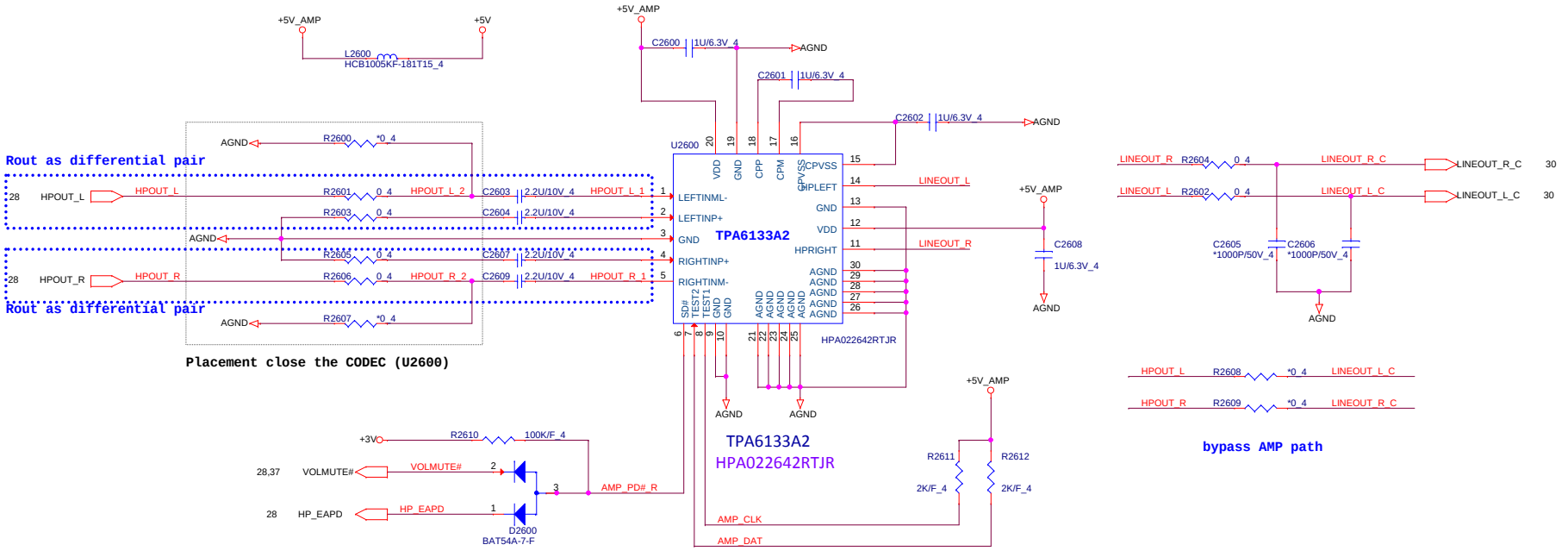


PROJECT : G35
Quanta Computer Inc.

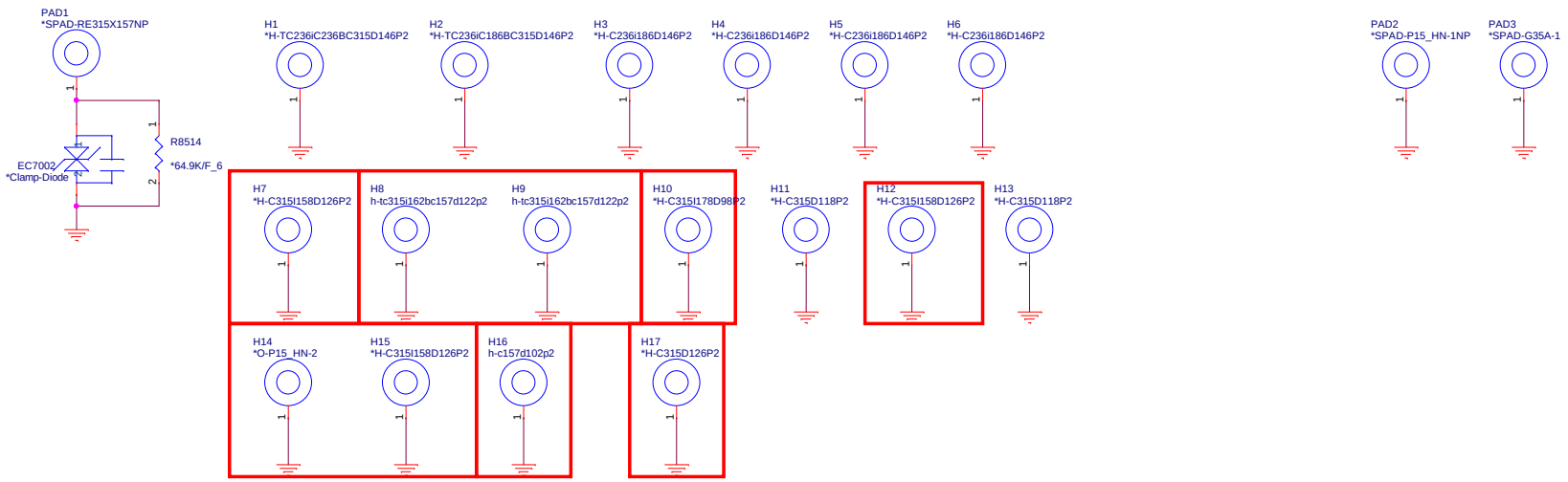
Size	Document Number	Rev
Custom	28 -- AUDIO CODEC ALC3258-CG	C5

Date: Thursday, December 24, 2015 | Sheet 28 of 51

Head Phone out



HOLE



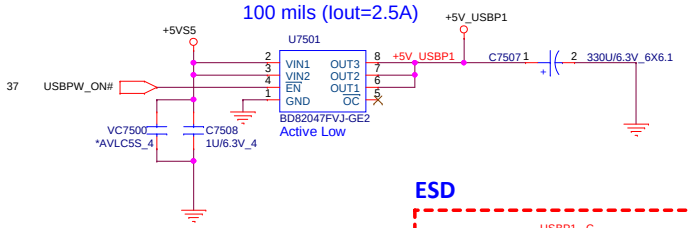
PROJECT : G35

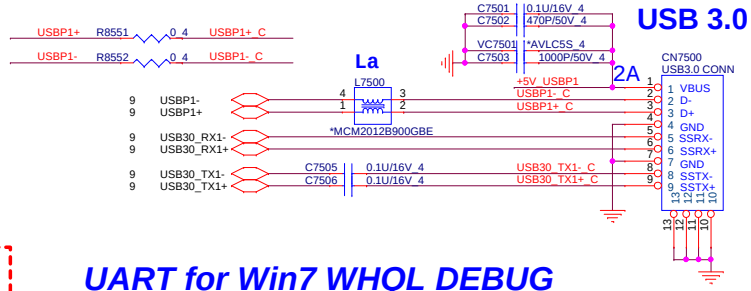
Quanta Computer Inc.

Size	Document Number	Rev
Custom	29-- HP AMP HPA022642RTJR	1A

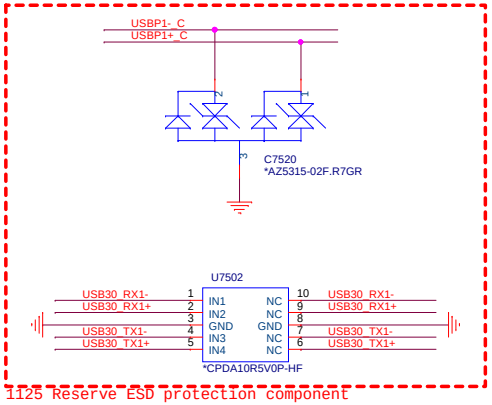
Date: Thursday, December 24, 2015 | Sheet 29 of 51

USB 2.0/3.0 Combo



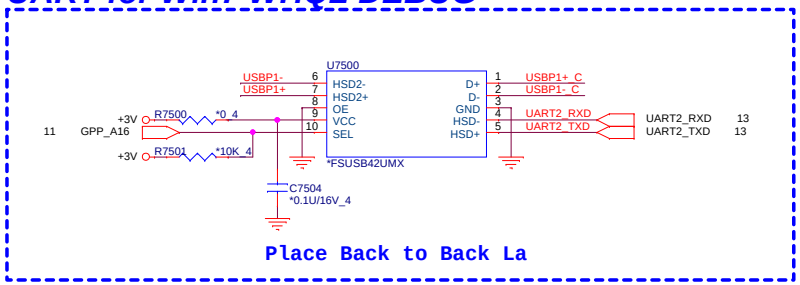


ESD



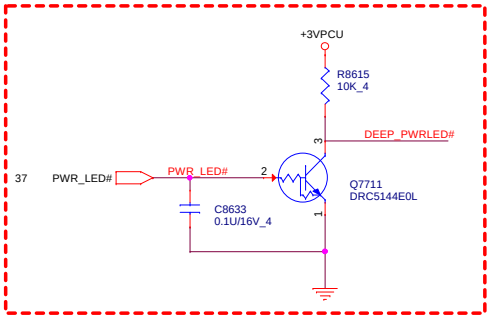
1125 Reserve ESD protection component

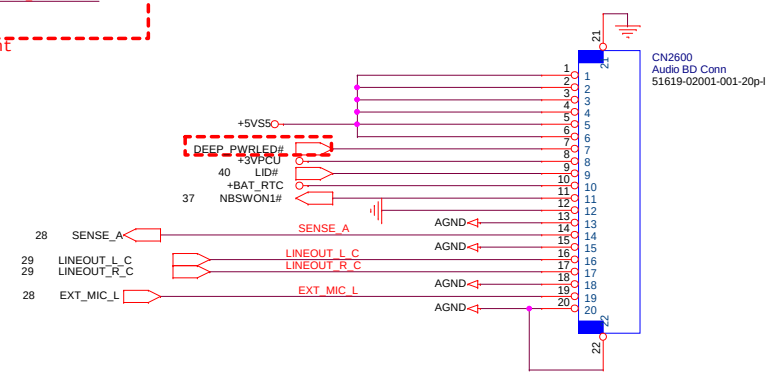
UART for Win7 WHQL DEBUG

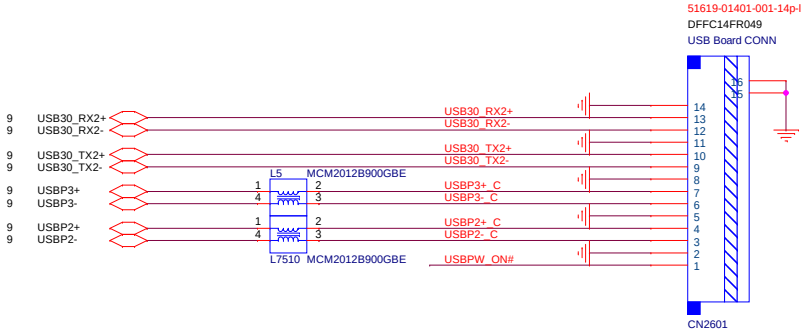


Daughter Board

1123 Add PWR LED MOS Circuit





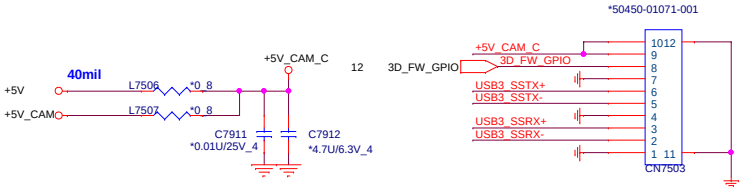


PROJECT : G35 Quanta Computer Inc.		
Size Custom	Document Number 30 – USB3.0/DB	Rev 1A
Date: Thursday, December 24, 2015	Sheet 30 of 51	

3D CAMERA

10/08 3D Camera MIC combine in LCD CONN

3D Camera Conn.



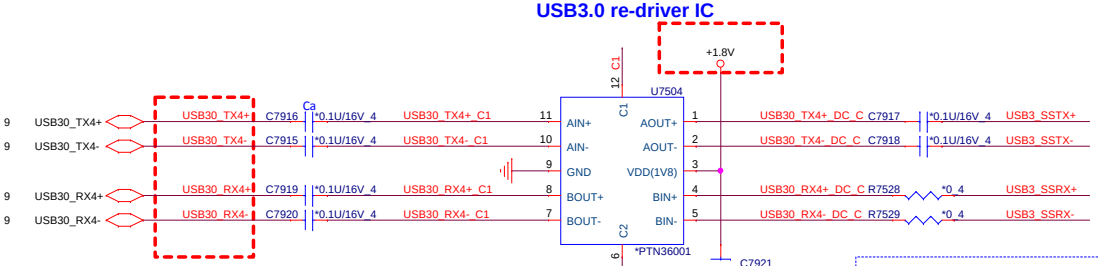
USB3.0

USB3.0 Re-driver IC

1123 Change UB3 re driver power rail
from +1.8V_DEEP_SUS to +1.8V

1123 Change UB3 re driver power rail
from +1.8V_DEEP_SUS to +1.8V

USB3.0 re-driver IC



0925 Correct Port net name

Layout Notes:
Stubs Trace less than 150mil

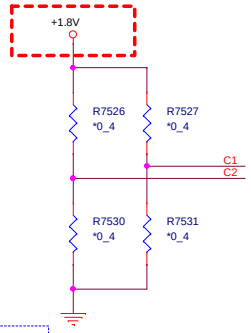


Table 4. C1 pin controls long/medium/short traces

State	Channel type	Pin C1 state	Channel B	Channel A	
			EQ[1]	DE[2]	OS[3]
H	Long	H	9 dB	–5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	–3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

Table 5. C2 pin controls long/medium/short traces

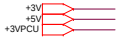
State	Channel type	Pin C2 state	Channel A	Channel B	
			EQ[1]	DE[2]	OS[3]
H	Long	H	9 dB	–5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	–3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

28,40,41,46,51 +5VPCU
5,10,30,33,37,38,40,41 +3VPCU
28,47 +1.8V

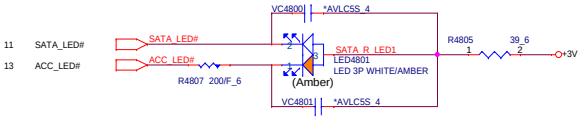
PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	31 – 3D CAM/REDRIVER	1A

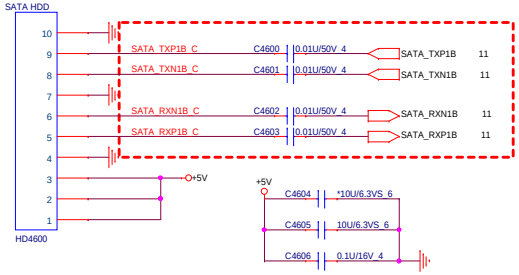
Date: Thursday, December 24, 2015 Sheet 31 of 51



SATA LED



HDD

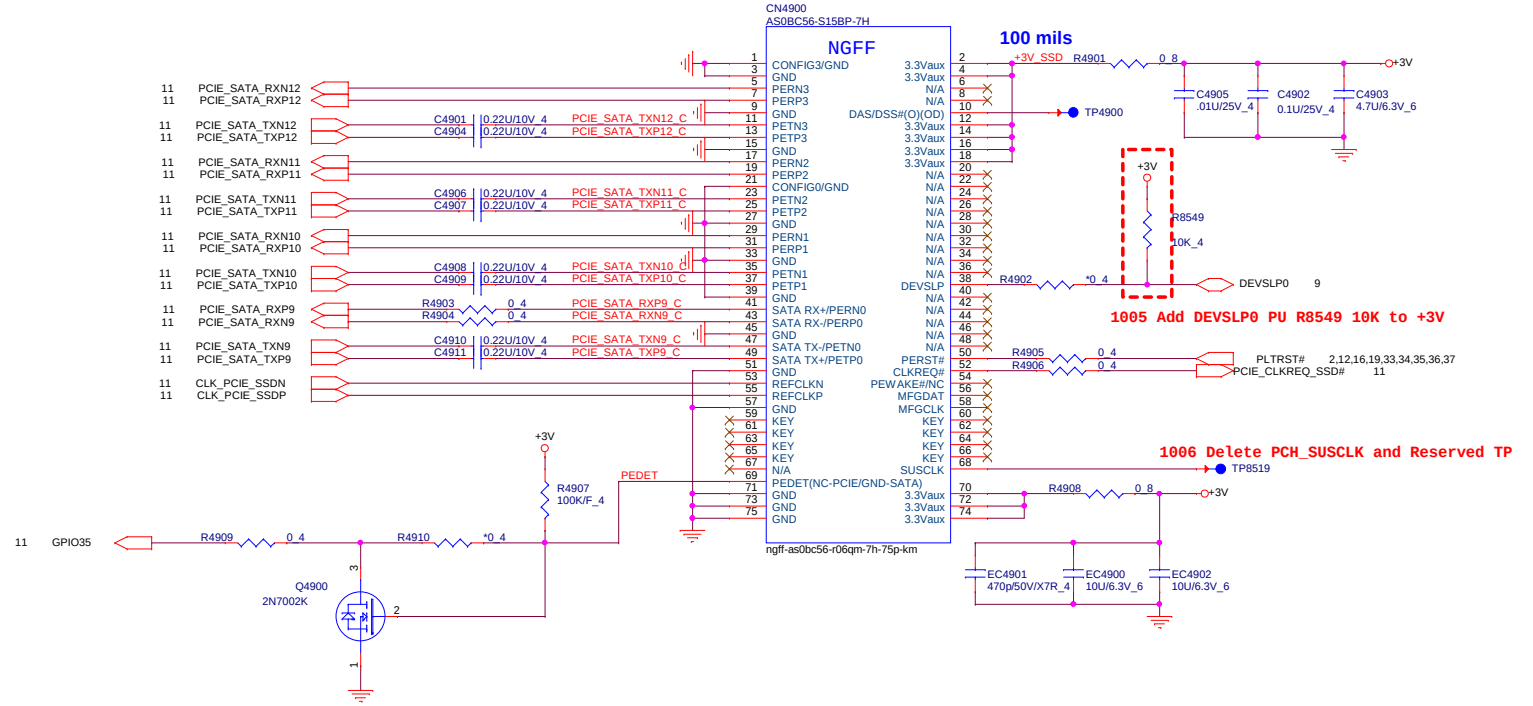


PROJECT : G35
Quanta Computer Inc.

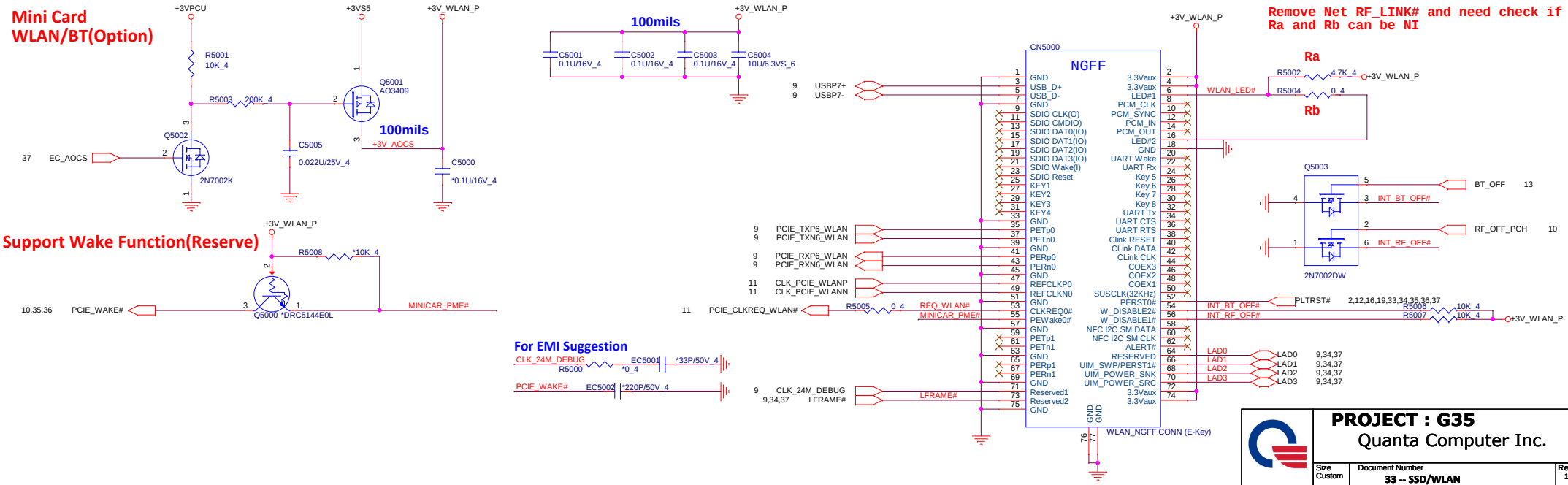
Size	Document Number	Rev
C	32 -- HDD/ODD	1A

Date: Thursday, December 24, 2015 Sheet 32 of 51

SSD



Mini Card WLAN/BT(Option)



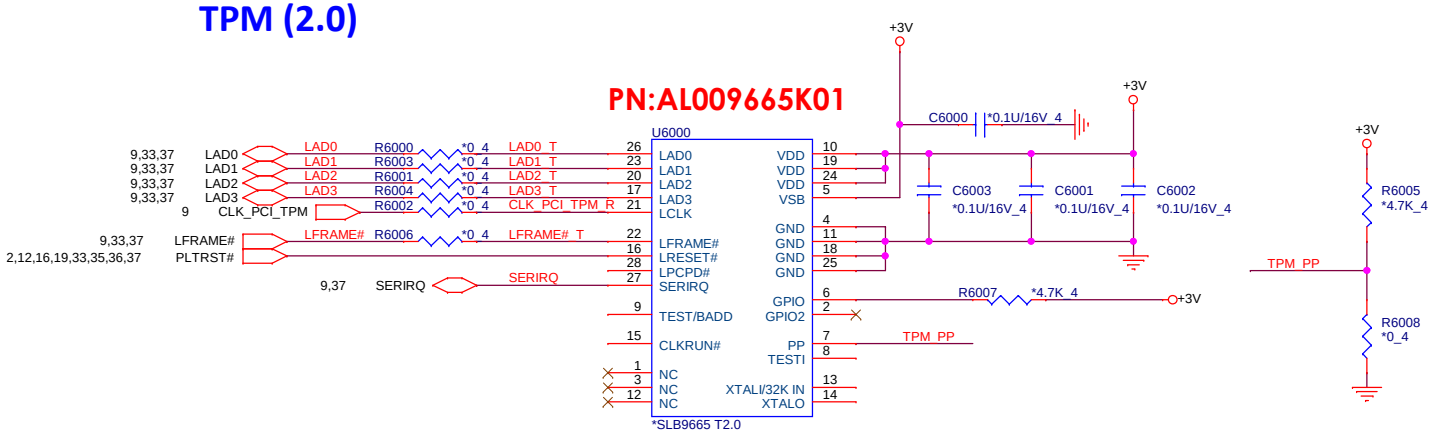
PROJECT : G35

Quanta Computer Inc.

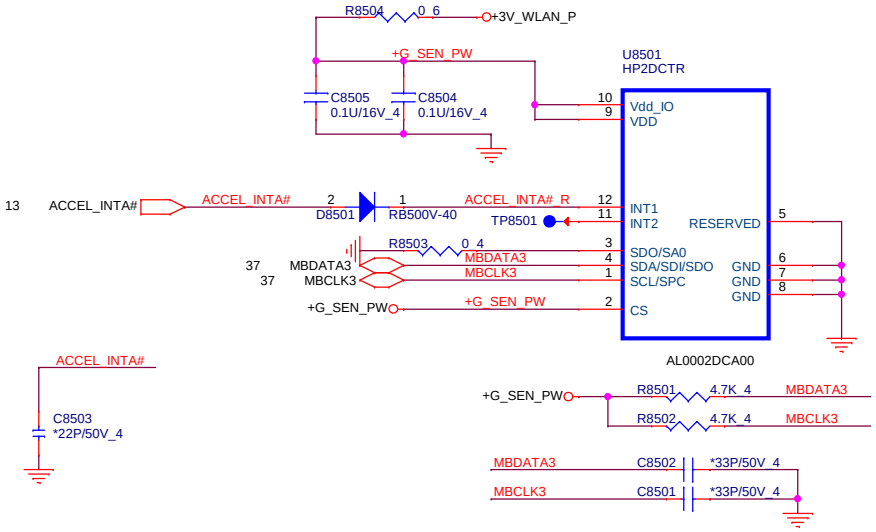
Size	Document Number	Rev
Custom	33 -- SSD/WLAN	1A

Date: Thursday, December 24, 2015 | Sheet 33 of 51

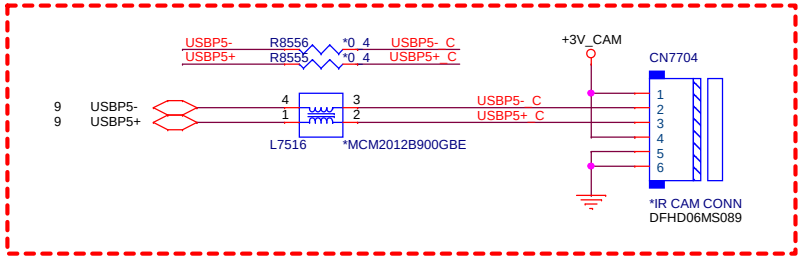
TPM (2.0)



Accelerometer Sensor



IR CAM



1015 Add IR CAM circuit

PROJECT : G35

Quanta Computer Inc.

B	34 - TPM/G-Sensor	Document Number	1A Rev
	Thursday, December 24, 2015	34	51
	Date:	Sheet	of

LAN & RJ45

35

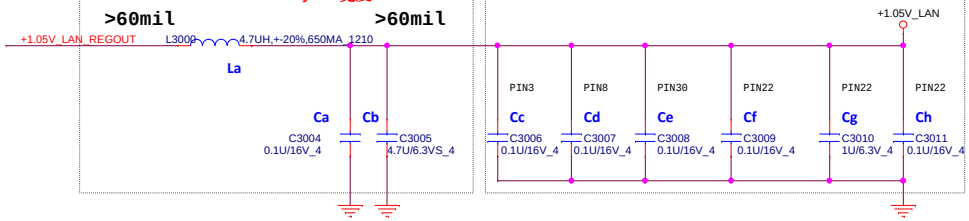
For SWR mode support RTL8111HSH/RTL8107ESH

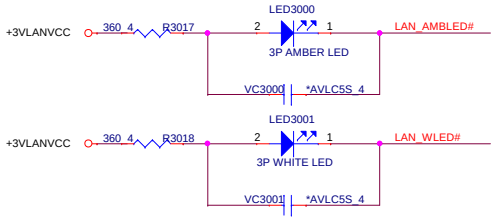
Stuff La, Ca ,Cb

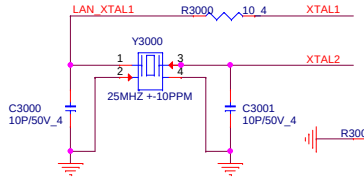
* Place Cc,Cd,Ce,Cf for RTL8111H(S) & RTL8107E(S) close to each VDD10 pin-- 3, 22, 8 , 30

* Place Cg,Ch for RTL8111H(S) & RTL8107E(S) close to each VDD10 pin-- 22(reserved)

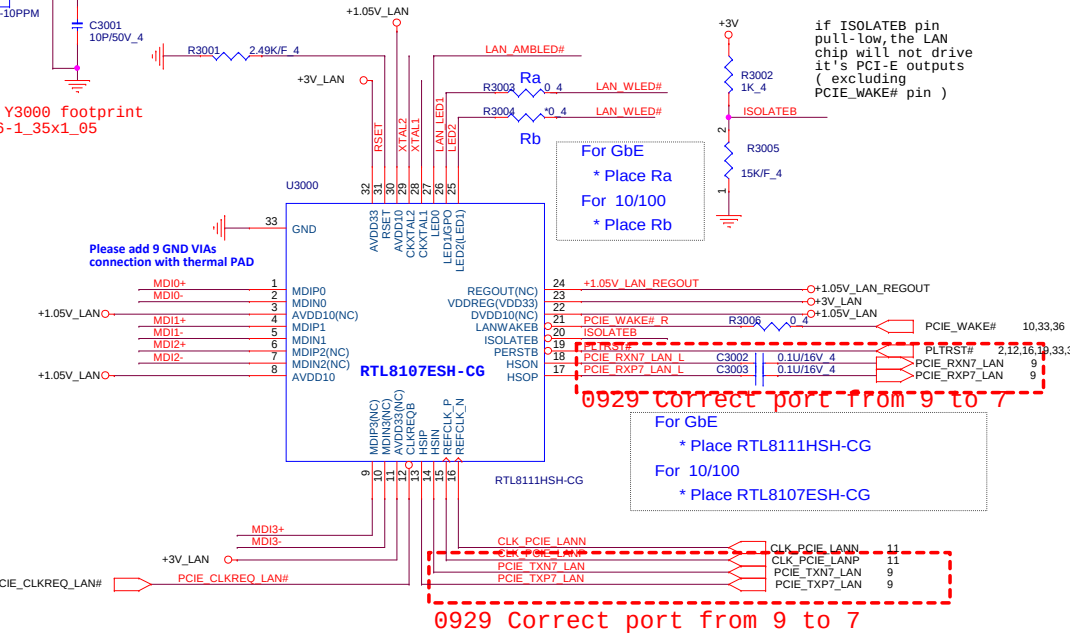
Power trace Layout 寬度> 60mil







1028 Change Y3000 footprint to xtl-2x1_6-1_35x1_05

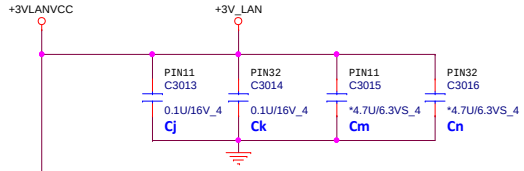


For 10/100 stuff only

Close RJ45

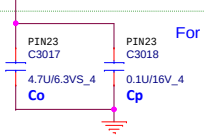
* Place Cj and Ck, close to each VDD33 pin-- 11, 32 for RTL8111H(S) & RTL8107E(S)

* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)



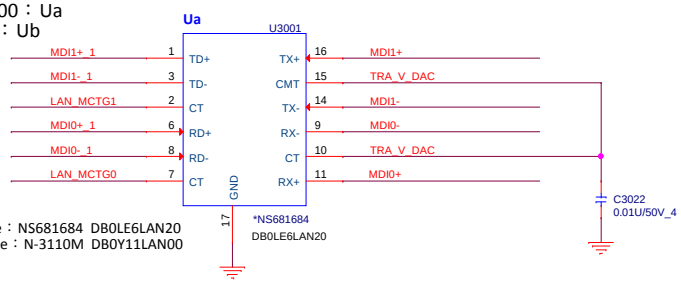
For SWR mode support RTL8111HSH/RTL8107ESH

Stuff Co, Cp



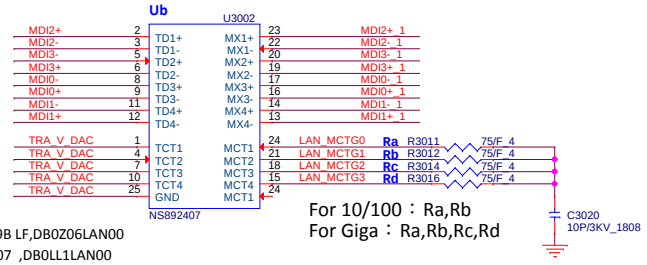
For 10/100：Ua

For Giga：Ub



1st source：NS681684 DB0LE6LAN20

2nd source：N-3110M DB0Y11LAN00



For GiGA

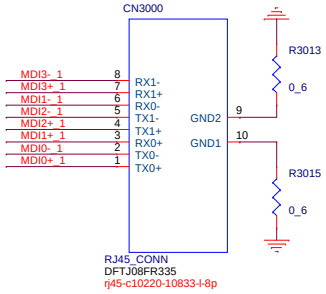
BOT:GST5009B LF,DB0Z06LAN00

FCE :NS892407 ,DB0LL1LAN00

For 10/100：Ra,Rb

For Giga：Ra,Rb,Rc,Rd

RJ45



5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,36,37,38,43,46,49 +3V

46 +3VLANVCC

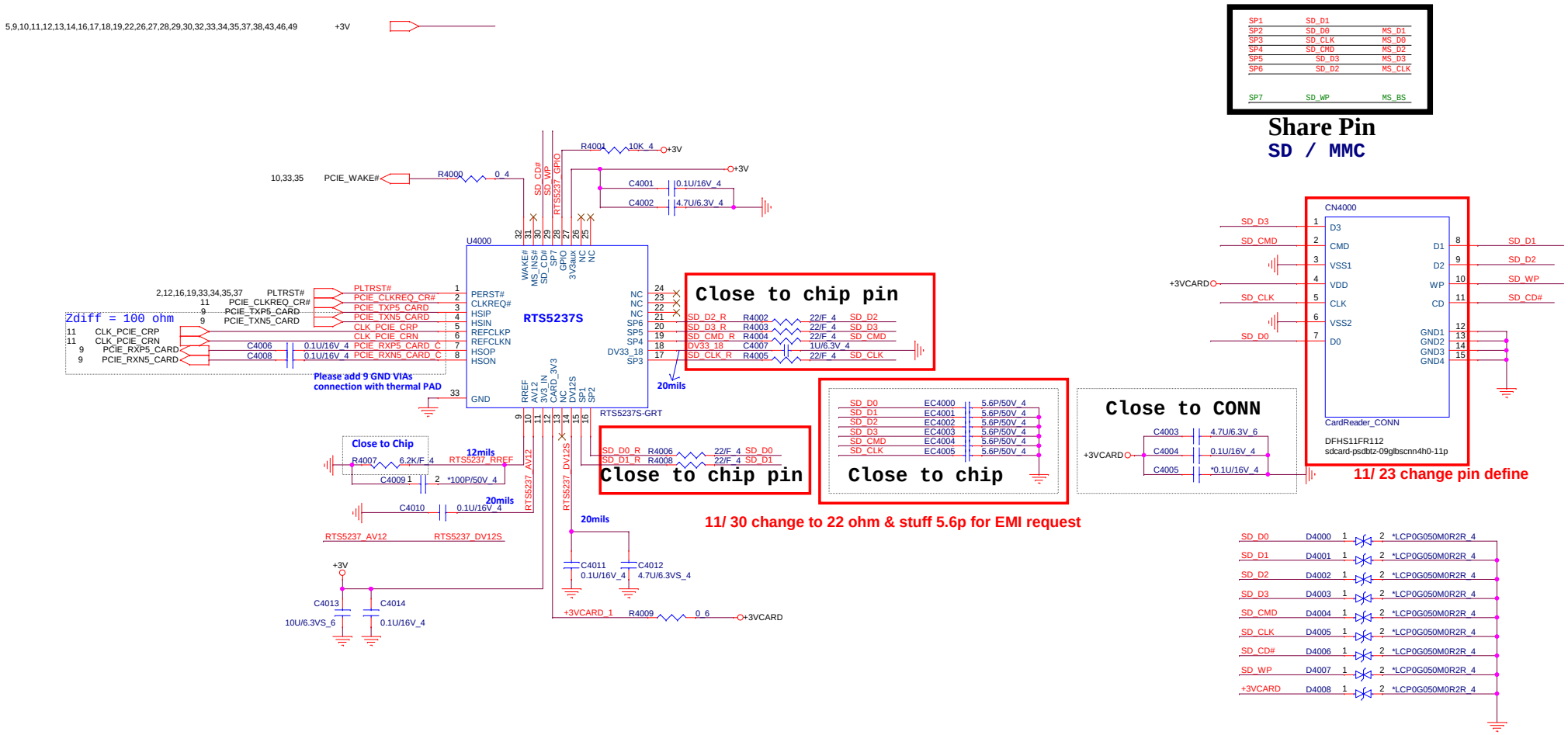
PROJECT : G35

Quanta Computer Inc.

Size	Document Number	Rev
Custom	35 – LAN RTL8107ESH-CG/RJ45	1A

Date: Thursday, December 24, 2015 Sheet 35 of 51

RTS5237S PCIE CARD READER Controller

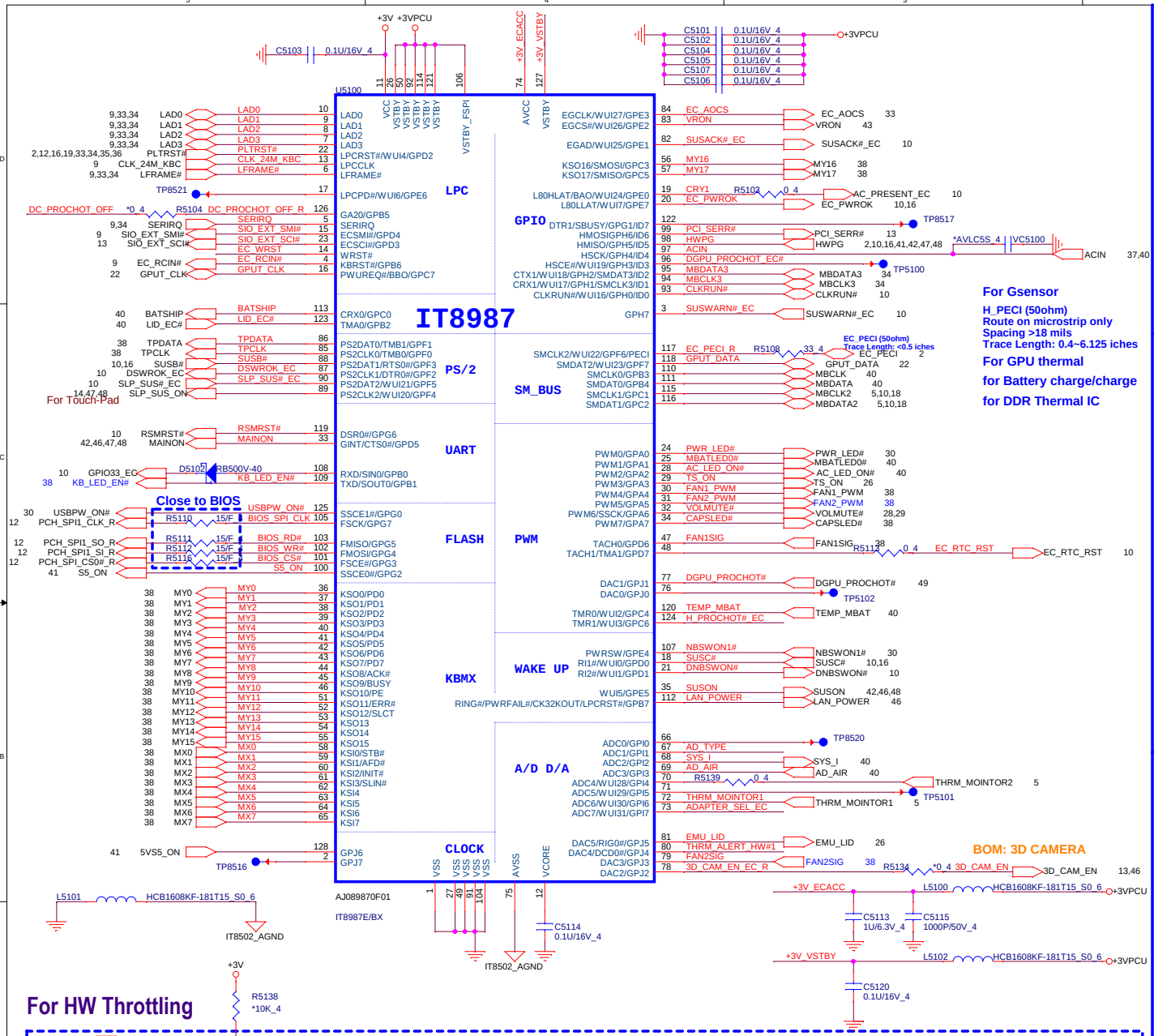


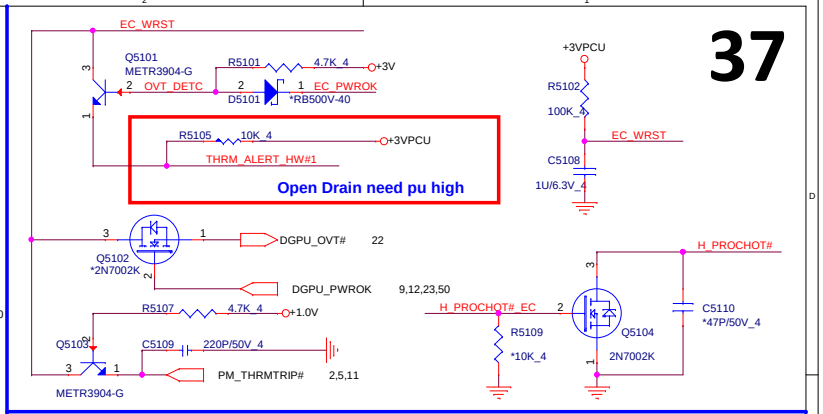
PROJECT : G35

Quanta Computer Inc.

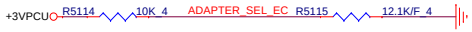
Size	Document Number	Rev
Custom	36 – CR RTS5237S/CR SOCKET	1A

Date: Thursday, December 24, 2015 Sheet 36 of 51



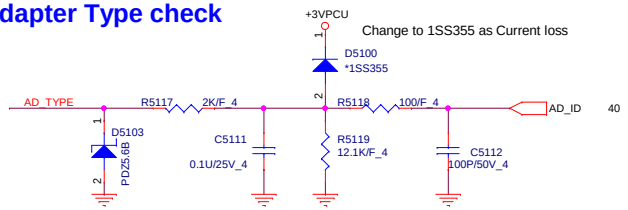


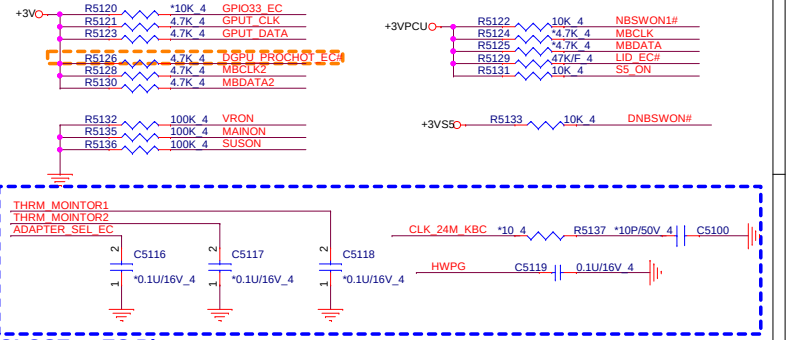
Adapter select for EC



	Ra	Rb	ADAPTER_SEL_EC	BOM
200W	10K(CS31002FB26)	100K (CS41002FB28)	3V	
150W	10K(CS31002FB26)	27.4K(CS32742FB14)	2.42V	
120W	10K(CS31002FB26)	12.1K(CS31212FB28)	1.8V	DIS
90W	10K(CS31002FB26)	6.2K(CS26202FB17)	1.26V	UMA
65W	10K(CS31002FB26)	2.2K(CS22202FB08)	0.59V	
45W	NC	10K(CS31002FB26)	0V	

Adapter Type check

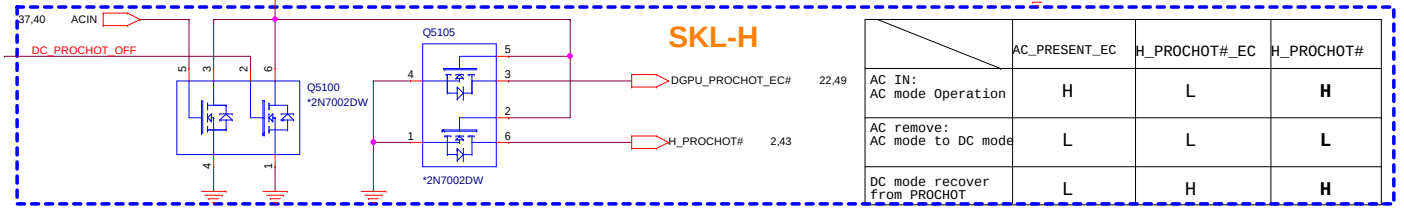




CLOSE to EC Pin

5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,35,36,38,43,46,49 +3V
10,12,14,16,26,33,41,42,46,47,48,51 +3VS5
5,10,30,33,38,40,41 +3VPCU

For HW Throttling



SKL-H

	AC_PRESENT_EC	H_PROCHOT#_EC	H_PROCHOT#
AC IN: AC mode Operation	H	L	H
AC remove: AC mode to DC mode	L	L	L
DC mode recover from PROCHOT	L	H	H

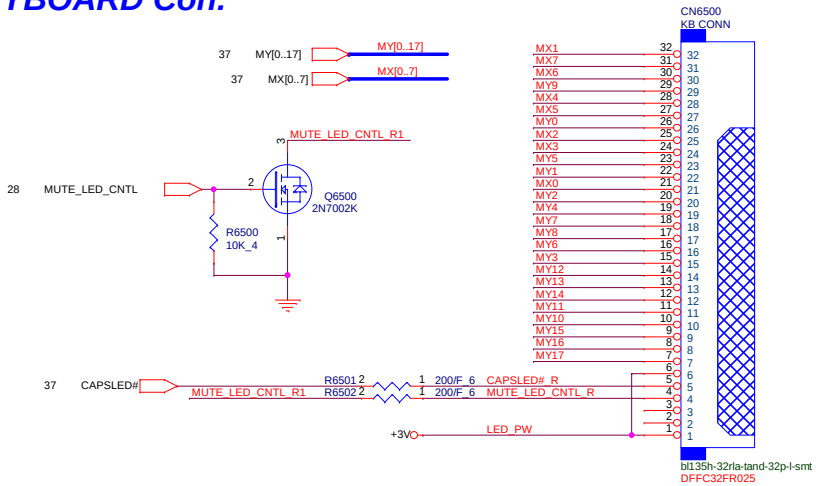
PROJECT : G35

Quanta Computer Inc.

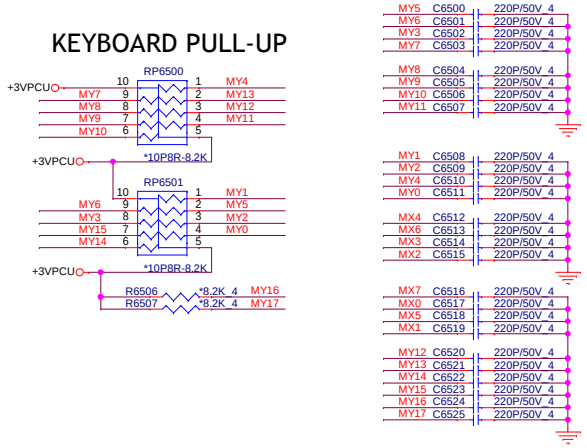
Size	Document Number	Rev
Custom	37 -- EC (IT8987)	1A

Date: Thursday, December 24, 2015 | Sheet 37 of 51

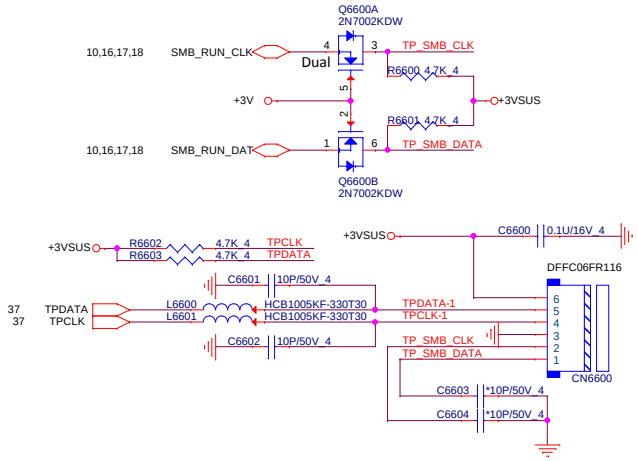
KEYBOARD Con.



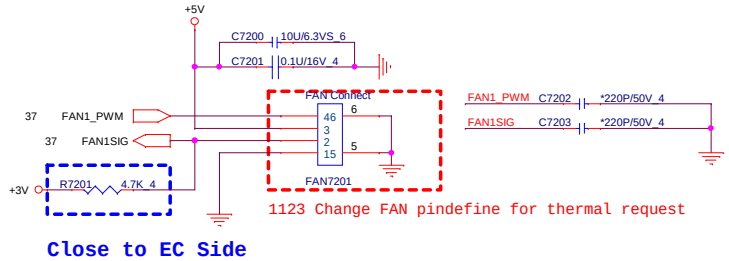
KEYBOARD PULL-UP

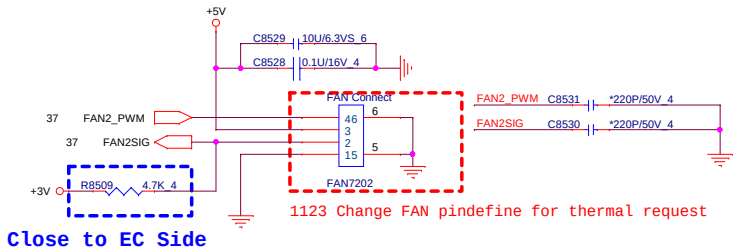


Touch Pad Connector

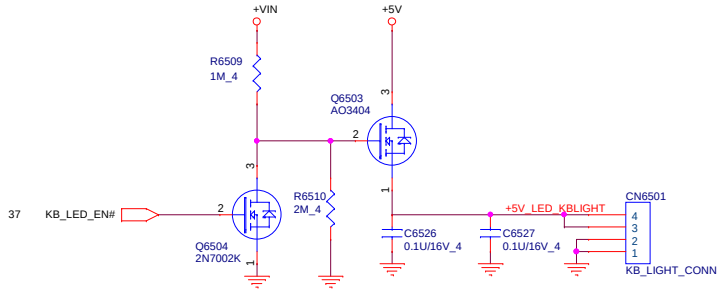


FAN





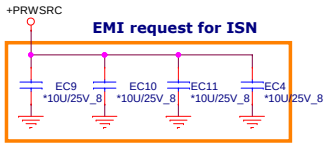
KB LIGHT CONN

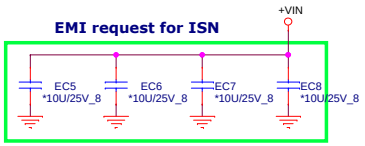


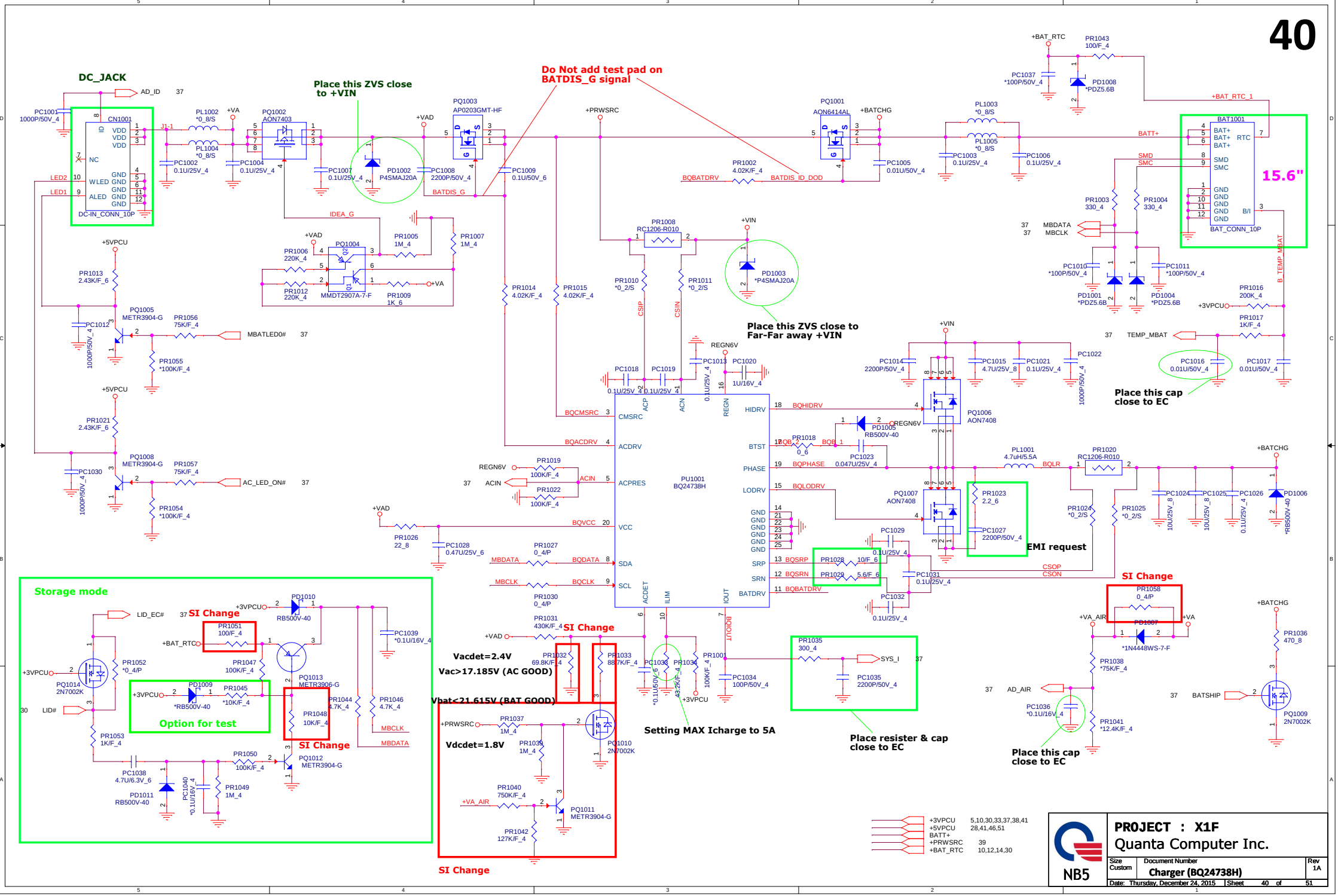
PROJECT : G35
Quanta Computer Inc.

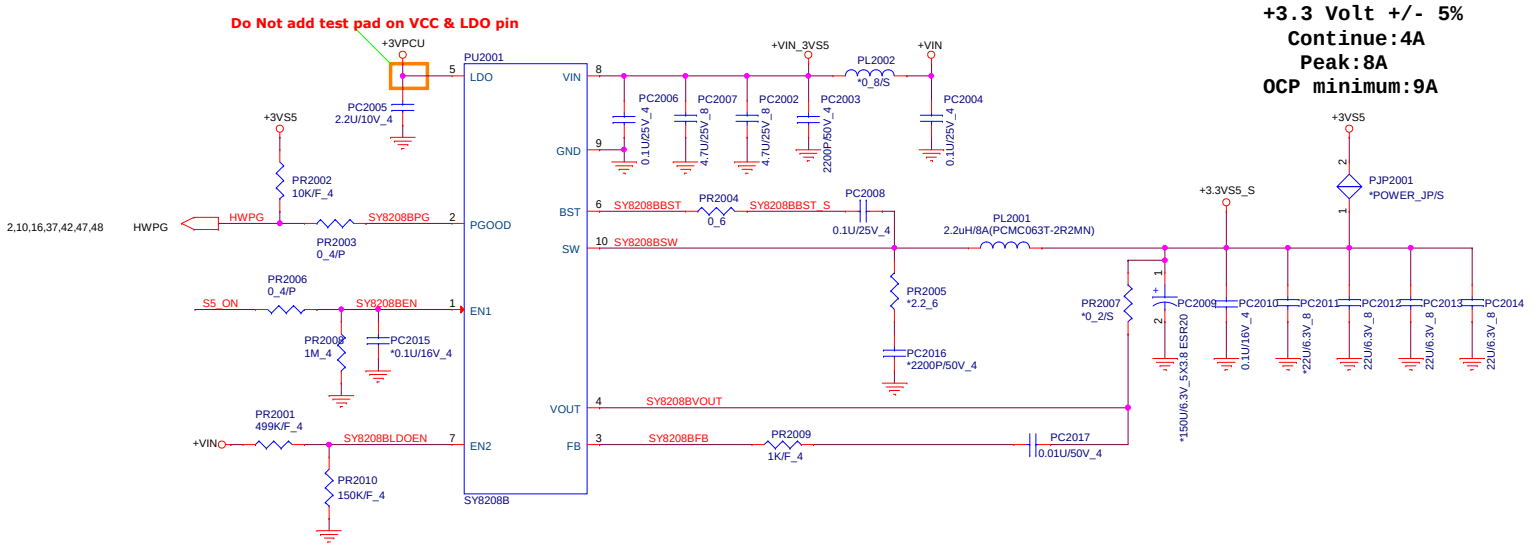
Size	Document Number	Rev
Custom	38 -- KB/TP/FAN/HOLE	1A

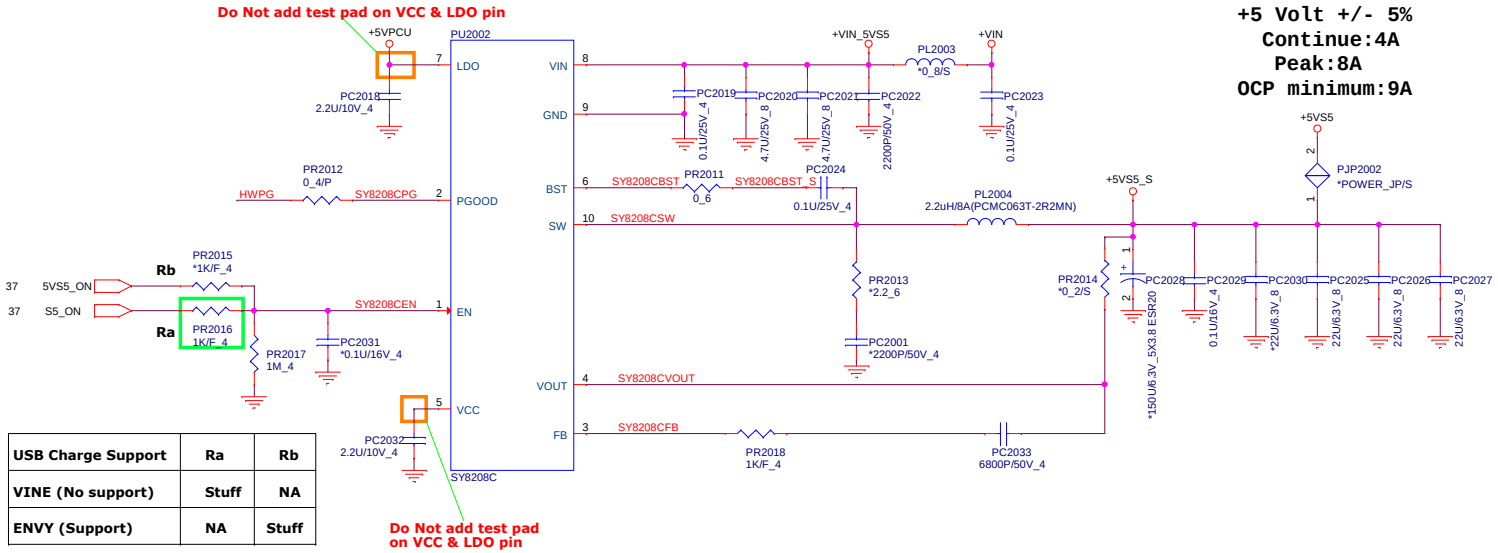
Date: Thursday, December 24, 2015 | Sheet 38 of 51


+PRWSRC
EMI request for ISN
EC9
*10U/25V_8
EC10
*10U/25V_8
EC11
*10U/25V_8
EC4
*10U/25V_8


+VIN
EMI request for ISN
EC5
*10U/25V_8
EC6
*10U/25V_8
EC7
*10U/25V_8
EC8
*10U/25V_8


DC_JACK
Place this ZVS close to +VIN
Do Not add test pad on BATDIS_G signal
Place this ZVS close to Far-Far away +VIN
Place this cap close to EC
EMI request
SI Change
Storage mode
Option for test
Vacdet=2.4V
Vac>17.185V (AC GOOD)
Vbat<21.615V (BAT GOOD)
Vdcdet=1.8V
Setting MAX Icharge to 5A
Place resister & cap close to EC
Place this cap close to EC
15.6"
PU1001 BQ24738H
CN1001
DC-IN_CONN_10P
BAT1001
BAT_CONN_10P
PQ1001 AON6414AL
PQ1002 AON7403
PQ1003 AP0203GMT-HF
PQ1004 MMDT2907A-7-F
PQ1005 METR3904-G
PQ1006 AON7408
PQ1007 AON7408
PQ1008 METR3904-G
PQ1009 2N7002K
PQ1010 2N7002K
PQ1011 METR3904-G
PQ1012 METR3904-G
PQ1014 2N7002K
PD1002 P4SMAJ20A
PD1003 *P4SMAJ20A
PD1005 RB500V-40
PD1006 *RB500V-40
PD1008 *PDZ5.6B
PD1010 RB500V-40
PD1011 RB500V-40
PD1001 *PDZ5.6B
PD1004 *PDZ5.6B
PR1008 RC1206-R010
PR1020 RC1206-R010
PL1001 4.7uH/5.5A
PR1023 2.2_6
PR1027 0_4/P
PR1028 10/F_6
PR1029 5.6/F_6
PR1030 0_4/P
PR1031 430K/F_4
PR1032 69.8K/F_4
PR1033 887K/F_4
PR1034 43.2K/F_4
PR1035 300_4
PR1036 470_8
PR1037 1M_4
PR1038 *75K/F_4
PR1039 *0.1U/16V_4
PR1040 750K/F_4
PR1041 *12.4K/F_4
PR1042 127K/F_4
PR1043 100/F_4
PR1045 *10K/F_4
PR1046 4.7K_4
PR1047 100K/F_4
PR1048 10K/F_4
PR1049 1M_4
PR1050 100K/F_4
PR1051 100/F_4
PR1058 0_4/P
PC1034 100P/50V_4
PC1035 2200P/50V_4
PC1036 *0.1U/16V_4
PC1037 *100P/50V_4
PC1038 4.7U/6.3V_6
PC1039 *0.1U/16V_4
PC1040 *0.1U/16V_4
PD1007 *1N4448WS-7-F
SYS_I
+3VPCU 5,10,30,33,37,38,41
+5VPCU 28,41,46,51
BATT+
+PRWSRC 39
+BAT_RTC 10,12,14,30
NB5
PROJECT : X1F
Quanta Computer Inc.
Size Custom
Document Number
Charger (BQ24738H)
Rev 1A
Date: Thursday, December 24, 2015
Sheet 40 of 51





USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff

Do Not add test pad on VCC & LDO pin

+VIN	26,38,39,40,42,43,44,45,47,48,49,50
+3VS5	10,12,14,16,26,33,37,42,46,47,48,51
+5VS5	10,26,28,30,42,43,44,45,46,47,48,49,50,51
+3VPCU	5,10,30,33,37,38,40
+5VPCU	28,40,46,51

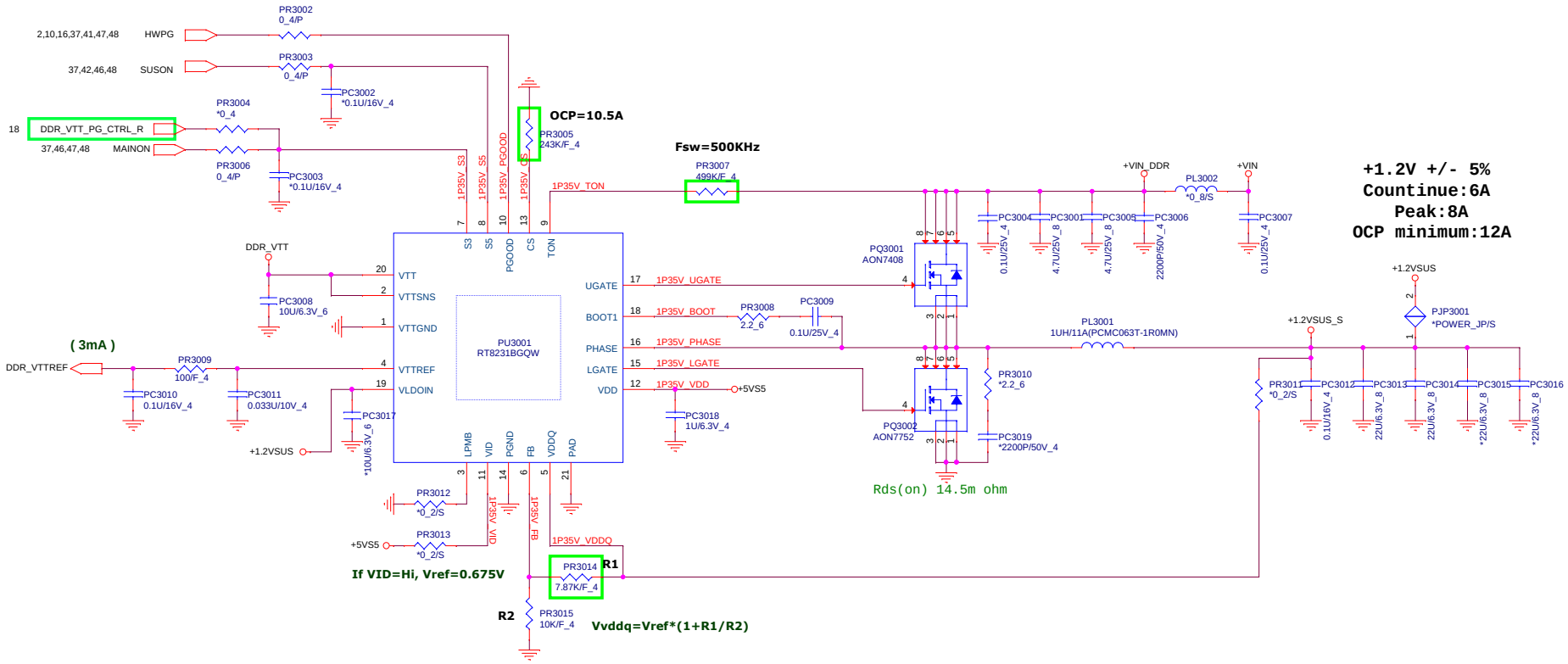
NB5

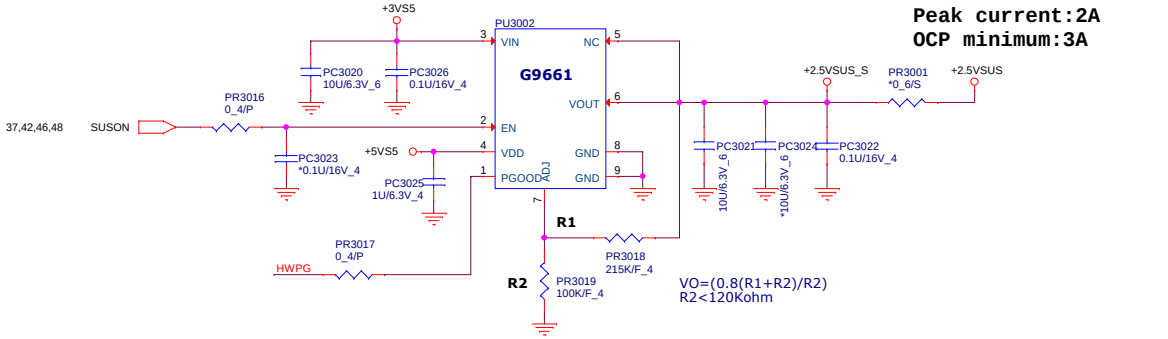
PROJECT : X1F

Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VS5 (SY8208B/SY8208C)	1A

Date: Thursday, December 24, 2015 | Sheet 41 of 51





+VIN	26,38,39,40,41,43,44,45,47,48,49,50
+5VS5	10,26,28,30,41,43,44,45,46,47,48,49,50,51
+1.2VSUS	2,6,10,17,18,48,51
DDR_VTT	17,18
+2.5VSUS	17,18

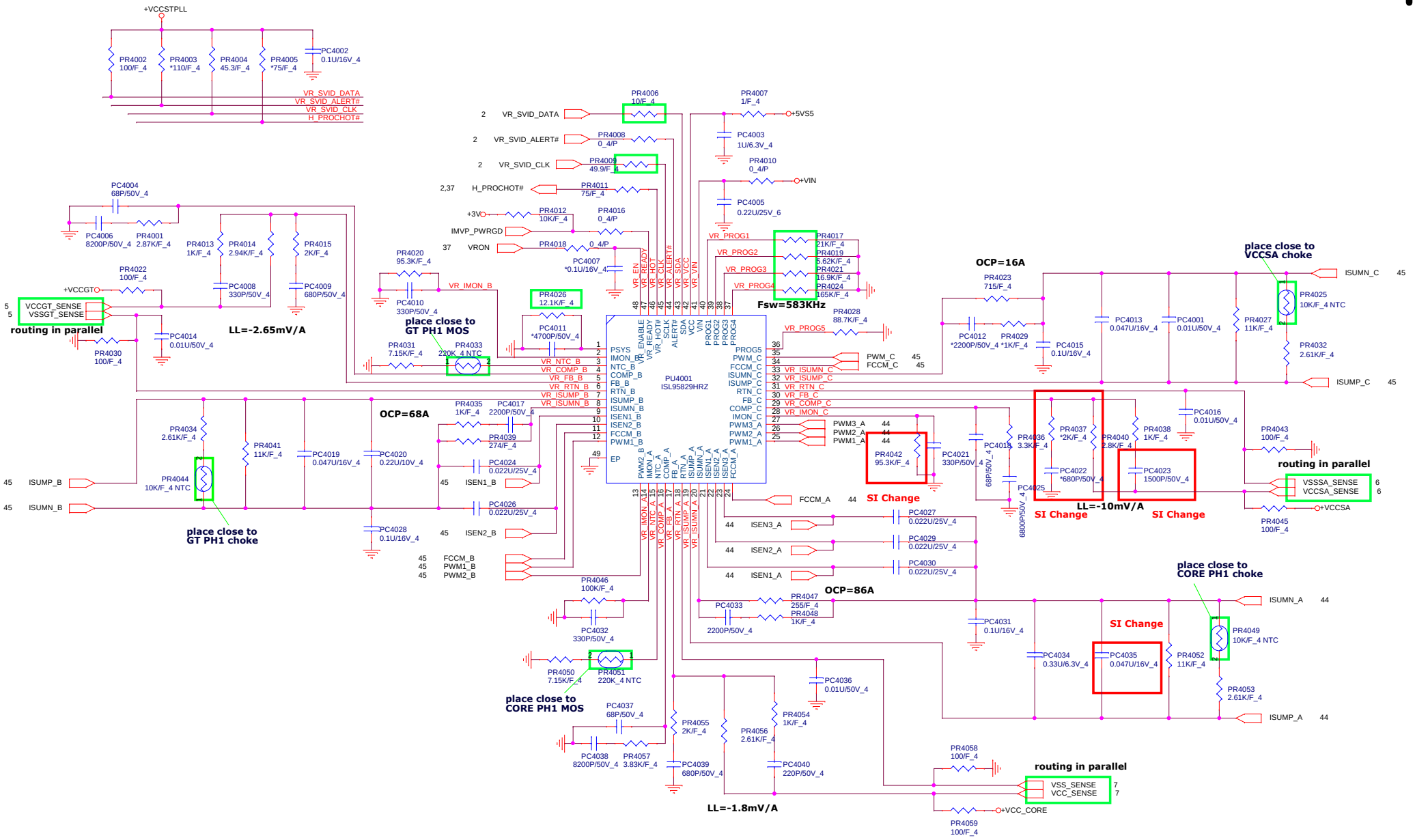
NB5

PROJECT : X1F

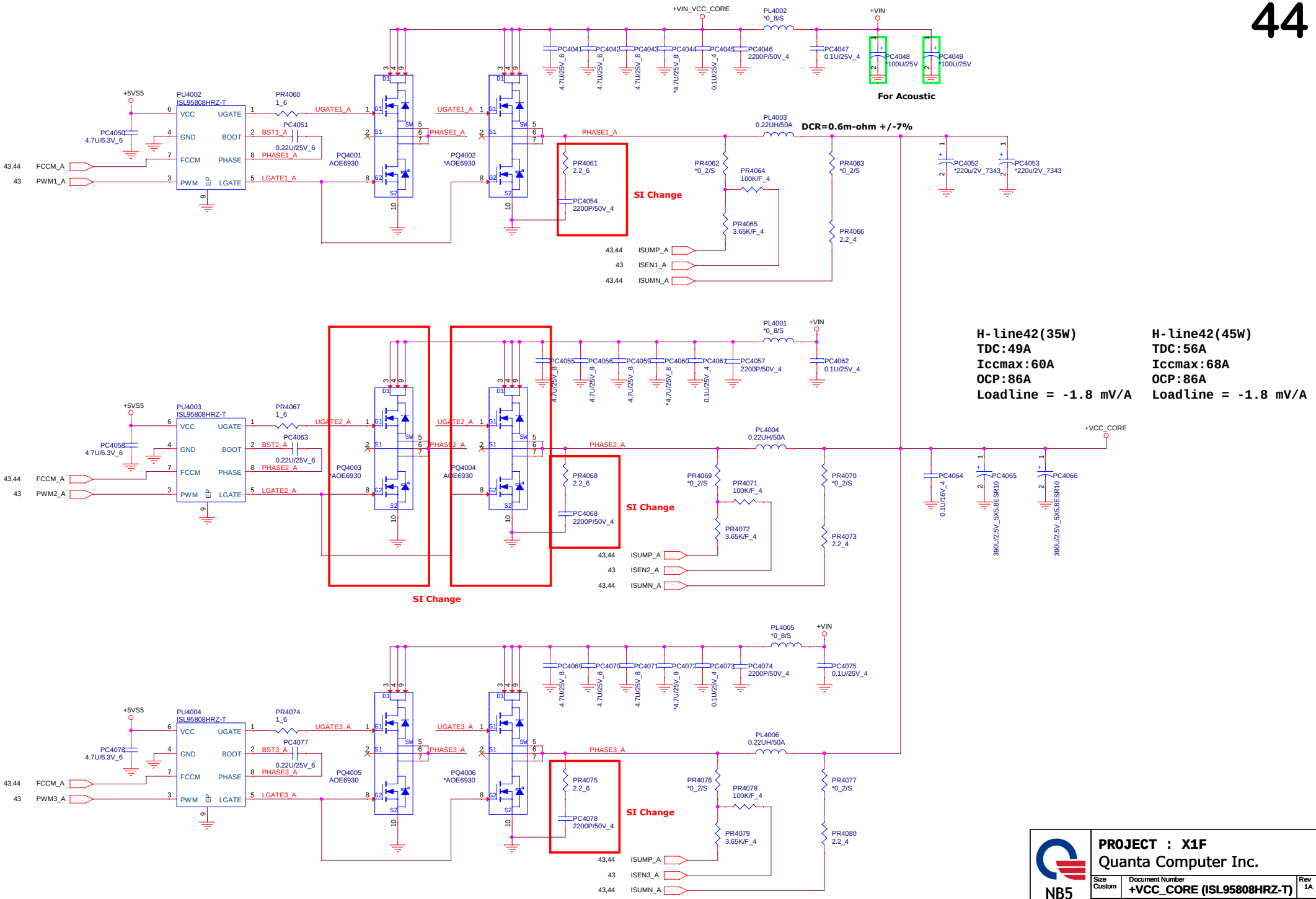
Quanta Computer Inc.

Size	Document Number	Rev
	DDR3 (RT8231B)	1A

Thursday, December 24, 2015 Sheet 42 of 51



NB5	**PROJECT : X1F**
	Quanta Computer Inc.
Size: Custom	Document Number: **CPU VR IC (ISL95829HRZ)** — Rev: 1A
Date: Thursday, December 24, 2015	Sheet 43 of 51



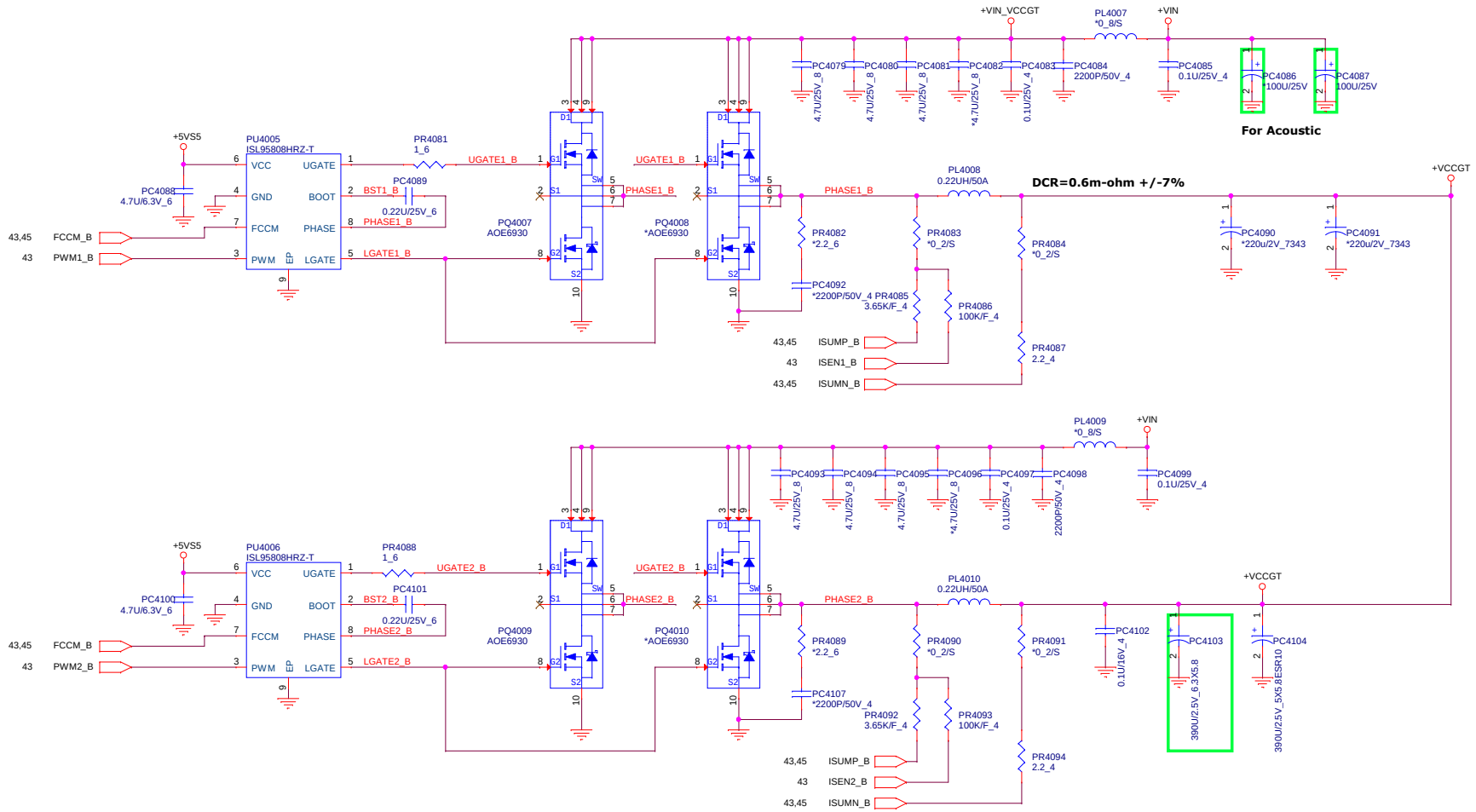
NB5

PROJECT : X1F

Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCC_CORE (ISL95808HRZ-T)	1A

Date: Thursday, December 24, 2015 | Sheet 44 of 51



H-line42(35W)
TDC:41A
Iccmax:55A
OCP:68A
Loadline = -2.65 mV/A

H-line42(45W)
TDC:39A
Iccmax:55A
OCP:68A
Loadline = -2.65 mV/A

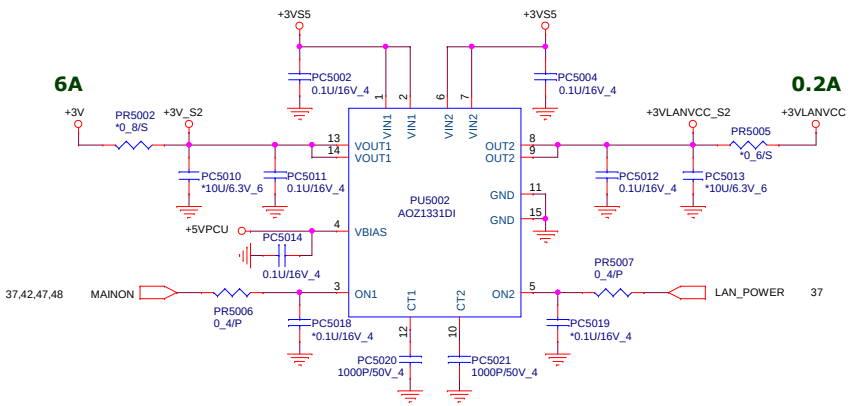
H-line42(35W/45W)
TDC:10A
Iccmax:11A
OCP:16A
Loadline = -10 mV/A

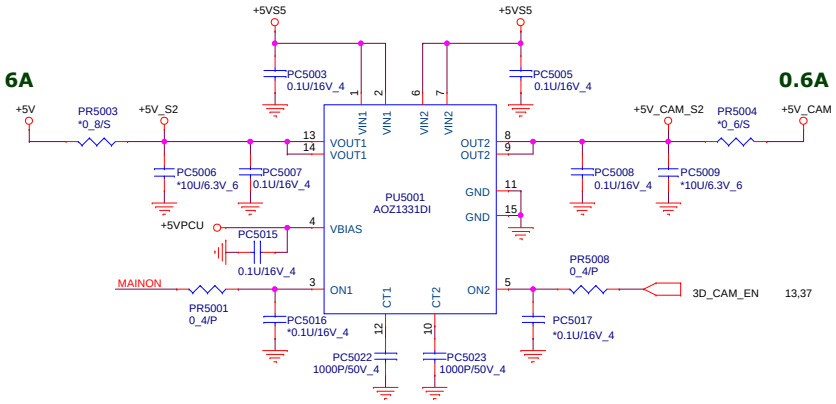
NB5

PROJECT : X1F
Quanta Computer Inc.

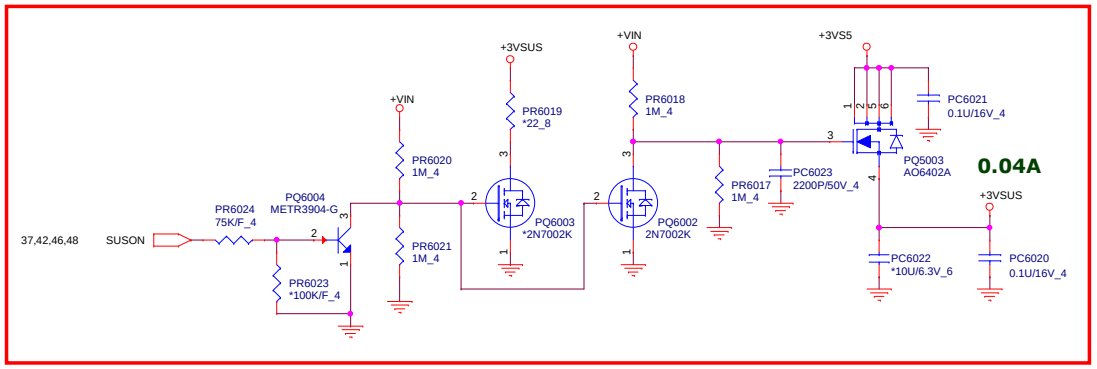
Size	Document Number	Rev
Custom	+VCCGT/SA (ISL95808HRZ-T)	1A

Date: Thursday, December 24, 2015 | Sheet 45 of 51





SI Change



+3V	5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,35,36,37,38,43,49
+5V	26,27,28,29,31,32,38,49
+3VS5	10,12,14,16,26,33,37,41,42,47,48,51
+5VS5	10,26,28,30,41,42,43,44,45,47,48,49,50,51
+3VSUS	38
+3VLANVCC	35
+5V_CAM	31
+3V_DEEP_SUS	9,10,12,13,14,16,18

NB5

PROJECT : X1F

Quanta Computer Inc.

Size	Document Number	Rev
Custom	**Load switch IC (AOZ1331D)**	1A

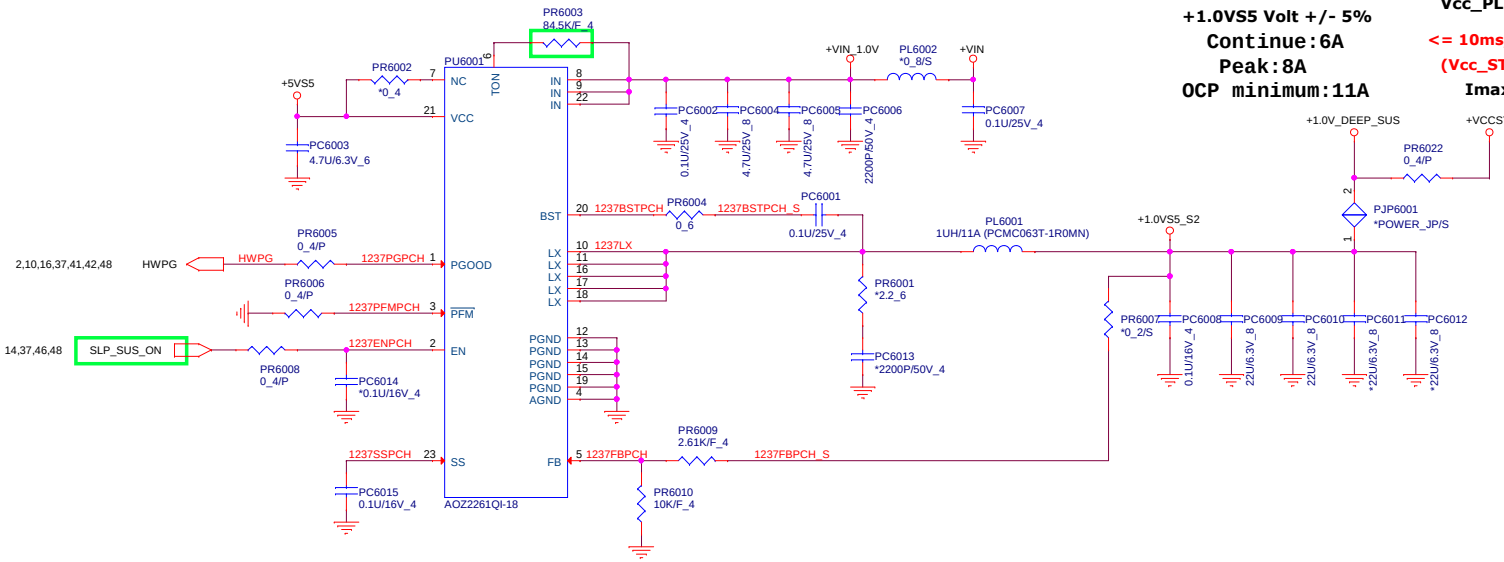
Date: Thursday, December 24, 2015 | Sheet 46 of 51

(V1.00A+V1.00_MODPHY+VccPRIM_CORE)

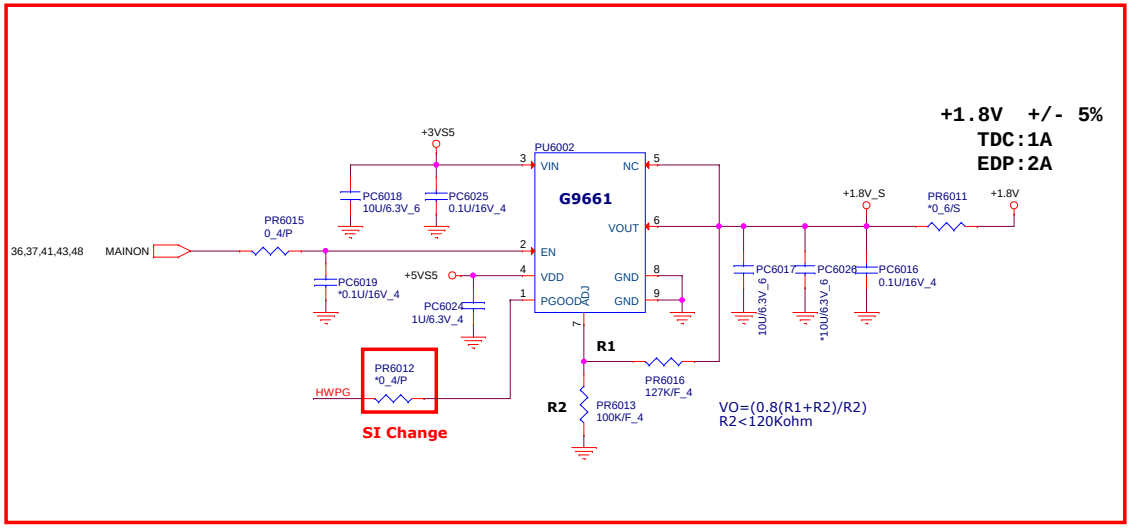
+1.0VS5 Volt +/- 5%
Continue:6A
Peak:8A
OCP minimum:11A

Volume Segment
Vcc_ST: 0.12A
Vcc_PLL: 0.12A

<= 10ms, full load ready
(Vcc_ST+Vcc_PLL)
Imax:0.24A



SI Change



SI Change

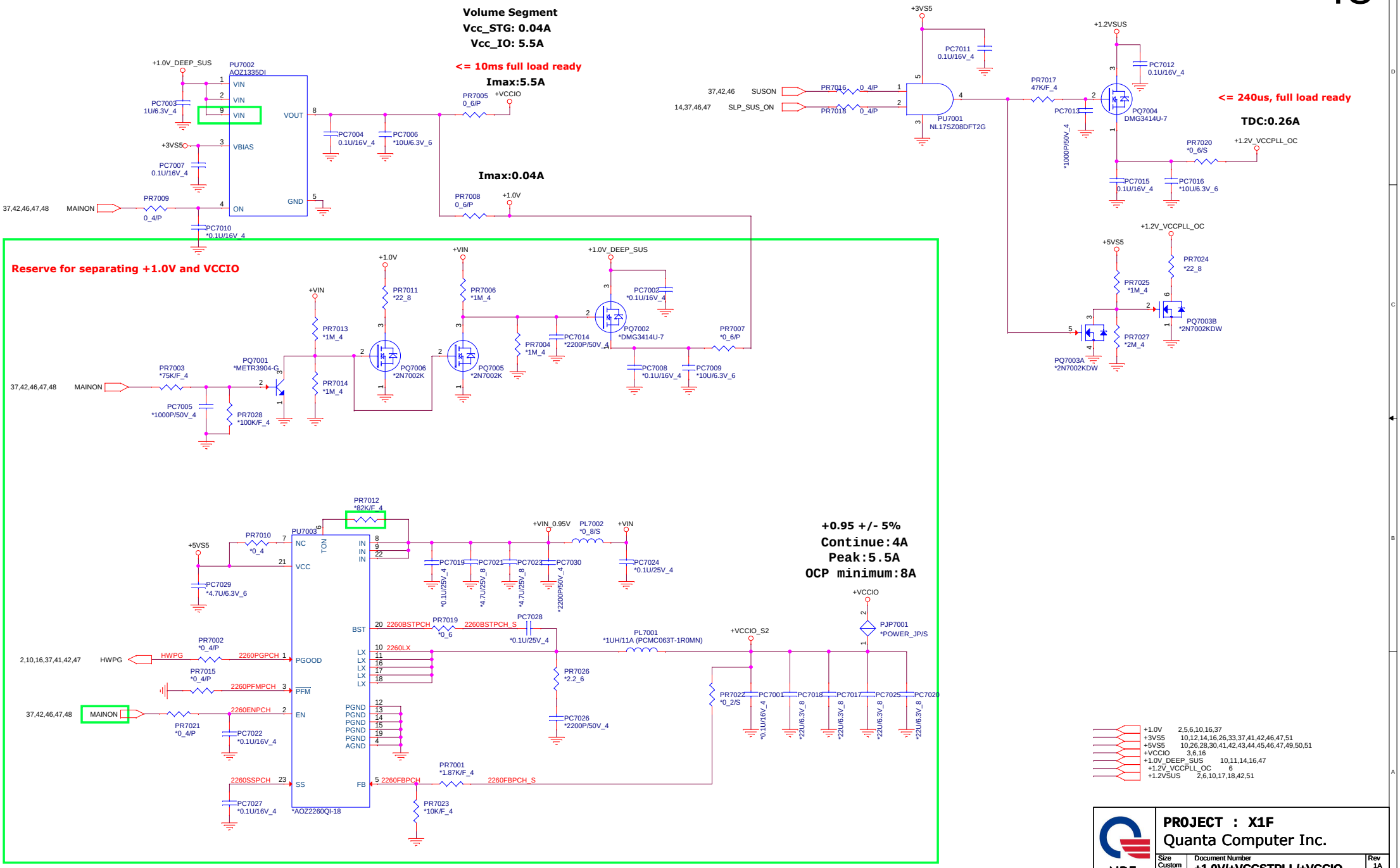
+VIN	26,38,39,40,41,42,43,44,45,48,49,50
+3VS5	10,12,14,16,26,33,37,41,42,46,48,51
+5VS5	10,26,28,30,41,42,43,44,45,46,48,49,50,51
+1.0V_DEEP_SUS	10,11,14,16,48
+1.8V_DEEP_SUS	31
+1.8V	28
+VCCSTPLL	2,6,43

NB5

PROJECT : X1F
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0_DEEP_SUS	1A

Date: Thursday, December 24, 2015 | Sheet 47 of 51



NB5

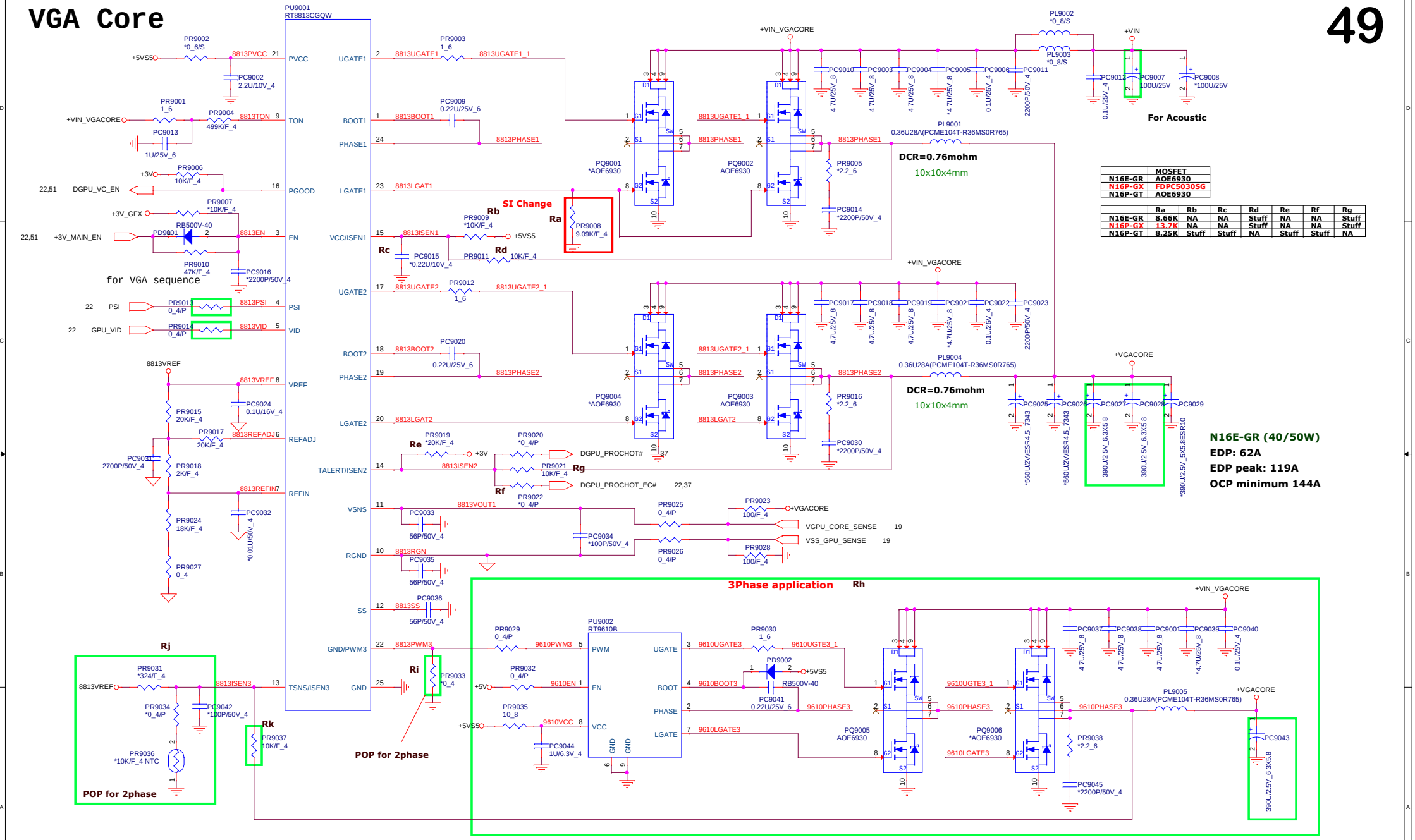
PROJECT : X1F

Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V/+VCCSTPLL/+VCCIO	1A

Date: Thursday, December 24, 2015 | Sheet 48 of 51

VGA Core



	MOSFET
N16E-GR	AOE6930
N16P-GX	FDPC5030SG
N16P-GT	AOE6930

	Ra	Rb	Rc	Rd	Re	Rf	Rg
N16E-GR	8.66K	NA	NA	Stuff	NA	NA	Stuff
N16P-GX	13.7K	NA	NA	Stuff	NA	NA	Stuff
N16P-GT	8.25K	Stuff	Stuff	NA	Stuff	Stuff	NA

	Rh	Ri	Rj	Rk
N16E-GR	Stuff	NA	NA	Stuff
N16P-GX	Stuff	NA	NA	Stuff
N16P-GT	NA	Stuff	Stuff	NA

+3V 5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46
+VIN 26,38,39,40,41,42,43,44,45,47,48,50
+5VS5 10,26,28,30,41,42,43,44,45,46,47,48,50,51
+3V_GFX 19,20,22,23,51
+VGACORE 23

NB5

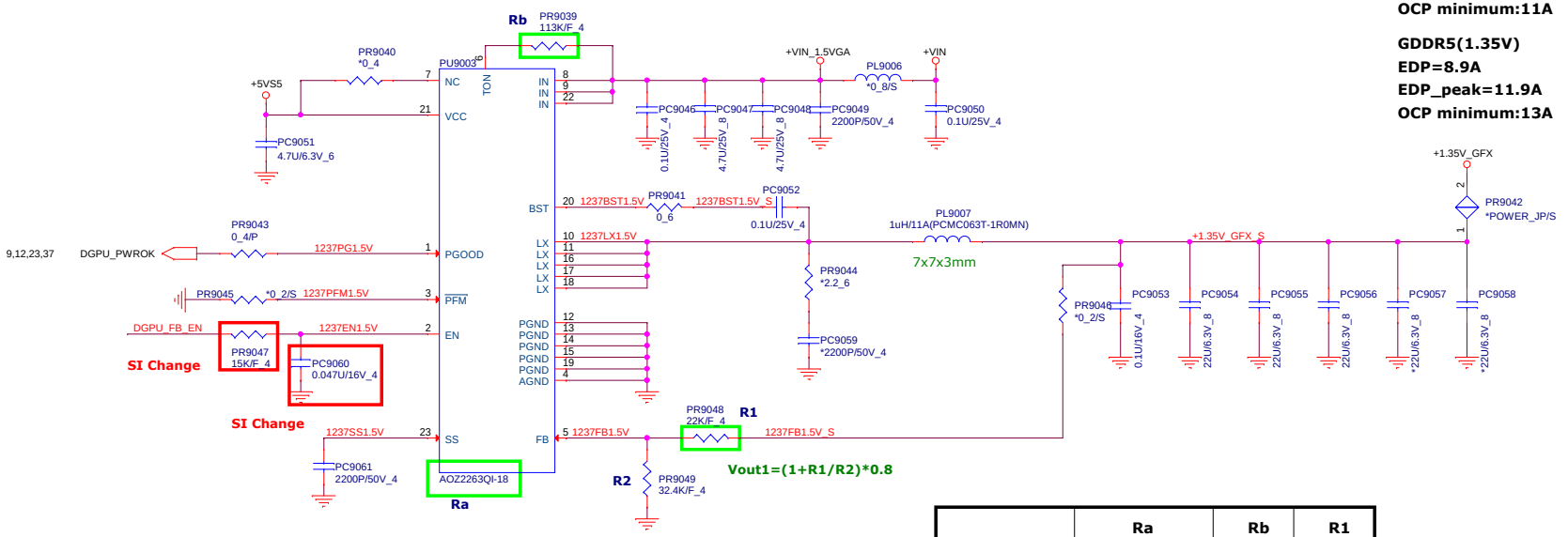
PROJECT : X1Q
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8813C)	1A

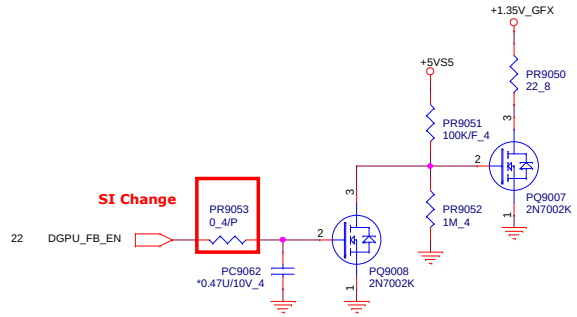
Date: Thursday, December 24, 2015 | Sheet 49 of 51

DDR3(1.5V / 1.35V)
EDP=4.18A
EDP_peak=6.54A
OCP minimum:11A

GDDR5(1.35V)
EDP=8.9A
EDP_peak=11.9A
OCP minimum:13A



	Ra	Rb	R1
DDR3 (1.5V)	AOZ2261QI-18	127K	28.7K
DDR3 (1.35V)	AOZ2261QI-18	113K	22K
GDDR5(1.35V)	AOZ2263QI-18	113K	22K



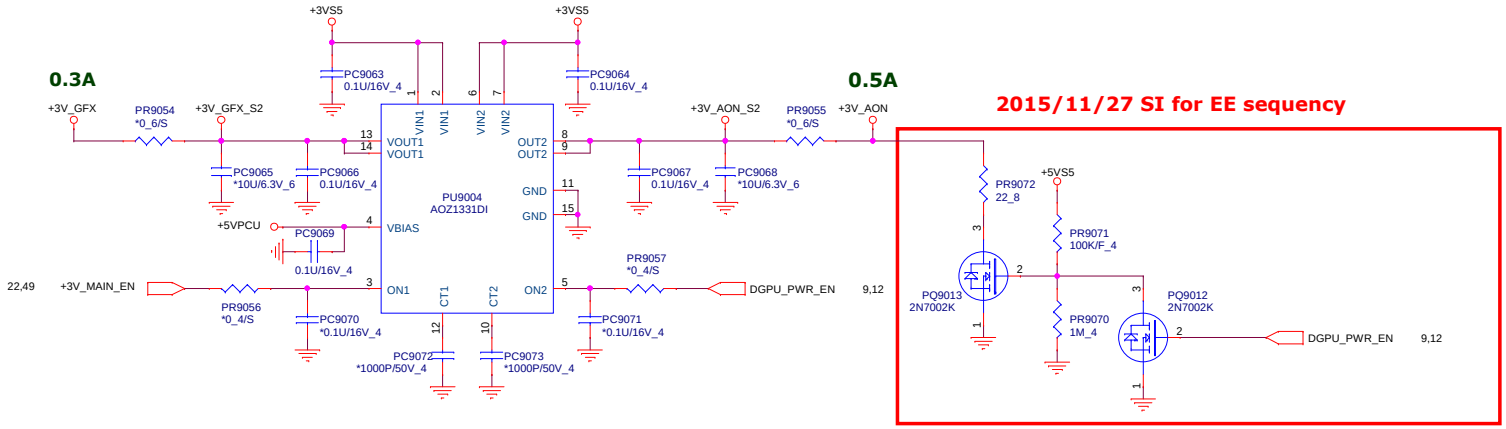
+VIN 26,38,39,40,41,42,43,44,45,47,48,49
+5VS5 10,26,28,30,41,42,43,44,45,46,47,48,49,51
+1.35V_GFX 20,23,24,25

NB5

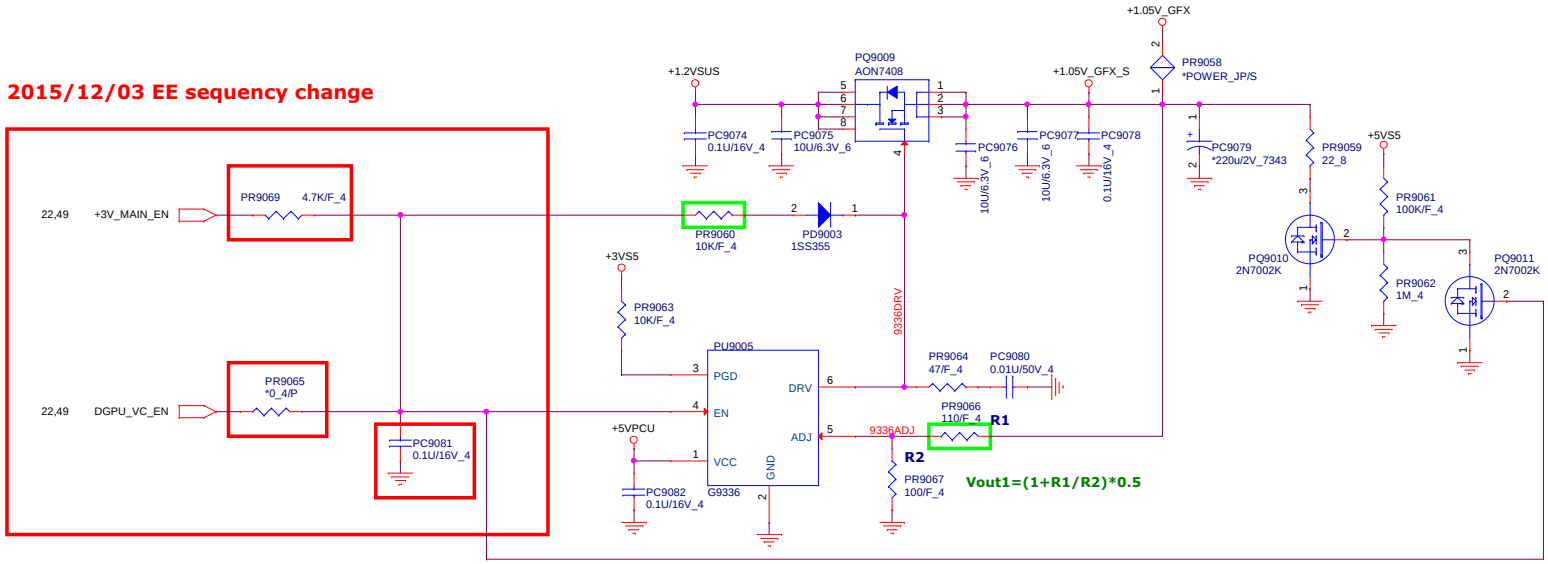
PROJECT : X1Q
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.35V_GFX (AOZ2263QI-18)	1A

Date: Thursday, December 24, 2015 Sheet 50 of 51



+1.05V_GFX Volt +/- 5%
EDP=2.38A
EDP_peak = 2.45A



+VIN	26,38,39,40,41,42,43,44,45,47,48,49,50
+3VS5	10,12,14,16,26,33,37,41,42,46,47,48
+5VS5	10,26,28,30,41,42,43,44,45,46,47,48,49,50
+3V_GFX	19,20,22,23,49
+3V_AON	19,22,23
+1.2VSUS	2,6,10,17,18,42,48
+1.05V_GFX	19,20,21,23

NB5

PROJECT : X1Q
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+3V/+1.05V_GFX(AOZ1331DI)	1A

Date: Thursday, December 24, 2015 | Sheet 51 of 51